EVR_LTR_220213
Enclosure 4

WCAP-18762-NP, Revision 0
"Advanced Logic System® v2 Platform Topical Report"
(Non-Proprietary)

Westinghouse Electric Company
1000 Westinghouse Drive
Cranberry Township, PA 16066

WCAP-18762-NP
Revision 0

December 2022

Advanced Logic System® v2 Platform Topical Report

WCAP-18762-NP
Revision 0

Advanced Logic System® v2 Platform Topical Report

Warren R. Odess-Gillett*

Licensing Engineering

December 2022

Reviewer: Mathew A. Shakun*, Principal Licensing Engineer
Licensing Engineering

Verifier: Thomas Tweedle*, Principal Engineer
Advanced Reactors and Engineering

Approved: Anthony Schoedel*, Manager
Advanced Reactors Licensing

Approved: James F. Mermigos*, Manager
Instrumentation & Monitoring Systems

*Electronically approved records are authenticated in the electronic document management system.

Westinghouse Electric Company LLC
1000 Westinghouse Drive
Cranberry Township, PA 16066, USA

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ACRONYMS AND TRADEMARKS

Acronym	Definition
2oo3	Two out of three
ADC	Analog-to-Digital Conversion
ALS	Advanced Logic System
ALS v2	Advanced Logic System version 2
ASU	ALS Service Unit
ATCT	ALS Test and Calibration Tool
CCC	Clock Conditioning Circuit
CCF	Common Cause Failure
CLB	Core Logic Board
CMT	Clock Management Technology
CRC	Cyclic Redundancy Check
DI&C	Digital Instrumentation and Control
DLL	Delay Locked Loops
ECC	Error Correction Code
EMC	Electromagnetic Compatibility
EQ	Equipment Qualification
ESFAS	Engineered Safety Features Actuation System
FIFO	First In First Out
FMEA	Failure Modes and Effects Analysis
FPA	Failure Path Analysis

Acronym	Definition
FPGA	Field Programmable Gate Array
Gbps	Gigabits per Second
HMI	Human Machine Interface
HP	Horizontal Pitch
I&C	Instrumentation and Control
I/O	Input / Output
IDE	Integrated Design Environment
IDI	Isolated Development Infrastructure
IV&V	Independent Verification and Validation
Kbits	Kilobits
Kb	Kilobytes
LAR	Licensing Amendment Request
LC	Inductor and Capacitor
LED	Light Emitting Diode
LSRAM	Large Static Random Access Memory
LUT	Lookup Table
MMCM	Mixed-Mode Clock Manager
Mbps	Megabits Per Second
MTBF	Mean Time Between Failures
nm	nanometer
NRC	Nuclear Regulatory Commission

Acronym	Definition
NVM	Nonvolatile Memory
PAMS	Post-Accident Monitoring System
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
PROM	Programmable Read Only Memory
RAB	Reliable ALS Bus
RAM	Random Access Memory
RLET	Reusable Logic Element
ROM	Read Only Memory
RPS	Reactor Protection System
RTD	Resistance Temperature Detector
RTL	Register Transfer Language
RVLIS	Reactor Vessel Level Indicating System
SE	Safety Evaluation
SoC	System on a Chip
SSPCE	Safety System Platform Change Evaluation
SRAM	Static Random Access Memory
SRP	Standard Review Plan
TAB	Test ALS Bus
TC	Thermocouple
TC/CCM	Thermocouple / Core Cooling Monitor

Acronym	Definition
TVS	Transient Voltage Suppression
v2	Version 2
V&V	Verification and Validation

[

]a,c

REFERENCES

1. 6002-00301-P-A, Rev. 4, “Advanced Logic System Topical Report,” Westinghouse Electric Company LLC.
2. EVR-ACS-GL-001, Rev. 0, “Advanced Logic System v2 Platform Licensing Strategy,” Westinghouse Electric Company LLC.
3. 6002-00008, Rev. 7, “ALS Application Guidance,” Westinghouse Electric Company LLC.
4. IEC-61000-4-2, “Electromagnetic Compatibility – Part 4-2; Testing and Measurement Techniques. Electrostatic Discharge Immunity Test,” Edition 2, International Electrotechnical Commission.
5. WCAP-18780-P, Rev. 0, “Advanced Logic System v2 Development Process Topical Report,” Westinghouse Electric Company LLC.
6. WNA-PV-00129-GEN, Rev. 0, “Advanced Logic System v2 Software Verification and Validation Plan,” Westinghouse Electric Company LLC.
7. ML17111A596, “Safety Evaluation By The Office Of New Reactors Licensing Topical Report (TR) 1015-18653-P (Revision 2) “Design Of The Highly Integrated Protection System Platform” Nuscale Power, LLC, Docket: PROJ0769,” US Nuclear Regulatory Commission.
8. 6003-00004, Rev. 2, “ALS v2 Equipment Qualification Plan,” Westinghouse Electric Company LLC.
9. 6002-00006, Rev. 3, “ALS Security Plan,” Westinghouse Electric Company LLC.
10. 6003-00000, Rev. 4, “ALS v2 Project Management Plan,” Westinghouse Electric Company LLC.
11. 6003-00011, Rev. 1, “ALS v2 Platform Design Specificaiton,” Westinghouse Electric Company LLC.
12. 6003-00010, Rev. 1, “ALS v2 Platform Requirements Specification,” Westinghouse Electric Company LLC.
13. NA 4.54, Rev. 2, “I&C Standard Safety System Platform Configuration Control Process,” Westinghouse Electric Company LLC.

1 INTRODUCTION

The Nuclear Regulatory Commission (NRC) reviewed and approved the Advanced Logic System® (ALS) platform in September 2013 (Reference 1). This topical report describes the enhancements to create the second generation of ALS platform, or ALS version 2 (v2).

The ALS v2 platform is based on the field programmable gate array (FPGA)-based ALS. The ALS v2 platform design program follows a similar approach for design, testing, and qualification that was utilized for the ALS platform.

Similar to the ALS platform, ALS v2 is comprised of one or more application-specific core logic boards (CLBs) and a set of generic slave boards to provide input / output (I/O) functions. These ALS v2 platform boards are configured for a specific nuclear application.

1.1 EXISTING ALS PLATFORM

The existing ALS platform is described in Reference 1. It is comprised of six standardized printed circuit boards (PCBs), which provide generic I/O capabilities and do not require application-specific FPGA programming. The seventh board, the CLB, does require application-specific FPGA programming. The use of each PCB requires configuration of its internal nonvolatile memory (NVM) settings to select the functionality needed to meet application specifications from the options specified to be available for the circuit board. ALS platform boards are described in Table 1-1.

Table 1-1: Existing ALS Platform Boards

Part Number	Board Type	Channels	Description
ALS-102	Core Logic	N/A	FPGA-Based Logic Board
ALS-302	Digital Input	32	Contact Input Board
ALS-311	Analog Input	8	Thermocouple (TC) / Resistance Temperature Detector (RTD) Input Board
ALS-321	Analog Input	8	Voltage / Current Input Board
ALS-402	Digital Output	16	Solid State Contact Output Board
ALS-421	Analog Output	8	Voltage / Current Output Board
ALS-601	Communications	8	EIA-422 / 485 Communication Board

ALS platform boards are interconnected with a platform standard communication bus architecture. This bus architecture comprises the reliable ALS bus (RAB) and test ALS bus (TAB). The RAB is composed of two redundant buses identified as RAB1 and RAB2. Figure 2-2 in Reference 1 describes the ALS platform architecture in the general context of an application with one CLB, three input boards, two output boards, and one communication board. An ALS service unit (ASU) connector is provided to facilitate TAB connection to a human-machine interface (HMI) system for board testing and calibration functions.

1.2 SCOPE

The scope of this topical report is to describe the changes from the NRC-approved ALS platform to make the ALS v2 platform. References will be made to the original topical report (Reference 1) when the ALS v2 has the same design and processes as the existing ALS platform.

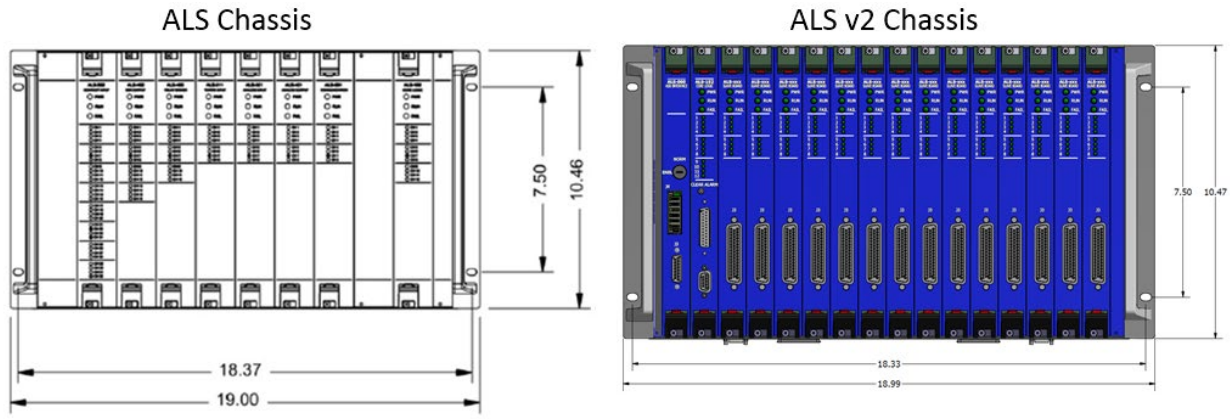
2 SUMMARY OF CHANGES FOR ALS V2

The ALS platform changes for ALS v2 comprises six categories of enhancements. Collectively, the enhancements yield the ALS v2 platform. As described in EVR-ACS-GL-001 (Reference 2), there are six categories of changes to the ALS platform planned for the ALS v2. Four of the six categories are included in this topical report for NRC review (Categories 1, 2, 4, and 6). These categories of changes support digital instrumentation and control (DI&C) upgrades for current operating nuclear power plants; whereas Categories 3 and 5 are specifically needed to support the eVinci microreactor and have a later development lifecycle. Category 3 and 5 changes will be submitted for NRC review in a separate or revised topical report for ALS v2 in the future. The category numbering is maintained for consistency with Reference 2. Therefore, this section will describe Category 1, 2, 4, and 6 changes.

2.1 CATEGORY 1 CHANGES

Category 1 changes are related to reducing chassis footprint and increasing I/O density. This is accomplished by reducing the ALS v2 board depth and width, therefore increasing the maximum number of ALS v2 boards within a 19-inch rack mount chassis assembly. The ALS v2 boards and chassis are redesigned so that 16 boards can fit in the same width and height as the existing 10-board ALS chassis. Figure 2-1 shows a comparison of the ALS and ALS v2 chassis with dimensions.

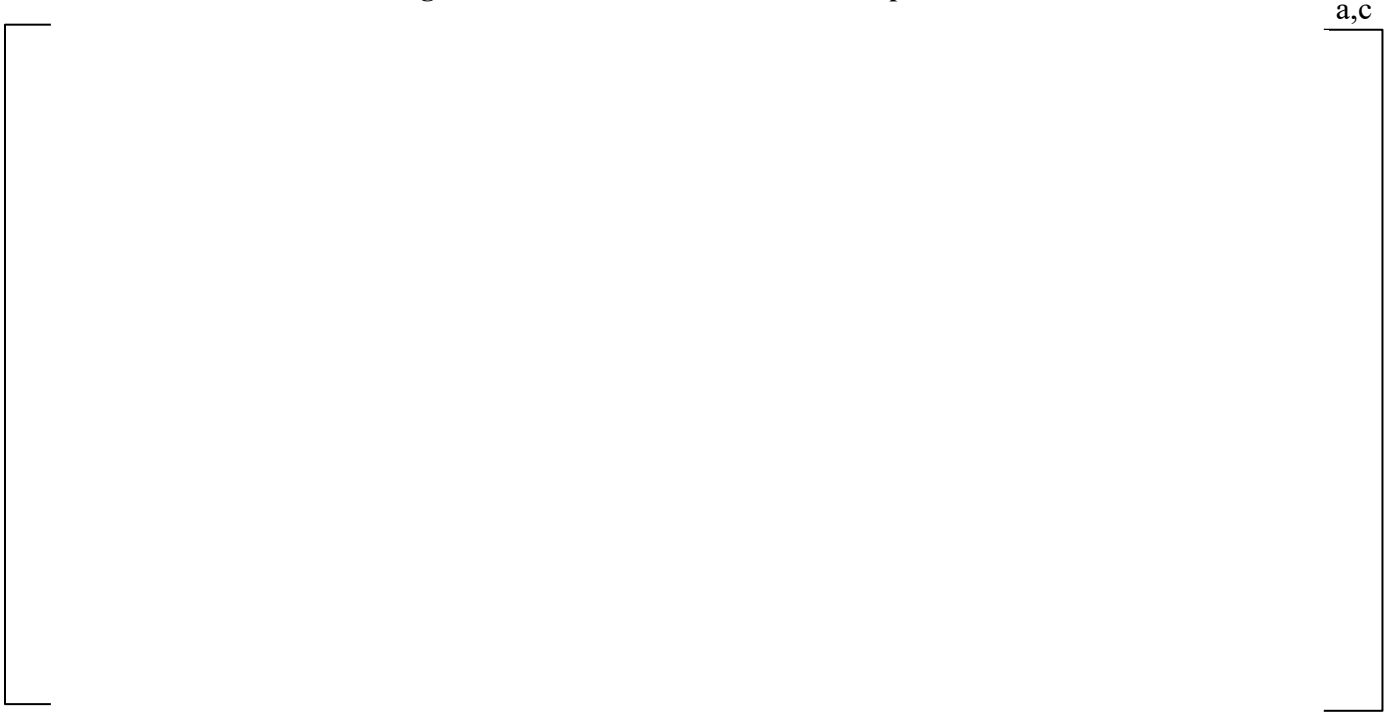
Figure 2-1: ALS vs. ALS v2 Chassis with Boards



There will also be a reduction in the overall depth of the chassis and the field connectors will move to the front versus being in the rear. Figure 2-2 provides a comparison of the ALS and ALS v2 board.

Figure 2-2: ALS vs. ALS v2 Board Comparison

a,c



This change in form factor is one of the key differentiators between ALS and ALS v2. This change only affects the hardware and mechanical design of the ALS v2 platform boards with no impact on functionality. The ALS v2 board numbers will change to designate the difference between ALS and ALS v2, as shown in Table 2-1.

Table 2-1: ALS vs. ALS v2 Platform Boards

Board Type	ALS Board Number	ALS v2 Board Number
Core Logic	ALS-102	ALS-152
Digital Input	ALS-302	ALS-352
Analog Input RTD and TC	ALS-311	ALS-361
Analog Input	ALS-321	ALS-371
Digital Output	ALS-402	ALS-452
Analog Output	ALS-421	ALS-471
Communications	ALS-601	ALS-651

2.2 CATEGORY 2 CHANGES

Category 2 changes relate to providing improved usability of the ALS v2 platform. These improvements are as follows:

- Implementing a 24Vdc board power supply for ALS v2 boards. ALS platform boards required 48Vdc. Utilizing 24Vdc for board power better aligns with Westinghouse standard cabinet designs.

- Implementing a standard backplane and chassis assembly for the ALS v2 platform. Included are:

  — A 16-slot standard backplane and chassis assembly.

  — A split backplane and chassis assembly derived from the 16-slot assembly. The split backplane allows for two ALS v2 systems (two CLBs) to operate independently in one physical chassis. Each half of the split backplane provides eight board slots. Each half of the backplane is electrically isolated from the other half, including power input and communication buses.

  — The standard 16-slot and split backplane chassis assemblies will also be tested and qualified as expansion chassis assemblies.

- Implementing a new ASU interface and power interconnection board for the ALS v2 platform. This board has no FPGA. This board is a hardware-based extension of the chassis power and TAB connections and can be used in applications where the chassis bottom power and TAB connectors are not accessible due to cabinet space constraints (refer to Reference 1, Section 5.3.3 for the existing ALS ASU interface over the TAB).

Category 2 enhancements also address two application restrictions on the existing ALS as documented in 6002-00008 (Reference 3):

- Increased rating of the 3.3Vdc board power supply [

  ]^{a,c}

- Hardware changes to the ALS-452 (derived from the ALS-402) [

  ]^{a,c}

The modification in application restrictions for ALS v2 will be documented in a separate application restrictions document, 6003-00008, “ALS v2 Application Guidance.”

2.3 CATEGORY 4 CHANGES

Category 4 changes relate to the design, qualification, and testing of new FPGA daughter cards for the ALS v2 platform. In the daughter card design, the FPGA and associated circuitry is transferred from the base I/O board and CLB and placed on a removable daughter card. With this design, different FPGAs can be used on the same base I/O board or CLB. This design enables a hardware-diverse implementation for the boards in the ALS v2 platform.

Three new daughter cards listed below comprise the Category 4 enhancements. Note ALS-851 is reserved for future use.

- ALS-850, [ ][a,c] FPGA Daughter Card
- ALS-852, [ ][a,c] FPGA Daughter Card
- ALS-853, [ ][a,c] FPGA Daughter Card

2.4 CATEGORY 6 CHANGES

Category 6 changes relate to creating reusable logic elements (RLETs) for common functions in the ALS v2 platform FPGA designs. The intent of this ALS v2 platform enhancement is to create a library of RLETs that are verified and validated as nuclear safety-related functions one time, then reused in future designs. By reusing RLETs that are already verified and validated, the verification and validation (V&V) effort for an application is more efficient.

3 ALS V2 DESIGN DESCRIPTIONS

Unless otherwise stated, the descriptions in the ALS Topical Report (Reference 1) apply to the ALS v2. This section provides detail to the summary of changes described in Section 2.

3.1 ALS V2 BACKPLANE

The ALS-050 is the standard backplane PCB for ALS v2 (see Figure 3-1). The ALS-050 has 16 slots for ALS v2 boards. The ALS-050 is mounted to the backplate of the chassis forming the ALS-010 ALS v2 standard chassis assembly (see Figure 3-2). The ALS-050 is standardized for all applications. Multiple ALS v2 chassis assemblies can be connected via rack expansion cable(s) if more boards are needed for a particular application. The ALS v2 internal bus architecture allows for up to 60 boards to be connected in four locally connected chassis assemblies (one main chassis and three expansion chassis connected).

Figure 3-1: ALS v2 Standard Backplane PCB

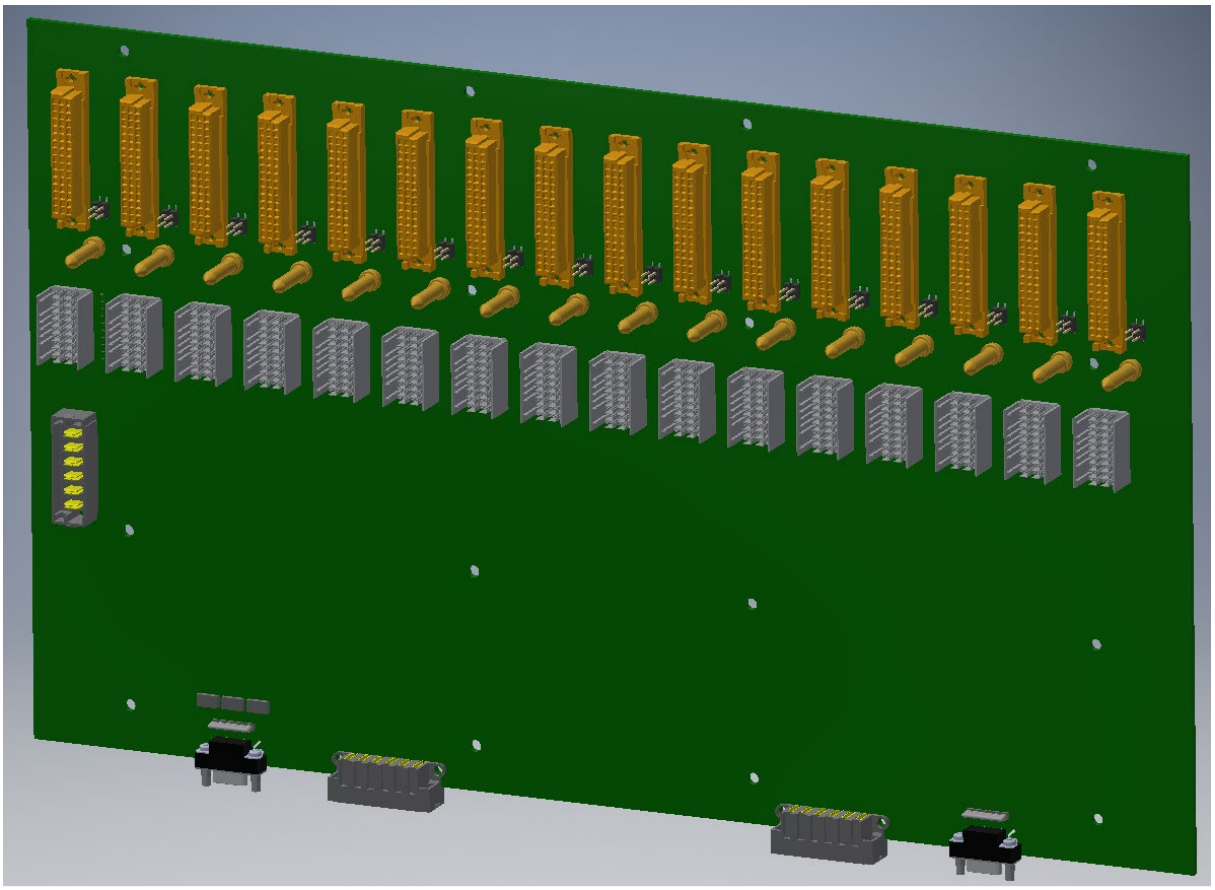
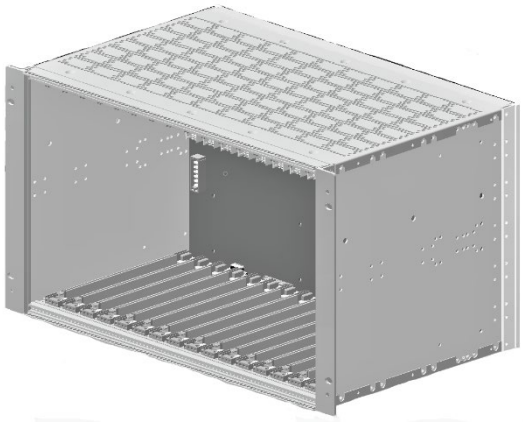


Figure 3-2: ALS v2 Standard Chassis Assembly with ALS-050 Backplane PCB



The ALS v2 board connectors are mounted on the front side of the backplane PCB. When the ALS v2 boards are inserted into the chassis assembly, these connectors will mate with the board. The backplane PCB provides all electrical connections between the ALS v2 boards, and connections to power, ASU (TAB), and the bus expansion to other ALS v2 chassis assemblies (RABs and TAB). The connections to the field, including inputs, outputs, and/or communications, are done through the D-Sub type connector, which are soldered directly to the ALS v2 board PCB and mounted on the ALS board front faceplate (see Figure 3-2).

There are no active components on the ALS backplane, [

]^{a,c}

The ALS v2 backplane can also be configured for a split backplane. The PCB for a split backplane is designated as ALS-055. The ALS-055 has 16 slots split for two groups of ALS boards. Each side of the ALS-055 is electrically isolated (e.g., each split backplane has a separate 24Vdc input and digital ground circuits). The ALS-055 is mounted to the backplate of the chassis forming the ALS-015 ALS v2 Split Chassis Assembly. Figure 3-3 is a diagram of the functional architecture of the ALS v2 split backplane.

Figure 3-3: ALS v2 Split Backplane Functional Architecture Diagram

a,c

Each group has a dedicated slot and seven general purpose slots for a CLB and slave boards (i.e., I/O and ALS-651 boards). The dedicated slot is the only slot that can be used for the ASU interface board (ALS-060), but it will accept other board types as well.

3.2 ASU INTERFACE BOARD

The ALS v2 ASU interface board (ALS-060) has the same functionality as the original ASU interface described in Reference 1, Sections 2.3.2, 2.6.3, 2.6.4, 3.2, 3.4, 3.5, and 5.3.3. It was enhanced to provide an extension of the chassis power and TAB connections for the v2 chassis when chassis are mounted close together vertically. These connections are normally at the bottom of the chassis, but this can be cumbersome when v2 chassis are vertically racked. Using these connections in the front of the ALS-060 in lieu of at the bottom of the chassis will remove these obstacles for vertical racking of the chassis. However, when the bottom connectors are not accessible, it's not possible to extend the ALS bus (RAB and TAB) extension chassis described in Section 3.1.

3.3 ALS V2 24V POWER SUPPLY SYSTEM

The 24Vdc power system feeds power to the ALS boards via redundant power internal circuits. The 24Vdc feeds are diode auctioneered and down converted on the ALS board to the voltage domains needed for its logic circuitry. The ALS board uses +3.3Vdc as its general power supply, as well as the source for other additional supporting power supplies.

The 24Vdc power entry circuit into an ALS board is shown on Figure 3-4. The auctioneered redundant 24Vdc supplies are fuse protected immediately after entering the board. A 3A fuse is provided on the 24Vdc power feed to protect the board and chassis power feed from a dead short condition. To support hot swap capability, a current limit function is provided that automatically turns off the board if it draws more than 500mA for more than approximately 100ms.

Figure 3-4: ALS v2 Board - 24Vdc Power Entry Circuit

a,c

The ALS v2 board power budget is based on the manufacturer's specifications and on experiences gained from earlier prototypes of the ALS boards that used a similar FPGA running at the same clock frequency.

The 24Vdc input power is down converted using DC/DC converters or low-drop out regulators to the following voltages:

- 3.3Vdc (Main): The core power supply, FPGA I/O power supply, base board auxiliary circuits, and daughter card auxiliary power.
- +/- 24Vdc: Used to power auxiliary and/or I/O circuits on the base board.

3.3.1 +3.3Vdc Power Supply

The ALS v2 board power supply circuit is based on a DC/DC module. [

]a,c

Figure 3-5: LC Filter to Reduce Conducted Emissions

a,c

The efficiency of the power supply is specified to 89.5% with a 30mA quiescent current. Based on the +3.3Vdc power budget, the expected worst-case current drawn from the 24Vdc supply is 4.6W. [

]a,c

The FPGA core voltage domain(s), which are dependent on the specific daughter card type, is regulated from the +3.3V supply and can deliver the current necessary for worst-case FPGA power consumption.

The ALS v2 daughter cards are equipped with voltage supervisors used to reset the FPGA logic. [

]a,c

3.4 CORE LOGIC AND I/O BOARDS

Figure 3-6 shows the common board layout for the ALS-152 CLB and the v2 I/O boards listed in Table 2-1. The form factor and the accommodation of a daughter card (to address platform diversity) are the major changes to these boards. The fast ALS bus and J5 connector is only on the CLB for a future use (see Figure 2.1-2 and Figure 3-6). The J6 DC IO is the daughter card I/O connector. J7 DC power is the daughter card power and ground connector (see Section 3.5). The J1 ALS bus is the connector for the RAB and TAB (Reference 1, Section 2.3).

The descriptions for the CLB and I/O boards in Reference 1, Section 2.2 still apply (see Table 5-1 in this document).

Figure 3-6: Typical ALS Board Layout

a,c

3.5 ALS V2 DAUGHTER CARDS

The daughter card is one of the major enhancements for the ALS v2 that did not exist in the original ALS platform. It contains the logic for the CLB and I/O boards. By utilizing different daughter cards in the same ALS v2 base board, the ALS v2 can provide equipment and logic diversity for the same base board. For instance, the CLB ALS-152 can have three different versions, each having a unique FPGA using different daughter cards (ALS-850, ALS-852, and ALS-853 as described in Section 2.3).

The configuration drawing for the ALS v2 board has designated group numbers according to the daughter card it uses. [

]^{a,c}

The daughter card interface to the CLB and I/O boards is comprised of two connectors. [

]^{a,c}

Figure 3-7: ALS-152 Base Board with Daughter Card Interface

a,c

The ALS-850 daughter card general layout is shown in Figure 3-8.

Figure 3-8: ALS-850 Daughter Card General Layout

a,c

[

]a,c

The NVM on the ALS and ALS v2 boards stores internal settings to select the specific functional options available for a particular board (refer to Reference 1, Section 2.1.5.2). The ALS v2 board NVM is used to configure channels and operation of the circuitry on the base board; the daughter card implementation does not affect the contents of the NVM. Therefore, there is one unique NVM image for the base board (CLB and I/O) that is used for all daughter card versions. For example, the ALS-352 base board with ALS-850 daughter card uses the same NVM image as the ALS-352 base board with ALS-852 daughter card.

3.5.1 FPGA Hardware

Section 2.3 defines the unique FPGA for each daughter card. The following sections will describe the unique characteristics of each FPGA for each daughter card. The descriptions provide an overview of the diverse nature of the FPGAs.

The following is a summary of the three FPGAs.

- ALS-850, [ ]^{a,c} FPGA Daughter Card
  [

  ]^{a,c}

- ALS-852, [ ]^{a,c} FPGA Daughter Card
  [

  ]^{a,c}

- ALS-853, [ ]^{a,c} FPGA Daughter Card
  [

  ]^{a,c}

The three FPGAs use different technologies, and they are implemented on different process technologies. An FPGA production line is built to manufacture a single process technology. Therefore, the three FPGAs will be manufactured on different production lines. The use of different production lines reduces the chance of two FPGA types being affected by the same production defect.

There are two main elements which make an FPGA unique. These are the internal building blocks and the routing resources. The internal building blocks are the elements that are configured to provide the logic, and routing resources that provide the connections between the internal building blocks. Since the FPGAs use LUTs with different numbers of inputs, the logic will be implemented differently in the FPGAs.

3.5.2 Development Tools

Utilizing different FPGA daughter cards invokes a level of tool diversity in the development of the images for the ALS v2 board.

3.5.2.1 FPGA Development Tools

Different development tools are used for each of the FPGA designs.

The following tools are used:
[

]a,c

These tools use the register transfer language (RTL) and their libraries to perform the synthesis, and place and route steps of the design process. A subset of the tools is used, and only the features of the tool that are necessary to perform these steps are used.

At each step in the process, an independent third-party tool, [ ]a,c is used to verify equivalence, and demonstrate that no logic errors were introduced by the design tool. This independent verification [ ]a,c is in addition to FPGA simulation and system level testing.

Figure 3-9 shows the tools that are used for a specific daughter card. Using diverse tools and the independent third-party verification tool, [ ]a,c provides confidence that the same FPGA application using different daughter cards will not include a common latent design error that has been introduced by the tools used for design and implementation. [

]a,c

Figure 3-9: Daughter Card Tools

a,c

An ALS v2 system design tools document will describe in more detail the tools used for the design and implementation of the FPGA application for each card used in the ALS v2 system.

3.5.2.2 Simulation Tools

Simulation is used to verify RTL functionality by identifying and solving design problems before creating the FPGA image. During the RTL development, a design engineer uses the simulator to verify functionality by monitoring clocks, pulses, state transitions, and other internal RTL signals.

Personnel independent of the FPGA design will use the simulation tool to test the FPGA design. Personnel independent of the FPGA design will meet the independence criteria of 10 CFR 50 Appendix B, Criterion III for independent checking process. An organizational independent verification and validation team will verify that the simulation test plan, test procedure(s), and test reports are adequate and complete. WCAP-18780-P (Reference 5) describes the ALS v2 design process, including testing, and references WNA-PV-00129-GEN (Reference 6).

3.5.3 Architecture Example with Daughter Card Implementation

An example of a basic architecture for a three-division level 1 reactor protection system (RPS) is shown in Figure 3-10. The system is divided into three safety divisions. Each safety division is independent from

the other safety divisions and each safety division provides the necessary inputs to the two-out-of-three (2oo3) hardware voting module to provide required protection of the facility.

Figure 3-10: Simplified Level 1 Three-Division RPS with 2oo3 Voting

a,c

The simplified Level 1 RPS is comprised of three safety divisions that read field-mounted sensors and provide logic on/off signals to the voting logic. In addition, the safety division provides analog outputs to operate main control board indicators, analog outputs for other ALS v2 subsystems in the safety division, and digital outputs for alarms and status indications.

Each safety division is separate and maintains electrical and signal isolation between safety divisions. Each safety division is implemented in a diverse manner by utilizing a different daughter card on all ALS v2 boards in that division for equipment and logic diversity. This attribute is shown with the color coding in Figure 3-10.

3.6 ALS TEST AND CALIBRATION TOOL

This section describes the use of the ALS test and calibration tool (ATCT). Although the ATCT has been used for the ALS and this same tool is used for ALS v2, Reference 1 did not describe the use of the tool as part of the development process. The ATCT is a tool developed by Westinghouse to configure and test the

ALS and now ALS v2 boards. It is used for programing the NVM for each multifunctional board to give it the unique characteristics for performing its specific function for the application.

For example, the ALS-361 board can process both TC and RTD inputs. The ATCT configures the ALS-361 for the specific function for a given channel on the board. The ATCT software is categorized as General Purpose software in accordance with WCAP-18780-P (Reference 5). Once the boards are configured for an application, the ALS v2 boards go through various levels of testing up to a system integration test as described in Reference 5.

The ATCT communicates with the ALS boards via the TAB. The ATCT can query an ALS board for a set of information that is used for status accounting of the board. The configuration data can be retrieved from both the FPGA and NVM (notated by NVM and FPGA below). The configuration data is retrieved from registers within the FPGA image. The following information can be obtained from an ALS board:
[

]^{a,c}

To support ALS v2, the ATCT is updated to allow the following information to be obtained from the new v2 boards:
[

]^{a,c}

The ATCT allows the user to test output channels on a board, including communication channels and the front panel light emitting diodes (LEDs).

The ATCT is used to configure each channel on the ALS-152. The ALS-152 is comprised of six digital input channels, four digital output channels, and two serial data link channels. ALS-152 digital input channel configuration is identical to the ALS-352 channel configuration described below. ALS-152 digital

output channel configuration is identical to the ALS-452 channel configuration described below. ALS-152 communication channel configuration is identical to the ALS-651 channel configuration described below, with the exception that ALS-152 communication channels are unidirectional (Tx only) by hardware design, and they do not have the option to be configured for Rx mode.

For each channel of the ALS-352, the ATCT configures if the channel is enabled or disabled, channel debounce filter timing, and if the channel operates in normally open or normally closed mode.

For each channel of the ALS-361, the ATCT configures the channel for thermocouple type E, J, K, N, R, S, T, or RTD-type three-wire or four-wire operating mode. For each channel, the ATCT configures the board for the gain, offset, coefficients for a three-stage digital filter, and the analog-to-digital conversion (ADC) zero and full scale for converting the field signal into engineering units. For RTDs it specifies the A, B, C RTD coefficients for a three- or four-wire RTD as well as the minimum and maximum range.

For each channel of the ALS-371, the ATCT configures the board for the type of input (voltage or current loop), the range (e.g., 0-5V, 4-20mA), and coefficients for a three-stage digital filter.

For each channel of the ALS-452, the ATCT configures if the channel is enabled or disabled, the failure mode of the channel (i.e., fail as-is, fail asserted, fail de-asserted), and if the channel continuity test is enabled or disabled.

For each channel of the ALS-471, the ATCT configures the board for the type of output (voltage or current loop) for each channel, the range, and the gain and offset for conversion from engineering units to electrical values. If required, the ATCT also configures the channel output value if a board failure is detected.

For the ALS-651, the ATCT enables and disables specific communication channels, and specifies protocol parameters (e.g., baud rate, parity type, number of stop bits). As described in Reference 1, Section 2.2.8, each ALS-651 channel is unidirectional, so the ATCT configures the direction of communication for each channel.

Once the ALS v2 boards have been configured, the ALS v2 safety system will undergo system integration testing to verify that the boards are configured correctly. If the ATCT is used to configure boards for spare parts, then the ALS v2 board undergoes a functional test to confirm that the board is configured correctly before supplying the spare part to a licensee.

4 REUSABLE LOGIC ELEMENTS (RLETS)

The ALS v2 platform expands upon the concept of common FPGA circuit modules by implementing RLETs (see Section 2.4). The intent is that an RLET is defined, developed, verified, and validated one time, then reused for multiple applications. Each RLET follows a standard design that originates with definition of RLET requirements. The RLET design document follows from the requirements. RLET RTL is written based on the design document, and the RTL is verified and validated one time. The RLET RTL is then utilized in a design. The intent is to build a library of verified and validated RLETs that are used throughout the ALS v2 application design.

RLET RTL is created in accordance with the ALS v2 quality and security development procedures. The RTL is placed under configuration control with a Software Release Record documenting:
[

]a,c

Formal design simulation and requirements-based testing is performed utilizing test plans, test procedures, and test cases to validate each RLET, which are traceable back to the requirements and design specifications respectively. The independent verification and validation (IV&V) team reviews the test plans, test procedures, test cases, and test reports as well as traceability to the RLET design and requirements. The IV&V team documents the results of their review. This is the same process that is used to develop RTL for an ALS v2 application.

The FPGA application engineer accesses the configuration management system hosting the verified and validated RLETs on the secure development environment. The engineer acquires a copy of the verified and validated RTL for the RLET and instantiates the source code into the FPGA application source code. The RLET then becomes part of the FPGA application when it is synthesized as shown in Figure 3-9. The software release record for the FPGA application will include the RLETs and their versions used in the application for traceability back to their verification and validation documentation.

5 ORIGINAL ALS TOPICAL REPORT REFERENCE TABLE

The purpose of this section is to provide a reference to each section of the original ALS Topical Report (Reference 1) to clearly identify which sections still apply to ALS v2 and to annotate any differences. As noted in Table 5-1, "no change" indicates the section, in its entirety, as written in the original ALS topical applies to the ALS v2. Table 5-2 is a supporting table to Table 5-1 (refer to Reference 1, Section 12.7.1)

Table 5-1: Reference Table to Original ALS Topical Report

Original ALS Topical Report Section #	Section Title	ALS v2 difference from the original ALS Topical Report (Reference 1)
1	Introduction	ALS v2 is developed by Westinghouse. The scope is the ALS v2 boards listed in Table 2-1. The ALS v2 is being developed concurrent with the submittal of this topical report.
2.1	ALS Platform Overview	The ALS internal bus system architecture allows for up to 60 boards to be connected in up to four different locally connected chassis (one main chassis and three expansion chassis connected within the same cabinet). The external power supplies ensure a stable ALS chassis voltage of 24V. Chassis figures are replaced with figures in this topical report.
2.1.1	ALS Boards	The board nomenclature is now what is defined in Table 2-1. The Generic ALS Platform Architecture Overview still applies for a single 16-slot backplane configuration (except for the board nomenclatures).
2.1.2	Generic ALS Core Logic Boards (ALS-1xx)	The nomenclature is changed to ALS-152.
2.1.3	Generic ALS Input Boards (ALS-3xx)	No change.
2.1.4	Generic ALS Output Boards (ALS-4xx)	No change.

Original ALS Topical Report Section #	Section Title	ALS v2 difference from the original ALS Topical Report (Reference 1)
2.1.5	Common Components/Design	Figure 3-6 replaces the generic ALS board figure to facilitate real estate for the daughter card. Note the field connector is moved to the front of the board. The logic circuit is now the daughter card, and the NVM is located on the daughter card.
2.1.5.1	Logic Circuits/FPGA	The logic circuits and FPGA are now located on the interchangeable daughter card. The ALS-850, [ ]^{a,c} daughter card, and the ALS-852 [ ]^{a,c} daughter card [ ]^{a,c}. The ALS-853, [ ]^{a,c} daughter card is [ ]^{a,c}.
2.1.5.2	Non-Volatile Memory Device	No change.
2.1.5.3	Power Supply	The ALS v2 boards are designed for 24V not 48V.
2.1.5.4	ALS Bus	No change.
2.1.5.5	Front Panel and LED	6002-00011 is replaced with 6003-00011, which discusses the LEDs on the front panel.
2.1.5.6	Back Panel Connectors	J3 is moved to the front of the board.
2.1.5.7	Channel Circuits	No change.
2.2	Standard ALS Boards	No change.
2.2.1	ALS-102 Core Logic Board	Nomenclature is ALS-152 for ALS v2. The daughter card now has the NVM device. The figure is replaced by Figure 3-6 to show real estate for the daughter card.
2.2.1.1	ALS-102 Input Channels	No change.
2.2.1.2	ALS-102 Output Channels	No change.

Original ALS Topical Report Section #	Section Title	ALS v2 difference from the original ALS Topical Report (Reference 1)
2.2.1.3	ALS-102 Communication Channels	No change.
2.2.2	ALS-302 Digital Input Board (48Vdc Contact Inputs)	Nomenclature is ALS-352 for ALS v2. Reference to ALS-102 is now ALS-152. The daughter card now has the NVM device. The figure is replaced by Figure 3-6 to show real estate for the daughter card.
2.2.2.1	Channel Configuration Options	No change.
2.2.3	ALS-311 Analog Input Board (RTD/Thermocouple)	Nomenclature is ALS-361 for ALS v2. The daughter card now has the NVM device. Figure 2.2-3 in Reference 1 is replaced by Figure 3-6 to show real estate for the daughter card.
2.2.3.1	Channel Configuration Options	No change.
2.2.4	ALS-321 Analog Input Board (Voltage/Current)	Nomenclature is ALS-371 for ALS v2. The daughter card now has the NVM device. Figure 2.2-7 in Reference 1 is replaced by Figure 3-6 to show real estate for the daughter card.
2.2.4.1	Channel Configuration Options	No change.
2.2.5	ALS-402 Digital Output Board (Contact Output)	Nomenclature is ALS-452 for ALS v2. The daughter card now has the NVM device. Figure 2.2-5 in Reference 1 is replaced by Figure 3-6 to show real estate for the daughter card.
2.2.5.1	Channel Configuration Options	No change.
2.2.6	“Deleted”	Not applicable.
2.2.7	ALS-421 Analog Output Board	Nomenclature is ALS-471 for ALS v2. The daughter card now has the NVM device. The figure is replaced by Figure 3-6 to show real estate for the daughter card.

Original ALS Topical Report Section #	Section Title	ALS v2 difference from the original ALS Topical Report (Reference 1)
2.2.7.1	Channel Configuration Options	No change.
2.2.8	ALS-601 Communication Board	Nomenclature is ALS-651 for ALS v2. The daughter card now has the NVM device. Figure 2.2-11 in Reference 1 is replaced by Figure 3-6 to show real estate for the daughter card.
2.2.8.1	Channel Configuration Options	Nomenclature is ALS-651 for ALS v2.
2.3	ALS Internal Communications	Nomenclature is ALS v2. Figure 2.3-1 in Reference 1 depicts dual-redundant +48V power supply input. This is changed to +24V for ALS v2.
2.3.1	Reliable ALS Bus (RAB)	Reference to CS Innovations is now Westinghouse.
2.3.2	Test ALS Bus (TAB)	Reference to CS Innovations is now Westinghouse. Reference to ALS-102 is now ALS-152.
2.3.3	ALS Bus Failure Detection and Mitigation	No change.
2.3.3.1	ALS Bus Failure Detection	No change.
2.3.3.2	ALS Bus Failure Mitigation	No change.
2.3.4	ALS Internal Communication Acceptance	No change.
2.4	Board Operation Modes	No change.
2.5	ALS Chassis	The Reference 1 typical example and Figure 2.1-1 are replaced by Sections 2.1 and 3.1 with the accompanying Figure 2-1, Figure 3-1, and Figure 3-2.

Original ALS Topical Report Section #	Section Title	ALS v2 difference from the original ALS Topical Report (Reference 1)
2.5.1	Chassis Mechanics	The ALS v2 chassis is 284.0mm (11.18") deep. Instead of a chassis earthing lug, the ALS v2 chassis is electrically connected and attached to a cabinet center plane that is electrically connected to earth ground. Except for card connections, which are in the front, all other chassis cabling is at the bottom of the ALS chassis using industrial grade plug connectors. The power connector in the front of the ASU interface board can be used in lieu of the power connector at the bottom of the chassis.
2.5.2	ALS Slot and Card Configuration	The front faceplate used for the ALS v2 boards are 5HP wide, 2.5mm (0.098 inch) thick plate. All ALS v2 chassis slots can be used for any ALS v2 board. The ASU interface board must use the first slot, but the first ALS v2 chassis slot can accept any other board type as well. The ALS v2 application logic (CLB) verifies the correct installation of daughter card types within a chassis.
2.5.3	ALS Boards	Figure 2.5-2 in Reference 1 is replaced by Figure 3-6.
2.5.4	ALS Front Plate	Figure 2.5-2 in Reference 1 would use the v2 board nomenclature.
2.5.5	Board Latches	No change.
2.5.6	Front Panel LEDs	No change.
2.5.6.1	Board Indication	No change.
2.5.6.2	Channel Indication	No change.

Original ALS Topical Report Section #	Section Title	ALS v2 difference from the original ALS Topical Report (Reference 1)
2.5.7	ALS Backpanel Assembly	The backpanel assembly is no longer application specific. The same backpanel assembly can be used for any application. Field terminations are now at the front of the individual ALS v2 boards instead of at the back of the chassis. [ ]^{a,c} The connectors used by the ALS v2 platform are D-sub style connectors. The D-sub connectors have a current carrying capability equal to or greater than the maximum channel current. Figure 2.5-4 and 2.5-5 in Reference 1 are no longer applicable. There is no "earthing connection" on the chassis (see Section 2.5.1 in this table). There are no connectors on the backplate. All field connections are at the front of the ALS v2 boards.
2.5.8	Expansion Chassis	The cable between the ALS v2 chassis will contain +24Vdc and ground.
2.6	Cabinet and Peripherals	Since the ALS v2 chassis in not application specific, it is no longer necessary to include in the list.
2.6.1	Cabinet	No change.
2.6.2	Power Supply and Distribution	The ALS chassis is powered via the power connector at the bottom of the ALS v2 chassis. The output of the redundant cabinet power supplies to the ALS v2 chassis is 24 Vdc.
2.6.3	ALS Service Unit (ASU)	Citation to the ALS Platform Specification is now 6003-00011. System and board information will be coming from the ALS v2 daughter cards. Calibration data, like setpoints, are saved on the CLB daughter card.

Original ALS Topical Report Section #	Section Title	ALS v2 difference from the original ALS Topical Report (Reference 1)
2.6.4	Control Panel	No change.
2.6.5	Assembly Panel	No change.
2.7	Response Time	References to ALS board numbers is replaced with the corresponding ALS v2 boards listed in Table 2-1.
2.8	ALS System Accuracy	The nomenclature for the v2 analog output board is ALS-471.
2.9	Human Factors Considerations	No change.
3	Diagnostics and Maintenance	No change.
3.1	ALS Diagnostics and Fault Indications	No change.
3.1.1	ALS Platform Diagnostics	No change.
3.1.1.1	System Self-Diagnostics	No change.
3.1.1.2	ALS Platform Self-Testing	References to ALS board numbers is replaced with the corresponding ALS v2 boards listed in Table 2-1.
3.1.1.3	System Self-Diagnostics	No change.
3.1.2	Application Diagnostics	No change.
3.1.3	Preferred Failure Mode for Abnormal and Unexpected Inputs	No change.
3.1.4	ALS Alarm Reset	No change.
3.2	ALS Platform Maintenance Features	No change.

Original ALS Topical Report Section #	Section Title	ALS v2 difference from the original ALS Topical Report (Reference 1)
3.3	Maintenance Terminology	No change.
3.4	Calibration of ALS Input and Output Boards	No change.
3.5	Test of Digital Output Boards	References to ALS board numbers is replaced with the corresponding ALS v2 boards listed in Table 2-1.
3.6	Maintenance of Set Points	No change.
4	Equipment Qualification	The ALS v2 Equipment Qualification (EQ) documentation is or will be as follows: • ALS v2 EQ Plan is 6003-00004 (Reference 8) • ALS v2 EQ Summary Report (6003-00200) • ALS v2 Application Guidance (6003-00008)
4.1 4.1.1	Environmental Qualification	The ALS v2 EQ Plan (Reference 8) supersedes this section of Reference 1.
4.2 4.2.1 – 4.2.4	Seismic	The ALS v2 EQ Plan (Reference 8) supersedes this section of Reference 1.
4.3 4.3.1 – 4.3.4	Electromagnetic Compatibility (EMC) Testing	The ALS v2 EQ Plan (Reference 8) supersedes this section of Reference 1.
5	ALS Platform Communications	No change.
5.1	Intra-Divisional Communication	The nomenclature for the ALS v2 communication board is ALS-651.

Original ALS Topical Report Section #	Section Title	ALS v2 difference from the original ALS Topical Report (Reference 1)
5.2	Inter-Divisional Safety-to-Safety Communication	The nomenclature for the ALS v2 communication board is ALS-651 and the CLB is ALS-152.
5.3	Inter-Divisional Safety-to-Non-Safety Communication	The nomenclature for the ALS v2 communication board is ALS-651.
5.3.1	Broadcasting Information to Non-Safety Devices using ALS-601	The nomenclature for the ALS v2 communication board is ALS-651 and the CLB is ALS-152.
5.3.2	Broadcasting Information to Non-Safety Devices using TxB Busses	References to ALS board numbers is replaced with the corresponding ALS v2 boards listed in Table 2-1.
5.3.3	Communication with Non-Safety Devices using the TAB Bus	No change.
5.4	Multidivisional Control, Display and Management	No change.
5.4.1	Multidivisional Control in Multiple Safety Divisions	The nomenclature for the ALS v2 communication board is ALS-651 and the CLB is ALS-152.
5.4.1.1	Multidivisional Maintenance in Multiple Safety Divisions	The nomenclature for the ALS v2 communication board is ALS-651 and the CLB is ALS-152. Reference to CSI is now Westinghouse.
6	Life Cycle Management Process	No change.
6.1 6.1.1 – 6.1.5	Development Process	The description in Reference 1 is superseded by WCAP-18780-P (Reference 5).
6.2	Life Cycle Planning Documentation	No change.
6.3	Verification and Validation	No change.

Original ALS Topical Report Section #	Section Title	ALS v2 difference from the original ALS Topical Report (Reference 1)
6.3.1	Field Programmable Gate Array V&V	Test independence at this level is as required by 10 CFR 50 Appendix B, "The verifying or checking process shall be performed by individuals or groups other than those who performed the original design, but who may be from the same organization."
6.3.2	Board V&V	Test independence at this level is as required by 10 CFR 50 Appendix B, "The verifying or checking process shall be performed by individuals or groups other than those who performed the original design, but who may be from the same organization."
6.3.3	System V&V	No change.
7	Reliability	Reference 1 states, "The concern for software common mode failures is mitigated by incorporating inherent ALS platform diversity using diversely configured FPGAs." ALS v2 uses diverse FPGAs in addition to diversely configured FPGAs.
7.1	Failure Modes and Effects Analysis (FMEA)	No change.
7.2	Reliability and Availability	No change.
8	Security	No change.
8.1	ALS Platform Security Overview	The same ALS Security Plan, 6002-00006 (Reference 9) is used for the ALS v2 development but updated to reflect Westinghouse security controls. In lieu of the CS Innovations isolated development infrastructure (IDI), the Westinghouse IDI will be used.

Original ALS Topical Report Section #	Section Title	ALS v2 difference from the original ALS Topical Report (Reference 1)
8.2	Life Cycle Security	No change.
8.2.1	Planning Activity	No change.
8.2.2	Development and Manufacturing Activities	Class 1E storage is now under the control of Westinghouse.
8.2.3	System Test, Installation, and Maintenance Activities	Control is now under Westinghouse.
8.3	ALS Platform Security Methods and Features	No change.
9	Diversity	The two levels of diversity for ALS v2 are 1) core diversity and 2) equipment diversity as described in Section 2.3 and Section 3.5.
9.1	Implementation of Diversity to Address Common Cause Failure	For core diversity, the IV&V teams will review the testing conducted by the design team. Test independence at this level is as required by 10 CFR 50 Appendix B, “The verifying or checking process shall be performed by individuals or groups other than those who performed the original design, but who may be from the same organization.” The second level of diversity description, embedded design diversity, is superseded by the use of diverse daughter cards for the same ALS v2 Board as described in Section 2.3 and Section 3.5.
9.2	NUREG/CR-6303 Diversity Evaluation	The ALS Diversity Analysis, 6002-00031 will be replaced with the ALS v2 Diversity Analysis, 6003-00031.
9.3	Typical Applications of Diversity	No change.

Original ALS Topical Report Section #	Section Title	ALS v2 difference from the original ALS Topical Report (Reference 1)
9.3.1	Diversity within the ALS FPGA	There is no Team A or Team B for ALS v2. Human diversity is implicit by using different FPGAs in the daughter cards (refer to Reference 7, page 41). Also, equipment diversity (i.e., FPGA technology diversity) is sufficient to ensure the system safety function is performed in the presence of a postulated software CCF that is limited to a single FPGA technology (refer to Reference 7, page 43).
9.3.2	Diversity between Chassis	Embedded design diversity is the use of diverse daughter cards for an ALS v2 board. There is no Team A or Team B implementing the same requirements. Human diversity is implicit by using different FPGAs in the daughter cards. There is no longer an A and B version of an ALS board. Instead, there are group designations for each ALS v2 board where each group has a different daughter card configuration for the board (see Section 3.5). Figure 9.3-2 in Reference 1 is superseded by Figure 3-10.
9.3.3	Diversity within Separation Groups	Embedded design diversity is the use of diverse daughter cards for an ALS v2 board. There is no Team A or Team B implementing the same requirements. Human diversity is implicit by using different FPGAs in the daughter cards. There is no longer an A and B version of an ALS board. Instead, there are group designations for each ALS v2 board where each group has a different daughter card configuration for the board (see Section 3.5). Figure 9.3-3 in Reference 1 is superseded by Figure 3-10.
10	Quality Assurance	CS Innovations is now Westinghouse except for historical information described in this section. Work on ALS v2 is governed by the Westinghouse Quality Management System.

Original ALS Topical Report Section #	Section Title	ALS v2 difference from the original ALS Topical Report (Reference 1)
11	Training	References to CS Innovations and CSI are now Westinghouse for the ALS v2. All training and quality records are maintained at Westinghouse. The ALS v2 Project Plan (Reference 10) describes the required training for the ALS v2 development.
12	Regulatory Compliance	No change.
12.1	Review of ALS Platform Compliance to IEEE-603 Requirements	No change.
12.1.1	IEEE 603-1991 Clause 4 – Safety System Designation	No change.
12.1.2	IEEE 603-1991 Clause 5.1 – Single-Failure Criterion	No change.
12.1.3	IEEE 603-1991 Clause 5.2 – Completion of Protective Action	No change.
12.1.4	IEEE 603-1991 Clause 5.3 – Quality	Instead of the CS Innovations QA program (Section 10) the Westinghouse Quality Management System governs the work for ALS v2. Although many of the same processes are used by Westinghouse, the cited Wolf Creek audit of CS Innovations nor the Westinghouse audit of CS Innovations is relevant to the development of ALS v2 under the Westinghouse Quality Management System.
12.1.5	IEEE 603-1991 Clause 5.4 – Equipment Qualification	See Section 4 in this table and the ALS v2 EQ Plan (Reference 8) for the codes and standards that are invoked for the ALS v2 Equipment Qualification.
12.1.6	IEEE 603-1991 Clause 5.5 – System Integrity	No change.

Original ALS Topical Report Section #	Section Title	ALS v2 difference from the original ALS Topical Report (Reference 1)
12.1.7	IEEE 603-1991 Clause 5.6 – Independence	Refer to the ALS v2 EQ Plan (Reference 8) for the relevant codes and standards.
12.1.7.1	IEEE 603-1991 Clause 5.6.1 – Independence between Redundant Portions of a Safety System	No change.
12.1.7.2	IEEE 603-1991 Clause 5.6.2 – Independence between Safety Systems and Effects of Design Basis Event	No change.
12.1.7.3	IEEE 603-1991 Clause 5.6.3 – Independence between Safety Systems and Other Systems	In addition to an ASU connector located on a control panel, the new ASU interface and power interconnection board for the ALS v2 platform can be used. This board is a hardware-based extension of the chassis power and TAB connections and can be used in applications where the chassis bottom side power and TAB connectors are not accessible due to cabinet space constraints (see Section 3.2).
12.1.8	IEEE 603-1991 Clause 5.7 – Capability for Test and Calibration	[ ]^{a,c}
12.1.9	IEEE 603-1991 Clause 5.8 – Information Displays	No change.
12.1.9.1	IEEE 603-1991 Clause 5.8.1 – Displays for Manually Controlled Actions	Reference to ALS-421, ALS-402, ALS-601, and ALS-102 are replaced by ALS-471, ALS-452, ALS-651, and ALS-152 respectively.
12.1.9.2	IEEE 603-1991 Clause 5.8.2 – System Status Indication	The ALS v2 Platform Specification 6003-00011 (Reference 11) replaces Reference 5 in the original ALS Topical Report (Reference 1).
12.1.9.3	IEEE 603-1991 Clause 5.8.3 – Indication of Bypasses	The board channel bypass LED is not red, but it is blinking as stated.

Original ALS Topical Report Section #	Section Title	ALS v2 difference from the original ALS Topical Report (Reference 1)
12.1.9.4	IEEE 603-1991 Clause 5.8.4 – Location	No change.
12.1.10	IEEE 603-1991 Clause 5.9 – Control of Access	Reference to the CS Innovations and its quality assurance program is replaced with Westinghouse Electric Company LLC and its Quality Management System.
12.1.11	IEEE 603-1991 Clause 5.10 – Repair	No change.
12.1.12	IEEE 603-1991 Clause 5.11 – Identification	No change.
12.1.13	IEEE 603-1991 Clause 5.11 – Identification	No change.
12.1.14	IEEE 603-1991 Clause 5.13 – Multi-Unit Stations	No change.
12.1.15	IEEE 603-1991 Clause 5.14 – Human Factor Considerations	No change.
12.1.16	IEEE 603-1991 Clause 5.15 – Reliability	Reference to ALS-321 is replaced with ALS-371. Mean time between failures (MTBF) calculations for the ALS v2 will not be performed by an independent second party. Westinghouse will perform the reliability analysis. A later version of 217PLUS™ will be used.
12.1.17	IEEE 603-1991 Clause 6.1 – Automatic Control	No change.
12.1.18	IEEE 603-1991 Clause 6.2 – Manual Control	Reference to ALS-302 and ALS-421 are replaced with ALS-352 and ALS-471 respectively.

Original ALS Topical Report Section #	Section Title	ALS v2 difference from the original ALS Topical Report (Reference 1)
12.1.19	IEEE 603-1991 Clause 6.3 – Interaction between Sense of Command Features and Other Systems	No change.
12.1.20	IEEE 603-1991 Clause 6.4 – Derivation of System Inputs	No change.
12.1.21	IEEE 603-1991 Clause 6.5 – Capability for Testing and Calibration	Reference to the ALS-421 is replaced by the ALS-471.
12.1.22	IEEE 603-1991 Clause 6.6 – Operating Bypass	No change.
12.1.23	IEEE 603-1991 Clause 6.7 – Maintenance Bypass	No change.
12.1.24	IEEE 603-1991 Clause 6.8 – Setpoints	No change.
12.1.25	IEEE 603-1991 Clause 7.1 – Automatic Control	No change.
12.1.26	IEEE 603-1991 Clause 7.2 – Manual Control	No change.
12.1.27	IEEE 603-1991 Clause 7.3 – Completion of Protective Action	No change.
12.1.28	IEEE 603-1991 Clause 7.4 – Operating Bypasses	No change.
12.1.29	IEEE 603-1991 Clause 7.5 – Maintenance Bypass	No change.

Original ALS Topical Report Section #	Section Title	ALS v2 difference from the original ALS Topical Report (Reference 1)
12.1.30	IEEE 603-1991 Clause 8 – Power Source Requirements	ALS v2 cabinet power can be supplied with two [ ]^{a,c} auctioneered supplies to avoid the cabinet power being a source of CCF.
12.2	IEEE-7-4.3.2 Compliance	No change.
12.2.1	IEEE 7-4.3.2 Clause 4 – Safety System Design Basis	No change.
12.2.2	IEEE 7-4.3.2 Clause 5.1 – Single-Failure Criterion	No change.
12.2.3	IEEE 7-4.3.2 Clause 5.2 – Completion of Protective Action	No change.
12.2.4	IEEE 7-4.3.2 Clause 5.3 – Quality	The CS Innovations QA program is not applied for the ALS v2 boards. The Westinghouse Quality Management System is the 10 CFR 50 Appendix B program that governs ALS v2 safety-related work.
12.2.5	IEEE 7-4.3.2 Clause 5.3.1 – Software Development	The FPGA logic development is described in WCAP-18780-P (Reference 5).
12.2.6	IEEE 7-4.3.2 Clause 5.3.1.1 – Software Quality Metrics	The use of metrics in the FPGA logic development process is described in WCAP-18780-P (Reference 5).
12.2.7	IEEE 7-4.3.2 Clause 5.3.2 – Software Tools	The ALS v2 Design Tools document is 6003-00030. CSI Configuration Management Program is replaced by the Westinghouse Configuration Management Program. See Section 3.5.2.
12.2.8	IEEE 7-4.3.2 Clause 5.3.3 – V&V	WCAP-18780-P (Reference 5) describes the ALS v2 V&V process.
12.2.9	IEEE 7-4.3.2 Clause 5.3.4 – Independent V&V Requirements	WCAP-18780-P (Reference 5) describes the ALS v2 V&V independence.

Original ALS Topical Report Section #	Section Title	ALS v2 difference from the original ALS Topical Report (Reference 1)
12.2.10	IEEE 7-4.3.2 Clause 5.3.5 – Software Configuration Management	The section is replaced by the description for configuration management in WCAP-18780-P (Reference 5).
12.2.11	IEEE 7-4.3.2 Clause 5.3.6 – Software Project Risk Management	Project risk management for ALS v2 projects is described in WCAP-18780-P (Reference 5).
12.2.12	IEEE 7-4.3.2 Clause 5.4 – Equipment Qualification	No change.
12.2.12.1	IEEE 7-4.3.2 Clause 5.4.1 – Computer System Testing	No change.
12.2.12.2	IEEE 7-4.3.2 Clause 5.4.2 – Qualification of Existing Commercial Computers	No change.
12.2.13	IEEE 7-4.3.2 Clause 5.5 – System Integrity	No change.
12.2.13.1	IEEE 7-4.3.2 Clause 5.5.1 – Design for Computer Integrity	No change.
12.2.13.2	IEEE 7-4.3.2 Clause 5.5.2 – Design for Test and Calibration	No change.
12.2.13.3	IEEE 7-4.3.2 Clause 5.5.3 – Fault Detection and Self-Diagnostics	No change.
12.2.14	IEEE 7-4.3.2 Clause 5.6 – Independence	No change.
12.2.15	IEEE 7-4.3.2 Clause 5.7 – Capability for Test and Calibration	No change.
12.2.16	IEEE 7-4.3.2 Clause 5.8 – Information Displays	No change.

Original ALS Topical Report Section #	Section Title	ALS v2 difference from the original ALS Topical Report (Reference 1)
12.2.17	IEEE 7-4.3.2 Clause 5.9 – Control of Access	No change.
12.2.18	IEEE 7-4.3.2 Clause 5.10 – Repair	No change.
12.2.19	IEEE 7-4.3.2 Clause 5.11 – Identification	No change.
12.2.20	IEEE 7-4.3.2 Clause 5.12 – Auxiliary Features	No change.
12.2.21	IEEE 7-4.3.2 Clause 5.13 – Multi-Unit Stations	No change.
12.2.22	IEEE 7-4.3.2 Clause 5.14 – Human Factor Considerations	No change.
12.2.23	IEEE 7-4.3.2 Clause 5.15 – Reliability	No change.
12.2.24	IEEE 7-4.3.2 Clause 6 – Sense and Command Features – functional and design requirements	No change.
12.2.25	IEEE 7-4.3.2 Clause 7 – Execute Features – functional and design requirements	No change.
12.2.26	IEEE 7-4.3.2 Clause 8 – Power Source Requirements	No change.
12.3	DI&C ISG-04 Highly-Integrated Control Rooms – Communications Issues	No change.

Original ALS Topical Report Section #	Section Title	ALS v2 difference from the original ALS Topical Report (Reference 1)
12.4	BTP 7-14, R5, Guidance on Software Reviews for Digital Computer-Based Instrumentation and Control Systems	WCAP-18780-P (Reference 5) describes the development processes relevant to NUREG-0800, Chapter 7, BTP 7-14.
12.5	BTP 7-19, Guidance for Evaluation of Diversity and Defense-in-Depth in Digital Computer-Based Instrumentation and Control Systems and ISG-02, Diversity and Defense-in-Depth Issues	NUREG-0800, Chapter 7, BTP 7-19, Revision 8, encompasses the retired DI&C-ISG-02. ALS v2 embedded design diversity is replaced by diverse FPGA daughter cards for the same ALS v2 board function. This and other diverse attributes of the ALS v2 will be described in the ALS v2 Diversity Analysis, 6003-00031, that allows for crediting internal platform diversity as a means to mitigate a postulated CCF of the safety system (see Section 3.5). This would meet the BTP 7-19 review criteria B.3.1.1.
12.6	RG 1.152, Revision 3 (Draft), Criteria for Use of Computers in Safety Systems of Nuclear Power Plants	RG 1.152 is now a published Revision 3. CSI is replaced with Westinghouse. The same ALS Security Plan, 6002-00006 (Reference 9), is used for ALS v2 development. CSI is now Westinghouse. In addition to the secure operating characteristics listed in this section that also apply to ALS v2, there are no exposed unused ports. All connections to the ALS v2 platform are hooded connectors fastened to the board or chassis.
12.7	ISG-06, Digital Instrumentation and Control (DI&C) Licensing Process	DI&C-ISG-06 Revision 2 is now the governing document for DI&C license amendment requests (LARs). As a result, DI&C-ISG-06 Enclosure B is revised. Westinghouse assumes this NRC review would be a “Tier 2-like” review since the bulk of the original ALS topical report (Reference 1) still applies, and this table explains the “deviations” from the original topical report.

Original ALS Topical Report Section #	Section Title	ALS v2 difference from the original ALS Topical Report (Reference 1)
12.7.1	Topical Report to Standard Review Plan (SRP) Regulation Cross Reference	Table 5-2 lists the replacement ALS v2 document citations to those cited in the SRP Regulation Cross Reference Table in Reference 1. They are listed in order of occurrence in Reference 1, Section 12.7.1. If not listed in Table 5-2, then the same document cited in Reference 1, Section 12.7.1 is used for ALS v2.
Appendix A	Reactor Protection System (RPS) / Engineered Safety Features Actuation System (ESFAS) Application	No change.
A.1	Introduction	No change.
A.2	Functionality	No change.
A.2.1	Level 1 Reactor Project System and Engineered Safety Features Actuation System	Figure A.2-1 shows diversity within a division using Core A and B. This would change for ALS v2 to using daughter cards to achieve diversity within a division for both the CLB and I/O boards. In addition, there are three daughter cards to choose from for diversity vs. only two core designs.
A.2.2	Level 2 Reactor Protection / ESFAS System	Similar to Figure A.2-1, Figure A.2-2 would change to designating different daughter cards vs. core logic (A or Alpha and B or Bravo). There is no Team A and Team B approach. Human diversity is implicit by using different FPGAs in the daughter cards (refer to Reference 7, page 41). Design diversity is achieved by using daughter cards instead (refer to Reference 7, page 43).

Original ALS Topical Report Section #	Section Title	ALS v2 difference from the original ALS Topical Report (Reference 1)
A.2.3	Level 3 Reactor Protection System	Similar to Figures A.2-1 and Figure A.2-2, Figures A.2-3 and A.2-4 would change to designating different daughter cards vs. core logic (A or Alpha and B or Bravo). The DI diversity in the figure would also be accomplished using different daughter cards.
Appendix B	Train Diverse Application	No change.
B.1	Introduction	In lieu of embedded design diversity being achieved by using two independent teams, different daughter cards are used to achieve the same objective. Human diversity is implicit by using different FPGAs in the daughter cards (refer to Reference 7, page 41).
B.2	Typical Example	No change.
B.3	ALS Implementation Block Diagram	Figure B.3-1 changes for ALS v2 include: • Board nomenclatures would change to those listed in Table 2-1. • A and B core logic for all boards would be replaced with different daughter cards to achieve the same diversity objective. • There are not two different design teams. Using different daughter cards achieves the same diversity objective. Human diversity is implicit by using different FPGAs in the daughter cards (see Reference 7, page 41).
Appendix C	Dual Train Application	No change.

Original ALS Topical Report Section #	Section Title	ALS v2 difference from the original ALS Topical Report (Reference 1)
C.1	Introduction	In lieu of Train A logic and Train B logic, different daughter cards would be used to achieve even greater design diversity since this appendix describes using only one design team. Human diversity is implicit by using different FPGAs in the daughter cards (refer to Reference 7, page 41).
C.2	Typical Examples	No change.
C.3	Description of Typical System Functionality	No change.
C.3.1	Thermocouple / Core Cooling Monitor (TC/CCM)	No change.
C.3.2	Post-Accident Monitoring System (PAMS)	No change.
C.3.3	Reactor Vessel Level Indicating System (RVLIS)	No change.
C.4	ALS Implementation Block Diagram	Board nomenclatures would change to those listed in Table 2-1.

The documents in Table 5-2 are listed in order of appearance in the table in Reference 1, Section 12.7.1.

Table 5-2: ALS v2 Documentation to Original SRP Regulation Cross Reference

Documents Cited in Reference 1 Section 12.7.1 (see Table 5-1, 12.7.1)	ALS v2 Replacement Documentation
6002-00000 ALS Management Plan	6003-00000 ALS v2 Management Plan
6002-00001 ALS QA Plan	6003-00001 ALS v2 QA Plan
6002-00003 ALS VV Plan	6003-00003 ALS v2 VV Plan
6002-00004 ALS EQ Plan	6003-00004 ALS v2 EQ Plan
6002-00005 ALS Test Plan	6003-00005 ALS v2 Test Plan
6002-xxx12 FPA FMEA and Reliability Analysis	6003-xxx12 FPA FMEA and Reliability Analysis, where xxx = board type (e.g., CLB ALS-152). See Table 2-1.
6002-00200 – ALS Platform EQ Summary Report	6003-00200 – ALS v2 Platform EQ Summary Report
6002-00031 – ALS Diversity Analysis	6003-00031 – ALS v2 Diversity Analysis
6002-00010 ALS Platform Requirements Specification	6003-00010 ALS v2 Platform Requirements Specification
6002-00011 ALS Platform Design Specification	6003-00011 ALS v2 Platform Design Specification
6002-00500 ALS Platform VV Summary Report	6003-00500 ALS v2 Platform VV Summary Report
6002-xxx01 Requirements Specification	6003-xxx01 ALS v2 Requirements Specification Where xxx = board type (e.g., CLB ALS-**152**). See Table 2-1.
6002-xxx82 VV Summary Report	6003-xxx82 VV Summary Report Where xxx = board type (e.g., CLB ALS-**152**). See Table 2-1.
6002-xxx94 Test Summary Report	6003-xxx94 Test Summary Report Where xxx = board type (e.g., CLB ALS-**152**). See Table 2-1.
6002-00007 ALS Platform Configuration Status Accounting	6003-00007 ALS v2 Platform Configuration Status Accounting
6002-00400 ALS Platform Configuration Management Summary Report	6003-00400 ALS v2 Platform Configuration Management Summary Report
6002-xxx50 Configuration Status Accounting Report	Incorporated into 6003-00007 ALS v2 Platform Configuration Status Accounting
6002-00016 FPGA Core A Common Module Design Specification 6002-00017 ALS FPGA Core B Common Module	6003-00016 FPGA Common Module Design Specification Note: There is no longer Core A and B design

Documents Cited in Reference 1 Section 12.7.1 (see Table 5-1, 12.7.1)	ALS v2 Replacement Documentation
Design Specification	documents now that daughter cards are introduced for design diversity.
6002-00060 ALS Board Manufacturing Procedure	6003-00255 ALS v2 Production Test Plan Note: 6003-00255 replaces 6002-00255 and 6002-00060.
NA 4.50 Electronics Development Procedure	NA 4.48 Component / Sub-assembly Hardware Design Process Note: Westinghouse Quality Procedure NA 4.50 is replaced by NA 4.48
6002-00008 – ALS Application Guidance	6003-00008 – ALS v2 Application Guidance
6002-xxx81 ALS-xxx Configuration Management Summary Report	Incorporated into 6003-00007 ALS v2 Platform Configuration Status Accounting
6002-00018 ALS Platform FPGA VV Test Plan	6003-00018 ALS v2 Platform FPGA VV Test Plan

6 ALS V2 TOPICAL REPORT CHANGE PROCESS

To evaluate changes to the ALS v2 platform for any impact on a future NRC-approved ALS v2 Topical Report, Westinghouse uses a Quality Level 3 Procedure NA 4.54 (Reference 13), which is part of the Westinghouse Quality Management System. The change process defined in NA 4.54 describes methods used to screen and evaluate proposed changes to ALS v2 components, logic, or processes defined within a future NRC-approved ALS v2 Topical Report, including the embedded NRC Safety Evaluation (SE).

This process defines criteria to be used for the determination of whether the safety conclusions of the NRC SE remain valid following the proposed change or if the changes will require submittal to the NRC for evaluation and approval prior to implementation. An example would be the decision by Westinghouse to replace one of the daughter card FPGAs (see Section 2.3 and Section 3.5). The NA 4.54 process would evaluate the FPGA change out and determine if the change invalidates any of the diversity arguments in this topical report and any NRC safety conclusions in the accompanying safety evaluation for the topical report. If the conclusion is that the change does invalidate either, then Westinghouse would not pursue an NRC approval for that change.

An ALS v2 Configuration Status Accounting document is maintained by an ALS v2 Configuration Control Coordinator responsible for maintenance of the configuration status accounting document and for ensuring the minimum requirements of the document are met. Proposed changes to the ALS v2 platform are processed and documented using a Safety System Platform Change Evaluation (SSPCE) Form. This form is used to evaluate the possible impact of changes to a future NRC-approved ALS v2 Topical Report. Specific screening criteria, including criteria that if satisfied would automatically require a licensing submittal for regulatory review and approval prior to implementation of the change, are documented in this form.

7 CONCLUSION

This topical report explains in detail the changes to the original NRC-approved ALS topical report (Reference 1). The four major changes are:

1. Chassis footprint and increased I/O density with no functionality changes.
2. Improved useability changes that now provide a standard backplane that can accommodate two ALS-152 CLBs, with 24V vs. 48V power, and moving platform hardware interfaces to be more accessible.
3. The development of diverse ALS daughter cards that can be connected to an ALS v2 board implementing the same functional requirements but with diverse logic. This is the new "embedded design diversity" replacing the Core A and B diverse design teams used by the original ALS platform.
4. The ability to create RLETs that are verified and validated by an IV&V team that can be reused for both platform and application development.

As delineated in Table 5-1, most of the existing functionality in the original ALS platform is carried forward to ALS v2.