DOOSAN

HF Controls

HFC-FPGA Control System of
HFC-6000 Safety Platform

HFC-FPGA Equipment Qualification Summary Test Report

TR901-302-02 Rev B

Effective Date 5 / 19 / 2020

Prepared By: Yang Lu

Reviewed By: Yin Guo

Approved By: Steve Yang

[ ]

Revision History

Date	Revision	Author	Changes
1/29/2020	A	Yang Lu	Initial release
5/13/2020	B	Yang Lu	Revised per reviewers' comments including correcting CR/Redmine numbers, updating CR status, and generating CR 2020-0093 to track a miss in isolation test execution.

TABLE OF CONTENTS

TABLE OF TABLES

TABLE OF FIGURES

1.0 PURPOSE

This document provides a summary of the Equipment Qualification (EQ) testing performed in accordance with the EQ Test Plans (References 1 and 2) on the HFC-FPGA Control System of HFC-6000 Safety Platform. The HFC-FPGA provides a generic digital safety Instrument and Control (I&C) platform to be used in mild environments as described in the EQ Test Plans.

This document summarizes the EQ test performed, test evaluation and test results required by the U.S. Nuclear Regulatory Commission (NRC) Interim Staff Guide DI&C-ISG-06 (Reference 3), item D.3.

The test results demonstrate that the HFC-FPGA platform perform its intended safety functions without experiencing environmentally induced common-cause failures during normal environmental conditions and anticipated operational occurrences.

2.0 ABBREVIATIONS AND ACRONYMS

AI	Analog Input
AO	Analog Output
BOE	Burst of Events
CR	Condition Report
DI	Digital Input
DO	Digital Output
EFT	Electrical Fast Transient
EMI	Electromagnetic Interference
EPRI	Electric Power Research Institute
EQ	Equipment Qualification
ESD	Electrostatic Discharge
ETL	Environmental Testing Laboratory
F-Link	Communication link between HFC-FPGA controllers and configured HFC-FPU I/O modules
FPGA	Field Programmable Gate Array
G-Link	Communication link between HFC-FPGA controllers and Communication Gateway controllers
HAS	Historical Archiving System
HFC	HF Controls
HPAT	HFC Plant Automated Tester
HSIM	High Speed Interface Module
I&C	Instrumentation and Control
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
I/O	Input / Output
M&TE	Measurement and Test Equipment
MCRT	HFC Graphic Display / Control Interface
NRC	Nuclear Regulatory Commission
NTS	National Technical Systems
OBE	Operating Basis Earthquake
PCB	Printed Circuit Board

QA	Quality Assurance
RIF	Redundancy Interface
RF	Radio Frequency
RFI	RF Interference
RG	Regulatory Guide
RH	Relative Humidity
RRS	Required Response Spectrum
RTD	Resistance Thermal Detector
SOE	Sequence of Events
SSE	Safe Shutdown Earthquake
TSAP	Test Specimen Application Program

3.0 SCOPE OF EQ TESTING

The EQ testing of the HFC-FPGA platform was performed in accordance with the requirements of Regulatory Guide (RG) 1.209 (Reference 4) and requirements of Institute of Electrical and Electronics Engineers (IEEE) Standard 323-2003 (Reference 5). Qualification Test Specimen for the EQ testing was designed to follow the guidance specified in EPRI TR-107330 (Reference 6). Requirements defined in NRC RG 1.180 (Reference 7) were used as the basis for EMI/RFI, ESD, and Surge Withstand qualification tests.

Isolation Test between Class 1E and non-Class 1E equipment was planned in TP901-200-07 Rev. E but testing had not been executed, CR2020-0093 has been generated to track this non-conformance. CR2020-0093 is in the process of being addressed and corrective actions will be taken to perform the Isolation Test.

The HFC-FPGA modules under the EQ testing are listed in Table 1.

Table 1. Qualification Modules

Assembly Part Number	Module Name	Description	BOM Part Number	BOM Revision

The Qualification Test Specimen was designed to function as a representative example of an HFC-FPGA system, containing all modules listed in Table 1 operating as they would in a plant. The Test Specimen Application Program (TSAP) used for the Qualification Test Specimen was developed to follow EPRI TR-107330 to demonstrate capabilities comparable to those that would be required on a plant-specific basis. The qualification process was:

a) The HFC-FPGA modules listed in Table 1 were designed and assembled following HFC's QA program and applicable Work Instructions.

b) The Qualification Test Specimen was designed and assembled using at least one instance of each HFC-FPGA module from Table 1 in a representative configuration. Support equipment was included to interface with the HFC-FPGA modules in a manner comparable to how they would be implemented in a plant setting.

c) The TSAP was defined and developed for HFC-FCPU and HFC-FCPUX modules of the Qualification Test Specimen. This TSAP served as a synthetic application designed to aid in the qualification and operability tests for the test specimen. In place of plant-specific requirements for the application, guidance from EPRI TR-107330 was used for defining the parameters of the TSAP.

d) The HFC-FCPU, HFC-FCPUX, HFC-FPGA I/O modules, and the TSAP were combined into a test configuration for execution of acceptance tests. This activity constitutes the system integration testing for each module included in the Qualification Test Specimen. This assembly was named the VV0115 Test Specimen, and the design is detailed in VV901-300-10 (Reference 8) including applicable support equipment and external wiring.

e) A set of qualification tests to be performed on the Qualification Test Specimen was created, including a defined set of Operability and Prudency tests to be conducted periodically during the qualification process. Operability and Prudency testing was performed before all qualification testing, after Environmental Stress testing, after EMI/RFI testing, and after Seismic testing. This was done to assess the impact of each group of tests on Test Specimen performance. A top-level description of these tests is shown in Figure 1.

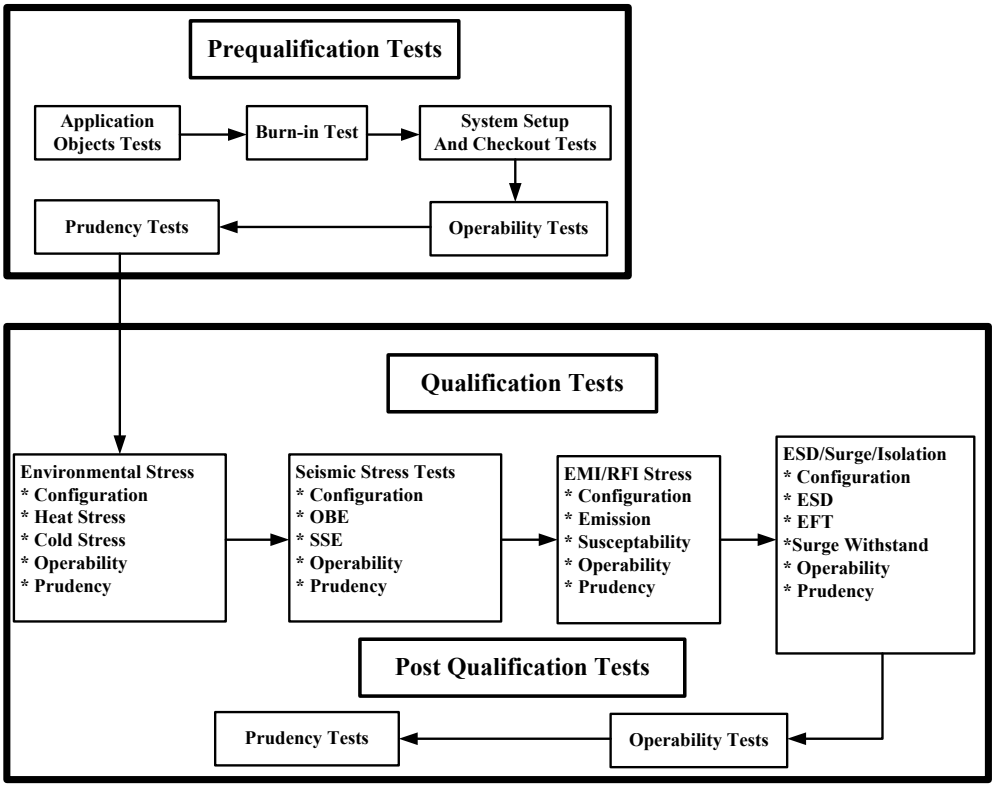


Figure 1. Overall Test Arrangement and Sequence

f) The qualification tests were performed, and the results were retained, analyzed for compliance with the acceptance criteria, and documented. A full report of qualification test results including completed procedures is given in TR901-302-01 (Reference 9). Baseline testing was performed periodically during the test sequence in Figure 1 to monitor for impacts on performance of the Qualification Test Specimen.

This test program intentionally duplicated the overall testing conducted for the original qualification of the HFC-6000 Safety Platform in order to demonstrate that the new FPGA hardware and software design will meet or exceed the capabilities of that platform. The specific sequence of EMI/RFI testing was not replicated due to the availability of laboratory equipment, and additional Operability and Prudency testing was performed relative to the original HFC-6000 qualification testing to obtain more information about the impacts of specific tests on the Test Specimen.

The HFC-FPGA qualification test does not include the Smoke Stress Test and the Radiation Stress Test. Smoke Stress Test was not conducted because the primary fire protection method is plant-specific fire protection designs that assess fire damage in defined fire zones, control fire and smoke propagation by design features and fire response procedures, and provide alternate safe shutdown means that are unaffected by fire damage to equipment in fire zones. Radiation Stress Test was not conducted because HFC-FPGA system will be housed in the auxiliary building control room in the plant and not in the containment building. Hence, it will not be exposed to radiation. 10 CFR Part 50, Appendix A (GDC 19-Control Room) states that adequate radiation protection shall be provided to permit access and occupancy of the control room under accident

conditions without personnel receiving radiation exposure in excess of 5 E-2 Sieverts (5 rem) whole body, or its equivalent to any part of the body, for the duration of the accident.

4.0 EQUIPMENT TESTED

The system layout drawings, wiring and power distribution diagrams, and assembly diagrams define specific details of the hardware design for the Qualification Test Specimen. Test plans and procedures provide detailed requirements and instructions for equipment mounting and interfaces to be used for equipment testing. The TSAP for each HFC-FCPU and HFC-FCPUX controller was developed as new application code using PromisE software and following the HFC Application Development process including the review and version management process required by the HFC QA Program Manual.

Figure 2 shows a typical configuration of the HFC-FPGA Qualification Test Specimen.

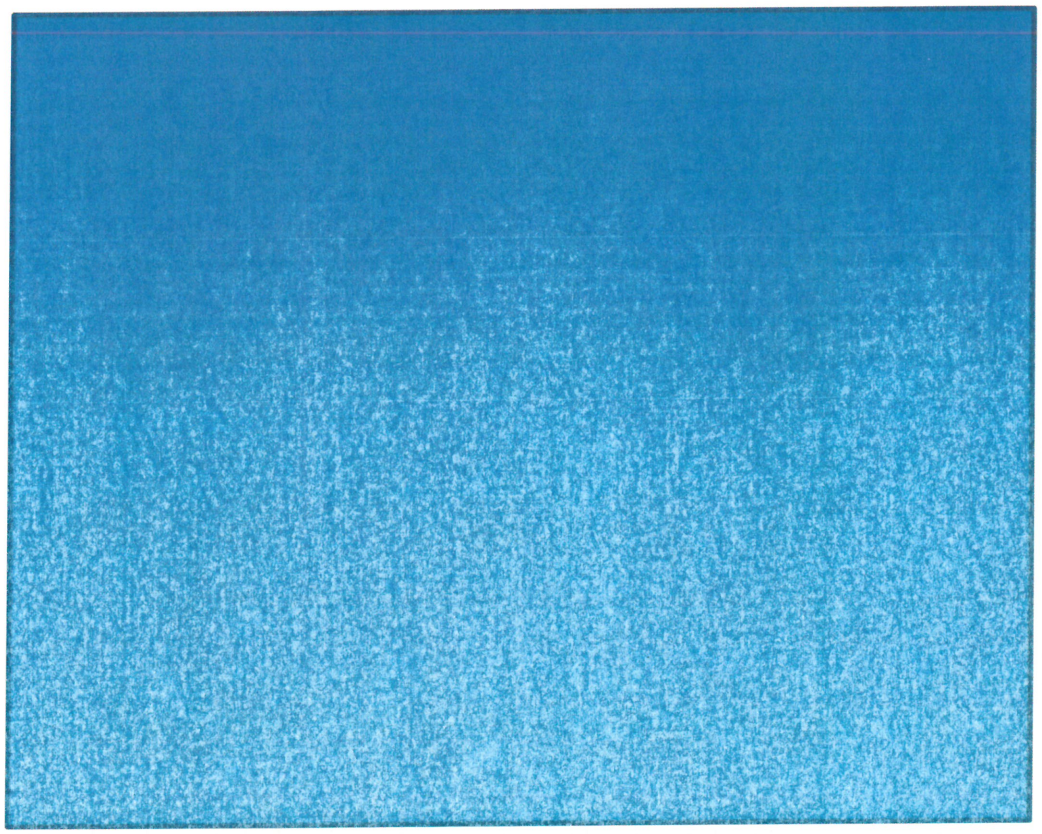


Figure 2. HFC-FPGA Qualification Test Specimen

Table 2 contains the Master Configuration List of equipment used in the VV0115 Qualification Test Specimen. Table 2 also describes functions of each module that were tested by the Qualification Test Specimen.

Table 2. Qualification Test Specimen Items

Rack Plug-In PCBs		
Designation	**Part Number**	**Function**
CON Cards (Plugs in at rear of backplane slots for interface to Termination Cards)		
Designation	**Part Number**	**Function**
Termination Cards (Field wire connection point. Connected to CON cards via DB25/50 cables)		
Designation	**Part Number**	**Function**

Miscellaneous Equipment		
Designation	**Part Number**	**Function**

Detailed configuration information, a full list of included hardware, and a detailed description of the TSAP is described in VV901-300-10 (Reference 8).

HFC-FPC08 gateway uses [ ] real time operating system, this version of [ ] has been dedicated by HFC for a customer and has been in use at power plants.

All FPGA used on the HFC-FPGA system were designed and manufactured by [ ], from the [ ] product lines. The specific [ ] FPGA chip used in each module is listed in Table 3:

Table 3. FPGA Type and Quantity

Module	FPGA Used	Quantity of FPGA used

The Qualification Test Specimen defined by HFC covered a subset of functional capabilities presented in EPRI TR-107330, Section 4. The specific capabilities demonstrated by the HFC qualification testing are as follows:

a) The capability of the test specimen to perform defined design functions within specified tolerances under normal environmental and operating conditions. Performance was measured using:

- Response Time for digital and analog I/O points,
- Digital and analog I/O point operability,
- Fault detection capability,
- Fault recovery capability,
- Redundancy and failover operability,
- External communication via RS-485.

b) The capability of the test specimen to perform design functions within specified tolerances under the stressed conditions defined in EPRI TR-107330, Sections 5 and 6. Specific stress conditions demonstrated the capability of the test specimen to:

- Function during and after exposure to abnormal temperature and humidity,
- Function during and after seismic stress,
- Function during and after application of EMI/RFI waveform exposures,
- Function during and after application of ESD/EFT/burst test discharges,
- Function during and after exposure to surge test waveforms.

These functional capabilities were selected to exercise the system in a manner comparable to a plant application.

5.0 TEST SYSTEM

Test system for the HFC-FPGA qualification testing includes HFC Plant Automated Tester (HPAT) and other supporting equipment. Figure 3 shows a typical configuration of the test system.

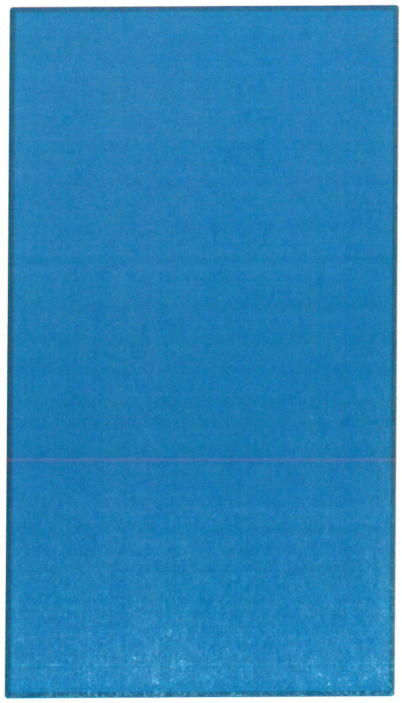


Figure 3. Typical HFC-FPGA Qualification Test System

Figure 4 shows the connection of the HFC-FPGA Qualification Test Specimen and Test System.

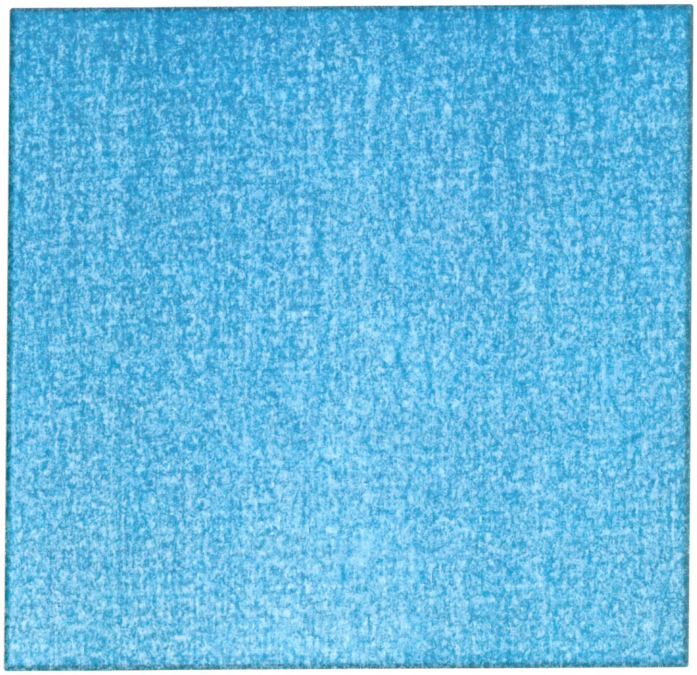


Figure 4. HFC-FPGA Qualification Test Specimen and Test System Connection

[

]

[

]

6.0 TEST REQUIREMENTS AND ACCEPTANCE CRITERIA

The generic EQ testing approach defined in the EQ Plans used guidance from EPRI TR-107330 to meet the requirements of IEEE Standard 323-2003 and other NRC guidance applicable to qualifying safety-related digital I&C systems intended for installation in a mild plant environment.

The qualification for the integrated test specimen consisted of a set of prequalification tests, a set of qualification tests, and a set of post-qualification tests as illustrated in Figure 1. These tests served two primary purposes:

- Tests conducted prior to the start of qualification testing confirmed that both the synthetic TSAP created for qualification testing purposes and the integrated hardware operated as intended.

- Operability and Prudency tests established a performance baseline for the test specimen as a whole. These tests were repeated at various points before, during, and after the qualification test to demonstrate that the system performance remained within acceptable limits.

The qualification tests exposed the test specimen to a specifically defined set of conditions as defined in EPRI TR-107330 and NRC RG 1.209. The purpose of these tests is to demonstrate the capability of the system hardware and software to continue operating within specified tolerances under extreme conditions. The full Operability and Prudency tests were run in between different qualification tests (Environmental, EMI/RFI, Seismic) to more accurately assess the effects of each specific test on the Test Specimen.

The Qualification Test System was monitored during the qualification test and any fault messages from the operational diagnostic were noted and evaluated. All self-diagnostics (including hardware watchdog timers) were in operation during qualification tests. This approach satisfied RG 1.209 Regulatory Position 2 that "qualification testing should be performed with the I&C system functioning, with software and diagnostics that are representative of those used in actual operation, while the system is subjected to the specific environmental service conditions, including abnormal operational occurrences."

The basic test acceptance criteria applied to the HFC-FPGA test specimen are the following:

- The HFC-FPGA test specimen will continue to function correctly during and/or after exposure to abnormal environmental conditions (temperature, and humidity).
- The HFC-FPGA test specimen will continue to function correctly during and after exposure to Operating Basis Earthquake (OBE) and Safe Shutdown Earthquake (SSE) seismic events.
- The HFC-FPGA test specimen will continue to function correctly during and after exposure to EMI/RFI, voltage surges, electrical fast transients, and electrostatic discharges.

- The HFC-FPGA test specimen will continue to function correctly during and after exposure to electrical faults applied to selected external interface points.

Correct functioning of the HFC-FPGA test specimen during normal and abnormal plant operating conditions was determined by the behavior or the performance of operational parameters identified in the respective test procedures. Correct functioning includes, but not limited to:

- Proper response of inputs to applied input signals,
- Proper response of outputs to application program control,
- Proper control of connected output devices,
- Proper operation of communication interfaces,
- Acceptable input/output (I/O) accuracy,
- Acceptable response time,
- Proper response to momentary interruption of input power,
- Proper response to loss of input power,
- Proper response to input power quality (voltage and frequency) variation,
- Proper failover to redundant components.

7.0 TEST PLANS AND TEST PROCEDURES

Pre-Qualification Test Plan (Reference 1) and Qualification Master Test Plan (Reference 2) were generated to provide a link between the guidance of EPRI TR-107330, NRC Regulatory guides, and the procedures that were used to conduct the tests. The test plan addresses the general approach for the test program, as detailed in VV901-300-09 (Reference 2). Two types of application programs are associated with the testing effort defined by these test plans:

- Test Specimen TSAPs for the HFC-FCPU and HFC-FCPUX controllers, and
- HFC Plant Automated Tester (HPAT) program for the test workstation.

The following Qualification Test Procedures were prepared:

- TP901-200-01 EPRI TR-107330 Burn-in Test Procedures,
- TP901-115-05 VV0115 Integration (Set-up and Check Out) Test Procedure,
- TP901-115-06 VV0115 TSAP Validation Test Procedure,
- TP901-115-01 VV0115 Qualification Operability Test Procedure,
- TP901-115-02 VV0115 Qualification Prudency Test Procedure,
- TP901-302-02 VV0115 Qualification Environmental Stress Test Procedure,
- TP901-302-03 VV0115 Qualification EMI/RFI Test Procedure,
- TP901-302-04 VV0115 Surge Withstand Test Procedure,
- TP901-302-05 VV0115 Electrostatic Discharge Withstand Test Procedure,
- TP901-302-06 VV0115 Qualification Seismic Test Procedure.

8.0 TEST RESPONSIBILITIES

All prequalification test activities were conducted by one or more qualified HFC test engineers and test technicians. Qualification tests that required specialized test equipment (e.g., Environmental, Seismic, and EMI/RFI/ESD/Surge Withstand testing) were conducted for HFC by personnel at qualified test facilities, including [ ]. HFC test personnel were present and conducted specified portions of the Operability and Prudency tests during these qualification tests.

Both test facilities were audited by HFC periodically and put on an HFC qualified vendor list. Laboratory testing services were performed in accordance with HFC procurement specification, which invoked the [ ] QA programs, which are in compliance with 10 CFR Part 50 Appendix B.

9.0 TEST CONTROL

HFC personnel were present to perform test setup and oversee all qualification testing performed by the test laboratory. HFC activities were performed according to the quality procedures for test control. Testing activities performed by HFC and the test laboratory were accomplished according to HFC test procedures.

HFC completed the procedures, recorded any deviation relating to the sequence of testing, the test specimen mounting, service conditions, test levels, test results and any exception, deficiency or field change which occurred during these tests. The results are summarized in the following Appendices A to F.

Issues and defects found during the qualification test execution were reported into Redmine or Condition Report (CR). Issues reported may be assigned to be fixed or the issue may be determined not needed to be fixed.

All test exceptions, deficiencies, and field changes resulting from discrepancies or deficiencies in test documentation or unacceptable test specimen hardware or software performance during qualification testing are identified in appendices A to F of this summary report and have been processed and resolved in accordance with HFC quality procedures.

10.0 MEASUREMENT AND TEST EQUIPMENT

All measurement and test equipment (M&TE) used in the HFC-FPGA Qualification Test Specimen qualification testing project to acquire data according to the qualification test procedures were calibrated. Calibration was done by a 3rd party vendor, [ ]. They were certified by Perry Johnson Laboratory Accreditation to ISO/IEC 17025:2005. The certificate of accreditation also bears ILAC MRA logo.

Test engineers recorded the used M&TE in the Test Equipment Log in the test procedures.

The test equipment used by [
] is calibrated per lab's QA program, test equipment ID/manufacturer/model/calibration information are recorded in the test reports issued by [
].

11.0 TEST SCHEDULE

The HFC-FPGA qualification test execution schedule is shown in Table 4. The ESD test was conducted in two phases. The first phase was conducted from September 7 to 13 of 2016, and the second was conducted on February 11 of 2017. All test points passed during the first phase of testing, but several FPC08 test points were erroneously performed without automated tests logging data, so they were re-run on February 11, 2017 to gather this data.

Table 4. Qualification Test Execution Schedule

Test	Execution Period
Prequalification Test	November 25, 2015 - June 6, 2016
Environmental Stress Test	June 6, 2016 - June 13, 2016 Post Test June 17, 2016 - June 24, 2016
EMI/RFI Test	June 27, 2016 - September 26, 2016 Post Test: September 28, 2016 - October 13, 2016
ESD Test	September 7, 2016 - September 13, 2016 and February 11, 2017
Surge Withstand Test	August 2, 2016 - September 9, 2016
Seismic Test	October 17, 2016 Post Test: October 26, 2016 - November 16, 2016

12.0 TEST DOCUMENTATION

This document is the summary report of EQ test results required by the NRC Interim Staff Guide DI&C-ISG-06, item D.3. Appendices A through F of this summary report provide a synopsis of each test and identify the supporting documentation that serves as the detailed record of the qualification testing and analysis of the HFC-FPGA Qualification Test Specimen.

The Test Summaries describe the results obtained from the implementation of the test procedures that were executed in accordance with the Test Plans.

The following terminology is used in the Appendices to describe the results of the qualification testing:

- Passed – Test acceptance criteria were met and all the anomalies found during the test execution were successfully resolved.
- Failed - Some test acceptance criteria were not met or some anomalies found during the test execution were not successfully resolved.

Detailed test results were recorded in Qualification Test Report TR901-302-01 (Reference 9).

13.0 EVALUATION OF TEST RESULTS

Test results for all qualification testing consist of a description of specific test conditions, analyzed data of automated tests conducted, and a report from the testing laboratory. A final summary of test results is detailed in TR901-302-01 (Reference 9), Section 12. EMI/RFI testing results from [ ] are detailed in PR037435, which is included as Attachment 13.18 of TR901-302-01 (Reference 9). Environmental testing results from [ ] are detailed in [ ] Certificate of Test 13999, which is included as Attachment 13.19 of TR901-302-01 (Reference 9). Seismic testing results from [ ] are detailed in 14149 IEEE Seismic Qualification Test Report, which is included as Attachment 13.25 of TR901-302-01 (Reference 9). The EMI/RFI, Environmental, and Seismic conditions that the VV0115 Test Specimen was subjected to through the course of these tests was a generic set of environmental conditions used to follow the guidance set forth in RG 1.209.

The Test Specimen was found to have operated normally during and following all qualification testing. All data logged during each step of qualification tests was analyzed and compared to the acceptance criteria. In-depth analysis of this data is included in TR901-302-01 (Reference 9) for each qualification test. The Test Specimen met all the acceptance criteria listed for Prequalification Tests, Operability Tests, Prudency Tests, Environmental Stress Qualification Tests, EMI/RFI Qualification Tests, Electrostatic Discharge Tests, Surge Withstand Tests, Seismic Tests, and Post Qualification Tests.

14.0 AS-TESTED EQUIPMENT QUALIFICATION ENVELOPE

Successful execution of the EQ tests defined in the Test Plans is intended to qualify the generic HFC-FPGA digital safety I&C platform for a qualification envelope substantiated by the actual test levels. The as-tested equipment qualification envelope is summarized in Table 5.

Table 5. Equipment Qualification Envelope

Equipment Qualification Category	Source of Qualification Test Specification	Modifications to Test Setup or Qualification Envelope	Qualification Test Acceptance Criteria
Environmental (Temperature & Humidity)	EPRI TR-107330 Sections 4.3.6, 4.6.1.1, 5.5, 6.2.1.1 item B, 6.3.1, 6.3.3 and 6.4.3, Figure 4-4, Table 5-1	The low-temperature test was longer than 8 hours due to a chamber air vent getting iced over periodically. The test was run long enough for over 24 hours of total run time at or below 33 °F (0.6 °C) cumulatively. Meeting requirement of 8 hours at 40 °F or lower for EPRI TR-107330 Figure 4-4.	Section 4.3.6 of EPRI TR-107330, 1996
Seismic	EPRI TR-107330 Sections 4.3.9, 4.4.6.1, 4.6.1.1, Figure 4-5, Table 5-1, 6.2.1.1.A, 6.3.1.C, 6.3.4	No modification made to qualification envelope.	Section 4.3.9 of EPRI TR-107330, 1996
EMI/RFI	The required levels of EMI/RFI susceptibility and radiation limits are defined in USNRC RG 1.180, Rev 1 – 2003. Radiated Susceptibility Test – RS101 (Reference MIL-STD 461E Paragraph 5.18) Radiated Susceptibility Test – RS103 (Reference MIL-STD 461E Paragraph 5.19) Conducted Susceptibility Test – CS101 (Reference MIL-STD 461E Paragraph 5.7)	No modification made to qualification envelope. No Modifications to test setup: CE102, CE101, CS114, RS101, CS115, CS116, RS103, RE101, CS101. 24 VDC wires twisted together inside unit, ½" braided grounding strap secured to chassis ground: IEC 61000-4-4, IEC 61000-4-5, IEC 61000-4-12 24 VDC wires twisted together inside unit, ½" braided grounding strap secured to chassis ground, FPC08 bezel grounded with field wire to	MIL-STD-461E and USNRC RG 1.180 list the maximum signal strength for each of the susceptibility tests. USNRC RG 1.180, Rev 1 - 2003 indicates the maximum acceptable equipment emissions and susceptibility level for each frequency range.

	Conducted Susceptibility Test – CS114 (Reference MIL-STD 461E Paragraph and 5.12) Conducted Susceptibility Test – CS115 (Reference MIL-STD 461E Paragraph 5.13) Conducted Susceptibility Test – CS116 (Reference MIL-STD 461E Paragraph 5.14) Radiated Emissions Test – RE101 and RE102 (Reference MIL-STD 461E Paragraph 5.15 and 5.16) Conducted Emissions Test – CE101 and CE102 (Reference MIL-STD 461E Paragraph 5.4 and 5.5)	chassis ground: IEC 61000-4-2 24 VDC wires twisted together inside unit, ½" braided grounding strap secured to chassis ground, FPC08 bezel grounded with field wire to chassis ground, signal and power cables enclosed in grounded conduit: RE102	
Surge Withstand & Electrical Fast Transient (EFT)	NRC RG 1.180 on power surge tests. EPRI TR-107330 section: 4.3.4.4.F, 4.6.2, 4.6.8, 6.3.1.E, 6.3.5, 8.6.1.C.	No modification made to qualification envelope.	Section 4.6.2 of EPRI TR-107330, 1996 and RG 1.180, Revision 1
Electrostatic Discharge (ESD)	EPRI TR-107330 Sections 4.3.8, Table 5-1, 6.3.1.B, 6.4.2 The level of ESD immunity required is defined in EPRI TR-102323-R1 Appendix B.	No modification made to qualification envelope.	Section 4.3.8 of EPRI TR-107330, 1996

15.0 SUMMARY

The HFC-FPGA platform have passed successfully the following qualification tests:

- Prequalification Test
- Environmental Stress Test
- EMI/RFI Test
- ESD Test
- Surge Withstand Test
- Seismic Test

[

]

[

]

16.0 REFERENCES

1.	HFC Document TP901-200-00, "Pre-Qualification Test Plan."
2.	HFC Document VV901-300-09, "VV0115 Qualification Master Test Plan."
3.	Interim Staff Guidance - Task Working Group #6: Licensing Process, DI&C-ISG-06, Revision 2, U.S. Nuclear Regulatory Commission
4.	RG 1.209, "Guidelines for Environmental Qualification of Safety-Related Computer-Based Instrumentation and Control Systems in Nuclear Power Plants", 2013
5.	IEEE Standard 323, "IEEE Standard for Qualifying Class 1E Equipment for Nuclear Power Generating Stations", 2003
6.	EPRI TR-107330, "Generic Requirements Specification for Qualifying a Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants", December 1996
7.	RG 1.180, "Guidelines for Evaluating Electromagnetic and Radio-Frequency Interference in Safety-Related Instrumentation and Control Systems", 2003
8.	VV901-300-10, "VV0115 FPGA Test Specimen Design Description."
9.	TR901-302-01, "HFC-FPGA Control System of HFC-6000 Safety Platform Qualification Test Report."
10.	TP901-115-05, "Qualification Integration (Set-up and Check-out) Test Procedure."
11.	TP901-115-06, "VV0115 TSAP Validation Test Procedure."
12.	TP901-115-04, "VV0115 Qualification Application Software Objects Test Procedure."
13.	TP901-115-01, "VV0115 Qualification Operability Test Procedure."
14.	TP901-115-02, "VV0115 Qualification Prudency Test Procedure."

15.	TP901-200-01, “EPRI TR 107330 Qualification Program Burn-In Test Procedures.”
16.	TP901-302-02, “VV0115 Environmental Stress Test Procedure.”
17.	TP901-302-03, “VV0115 Qualification System EMI/RFI Test Procedure.”
18.	TP901-302-05, “VV0115 Qualification System ESD Test Procedure.”
19.	TP901-302-04, “VV0115 Qualification System Surge Withstand Test Procedure.”
20.	TP901-302-06, “VV0115 Qualification Seismic Test Procedure.”
21.	TR901-200-02, “ERD111 Pre-Qualification before Retest Detail Report.”
22.	TR901-200-03, “ERD111 Environment Stress Retest Detail Report.”
23.	TR901-200-05, “ERD111 Post Qualification After Retest Detail Report.”

Appendix A. Prequalification Test Summary

A.1. Purpose

This test summary describes the Prequalification Test of the HFC-FPGA Qualification Test Specimen and Test System and presents the results of this test. The purpose of the Prequalification Test was to verify that the project specified hardware, wiring, and communication cabling had been installed and that communication was established over each communication link before the start of the Qualification Test.

A.2. Objective

The Prequalification Test verified that the Test Specimen was properly assembled and fully operational prior to the initial execution of the Operability and Prudency tests. These latter tests established a performance baseline for performance during and after each of the qualification stress tests.

A.3. Equipment Tested

The equipment tested were the HFC-FPGA Qualification Test Specimen and Test System. Table 2 identifies the specific items that are part of the Qualification Test Specimen.

A.4. Sequence of Testing

The Prequalification Test is the first test performed on Qualification Test Specimen and Test System. The Prequalification Test was performed at the HFC test facility in Carrollton, TX. Based on Figure 1, the prequalification test includes the following tests:

- Application Software Object Test
- Burst-in Test
- Integration (System Set-up and Check-out) Test
- TSAP Validation Test
- Operability Test
- Prudency Test

A.5. Procedures

The following procedures were used during the Prequalification Test:

- TP901-115-04, VV0115 Qualification Application Software Objects Test Procedure (Reference 12): This procedure includes a series of tests defined in Section 5.6 of EPRI TR-107330. Software objects that have a direct impact on the application code or that can be accessed by application code while it is running on the HFC-FPGA platform were verified.
- TP901-200-01, EPRI TR 107330 Qualification Program Burn-In Test Procedures (Reference 15): This procedure includes a series of tests defined in Section 5.2 of EPRI TR-107330. Test specimen ran in a normal operating environment for a

minimum period of 352 hours to detect any early-life failures of FPGA/PCB and components. This test included spare parts which can be used to replace for any PCB that fails during subsequent qualification tests.

- TP901-115-05, VV0115 Qualification Integration (Set-up and Check-out) Test Procedure (Reference 10): This procedure includes a series of tests defined in Section 5.2 of EPRI TR-107330. Through this procedure, initial HFC-FPGA Qualification Test Specimen calibration was addressed, and the correct operation of the HFC-FPGA Qualification Test Specimen and Test System was verified.
- TP901-115-06, VV0115 TSAP Validation Test Procedure (Reference 11): This procedure includes a series of tests defined in Section 5.2 of EPRI TR-107330. The simulated control loop logic was wired to I/O points, and its functional operation was verified directly. The logic and I/O points were available for use as static test points, but they were not generally part of any automated test.
- TP901-115-01, VV0115 Qualification Operability Test Procedure (Reference 13): This procedure includes a series of tests defined in Section 5.3 of EPRI TR-107330 that verified acceptable performance of the HFC-FPGA Qualification Test Specimen in accordance with the manufacturer's specifications for the HFC-FPGA platform. The prequalification test run of this procedure established baseline performance of the HFC-FPGA Qualification Test Specimen for use in performance of the Operability Test Procedure throughout qualification testing.
- TP901-115-02, VV0115 Qualification Prudency Test Procedure (Reference 14): This procedure includes a series of tests defined in Section 5.4 of EPRI TR-107330 that verified acceptable performance of the HFC-FPGA Qualification Test Specimen in accordance with the manufacturer's specifications for the HFC-FPGA platform. The prequalification test run of this procedure established baseline performance of the HFC-FPGA Qualification Test Specimen for use in performance of the Prudency Test Procedure throughout qualification testing.

All procedures above include instructions and checklists for performing the Prequalification Test as follows:

- Perform Application Software Objects Test
    - Failure Detection Test (Loss of Communication Path)
    - Software Tools Verification
    - Configuration Management Verification
    - Sequence of Events (SOE) Processing Verification
    - Human/Machine Interface Verification
    - Alarm Processing Test
- Perform Burn-In Test
- Perform Integration (Set-up and Check-out) Test
    - Equipment / Hardware Setup
    - Continuity Test
    - Telnet Communication Test
    - I/O Functional Test
- Perform TSAP Validation Test
    - Source Code Verification
    - Operability Test Support
        - Accuracy Test

        - Digital and Analog Response Time Tests
        - Timer Test
    - Prudency Test Support
- Perform Operability Test
    - Accuracy Test
    - Response Time Test
    - Discrete Input Operability Test
    - Discrete Output Operability Test
    - Communication Operability Test
    - Timer Test
    - Failure to Complete Scan Detection
    - Failover Test
    - Power Supply Redundancy Test
    - Loss of Power Test
- Perform Prudency Test
    - Burst of Events Test
    - Serial Port Failure / Noise Test

A.6. Test Specimen Mounting

EPRI TR-107330 provides no requirements or guidance for mounting of the test specimen during the prequalification test.

As shown in Figure 5, selected components of the HFC-FPGA system were configured as redundant racks (Test Specimen) using DPS and LDS logic and I/O configuration. Each rack includes redundant HFC-FPC08 gateway controllers, redundant HFC-FCPU controllers, redundant HFC-FCPUX controllers and a set of FPGA digital and analog I/O boards which are mounted in a single chassis. One chassis that serves as the HPAT is connected to the Test Specimen by several bundles of signal cable. The complete Test Specimen (controllers, I/O modules, and chassis) was subjected to a battery of tests intended to qualify it as a controller configuration to be used in safety-related applications.

Figure 5. Test Specimen Mounting for Prequalification Test

A.7. Service Conditions

EPRI TR-107330 provides no requirements or guidance for operation of the test specimen during the Prequalification Test. During prequalification test, the HFC-FPGA Test Specimen was powered with the I/Os operating under control of the TSAP and the connected test system simulation devices.

EPRI TR-107330 provides no requirements or guidance for control of ambient conditions (temperature, pressure, and humidity) during the Prequalification Test. During prequalification test, the test space conditions of temperature and humidity were maintained within the normal operating range of the HFC-FPGA Test Specimen as follows:

- Temperature: 50° to 104° F
- Relative Humidity: 7% to 90%

A.8. Test Levels

The test levels (supply power and I/O signal and load levels) applied to the HFC-FPGA Test Specimen during the Prequalification Test were set as specified in corresponding test procedures (References 10 - 15).

A.9. Performance Monitoring

Performance monitoring of the HFC-FPGA Test Specimen during the Prequalification Test were set as specified in corresponding test procedures (References 10 - 15).

A.10. Acceptance Criteria

Acceptance criteria for performance monitoring of the HFC-FPGA Test Specimen during the Prequalification Test were set as specified in corresponding test procedures (References 10 - 15). They are summarized in Table 6.

Table 6. Acceptance Criteria for Prequalification Test

Test	Sub-Test	Acceptance Criteria
Application Software Objects Test	Failure Detection Test (Loss of Communication Path)	
	Software Tools Verification	
	Configuration Management Verification	

Test	Sub-Test	Acceptance Criteria
	Sequence of Events (SOE) Processing Verification	
	Human/Machine Interface Verification	
	Alarm Processing Test	
Burn-In Test	N/A	
Integration (Set-up and Check-out) Test	Equipment / Hardware Setup	
	Continuity Test	

Test	Sub-Test	Acceptance Criteria
	Telnet Communication Test	
	I/O Functional Test	
TSAP Validation Test	Source Code Verification	
	Operability Test Support - Accuracy Test	
	Operability Test Support - Digital Response Time Test	

Test	Sub-Test	Acceptance Criteria
	Operability Test Support - Analog Response Time Test	
	Operability Test Support - Timer Test	
	Prudency Test Support - Burst of Events Test	
Operability Test	Accuracy Test (Automatic and Manual)	
	Response Time Test (Digital and Analog)	
	Discrete Input Operability Test	
	Discrete Output Operability Test	
	Communication Operability Test	

Test	Sub-Test	Acceptance Criteria
	Timer Test	
	Failure to Complete Scan Detection	
	Failover Test	
	Redundancy Test	
	Loss of Power Test	
Prudency Test	Burst of Events Test	

Test	Sub-Test	Acceptance Criteria
	Serial Port Failure / Noise Test	

A.11. Documentation

The following attachments in TR901-302-01 (Reference 9) were prepared as records by HFC to document the results of HFC-FPGA prequalification test:

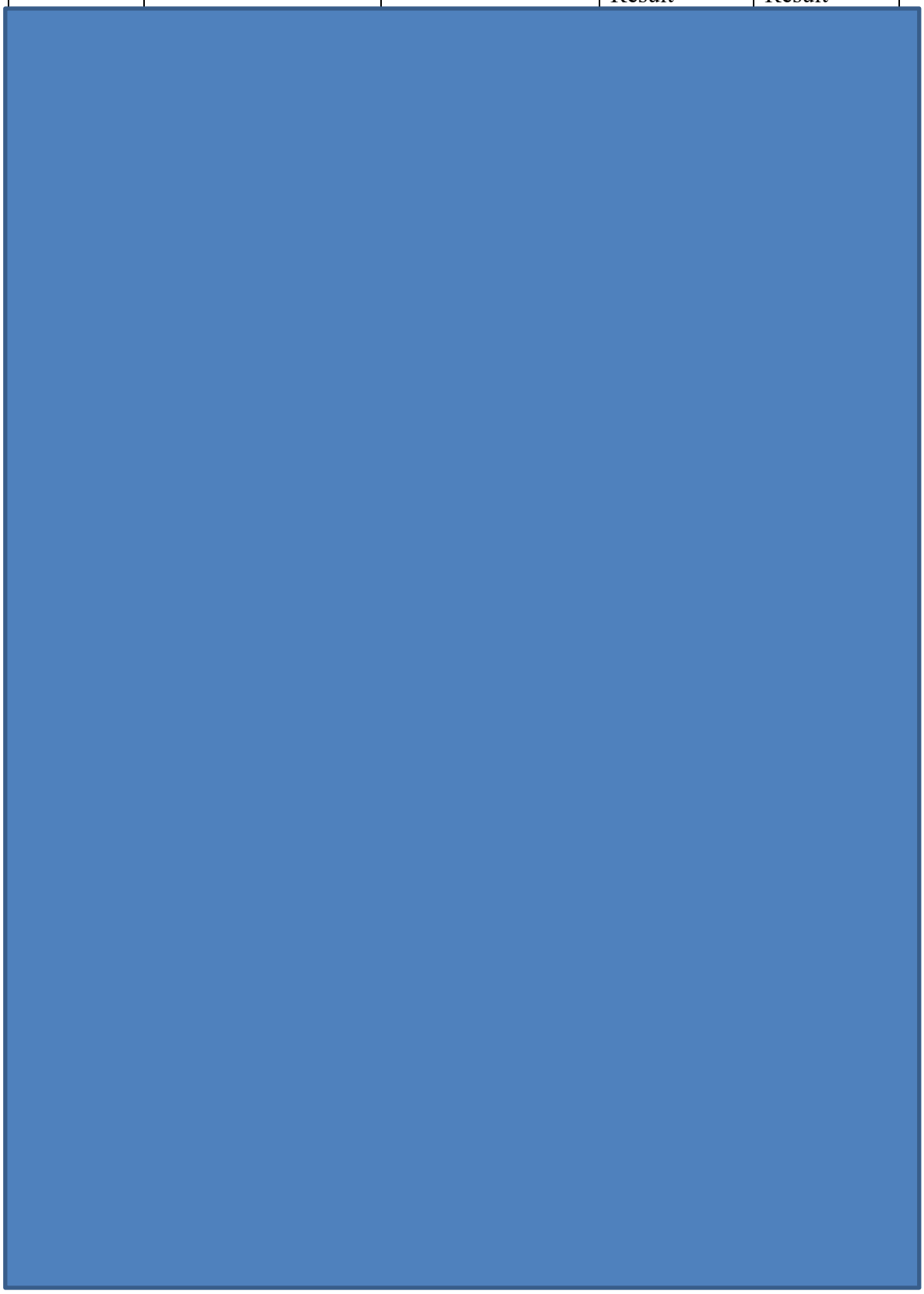
- Application Software Objects Test
  - Attachment 13.2 Completed record of TP901-115-04, Application Software Object Test Procedure
- Burn-In Test
  - Attachment 13.1 Completed record of TP901-200-01, Burn In Test Procedure
- Integration (Set-up and Check-out) Test
  - Attachment 13.6 Completed record of TP901-115-05, Integration Test Procedure
- TSAP Validation Test
  - Attachment 13.3 Completed record of TP901-115-06, TSAP Validation Test Procedure
  - Attachment 13.4 Highlighted record of 71005901Q
  - Attachment 13.5 Highlighted record of 71005902Q
- Operability Test
  - Attachment 13.8 Completed record of TP901-115-01, Operability Test Procedure for Pre-test
- Prudency Test
  - Attachment 13.7 Completed record of TP901-115-02, Prudency Test Procedure for Pre-test

A.12. Test Results

Detailed test results of the Prequalification Test were reported in TR901-302-01 (Reference 9), which are summarized in Table 7.

Table 7. Summary of Prequalification Test Results

Test	Sub-Test	Redmine or CR	Sub-Test Result	Overall Result



Operability Test	Response Time Test	Yes, CR No: 2016-0204	Passed	

A.13. Resolution of Test Discrepancies

HFC uses a Condition Report Microsoft Access Database and a Redmine project management and issue tracking tool to record all the issues encountered during Equipment Qualification.

During Prequalification, below issues were tracked and resolved:

Redmine issue 593, created on 3/29/2016, AO glitch observed on FPUAO with an oscilloscope. [

]

Redmine issue 594, created on 3/29/2016, some DO channels on FPUD01 are not working, channels regain functionality after a board reset. [

]

Redmine issue 601, created on 4/5/2016, DO glitch observed on FPUD01 with an oscilloscope and in SOE data. [

]

Redmine issue 605, created on 4/25/2016, accuracy requirement for FPGA analog cards have not been met. Acceptance criteria need to be added to the test procedure. [

]

Redmine issue 606, created on 5/3/2016, some input channels on FPUL reported Ok when there is no input (Open). [

]

Redmine issue 607, created on 5/11/2016, FPUAO 8th channel error LED flashes when there is no input. A jumper was missing on the termination board for those unused AO channels. [ ]

Redmine issue 613, created on 5/26/2016, Failure to Complete Scan test results does not meet EPRI TR-107330 5.3H. [

]

Redmine issue 616, created on 6/03/2016. New FCPUX FPGA load enabled F-link diagnostics, one FCPUX shows F-link CRC error when both FCPUX have identical hardware, FPGA load and configuration switch settings. [

]

Condition Report CR2016-0083, created on 3/10/2016. The G-link for 3 HFC-FPC08 does not work properly. [
]

Condition Report CR2016-0186, created on 5/27/2016, two red-line changes to TP901-115-04, Application Software Object Test Procedure, per errors discovered in VV0115 baseline testing. [
]

Condition Report CR2016-0187, created on 5/27/2016, five red-line changes to TP901-115-05, Integration Test Procedure, per errors discovered in VV0115 baseline testing. [

]

Condition Report CR2016-0192, created on 6/1/2016, seventeen red-line changes to TP901-115-02, Prudency Test Procedure, per errors discovered in VV0115 baseline testing. [
]

Condition Report CR2016-0204, created on 6/9/2016, fourteen red-line changes to TP901-115-01, Operability Test Procedure, per errors discovered in VV0115 baseline testing. [
]

Appendix B. Qualification Test Summary – Environmental Stress Test

B.1. Purpose

This test summary describes the Environmental Stress Test of the HFC-FPGA Qualification Test Specimen and Test System and presents the results of this test. The purpose of the Environmental Stress Test was to demonstrate that the physical components of the Qualification Test Specimen work within acceptable parameters including timing and maintaining contact during heating and cooling.

B.2. Objective

The objective of Environmental Stress Test was to demonstrate the HFC-FPGA Qualification Test Specimen did not experience failures due to abnormal service conditions of temperature and humidity. Section 4.3.6 of EPRI TR-107330 defines the recommended normal and abnormal temperature and humidity exposure levels the test specimen must withstand (i.e., the test specimen must continue to meet the manufacturer specified performance levels).

B.3. Equipment Tested

The equipment tested were the HFC-FPGA Qualification Test Specimen. Table 2 identifies the specific items that are part of the Qualification Test Specimen.

B.4. Sequence of Testing

EPRI TR-107330 states that the Environmental Stress Test is the first of the Qualification Tests to be conducted. Based on Figure 1, the Environmental Stress Test includes the following tests:

- Configuration: Pre-Test Setup and Inspection
- Test E1: High Temperature Heat Stress
- Operability and Prudency Check: High Temperature
- Test T1: Ramp Down to Low Temperature
- Test E2: Low Temperature Cold Stress
- Operability and Prudency Check: Low Temperature
- Test T2: Ramp Up to Ambient Temperature
- Operability and Prudency Check: Ambient Temperature
- Operability Test: Post Environmental Stress Test
- Prudency Test: Post Environmental Stress Test

The Environmental Stress Test consisted of three major phases (Figure 6):

- Test E1: A minimum [ ]-hour period with the ambient temperature at [ ] at [ ]% RH and a transition period of [ ] during which the ambient temperature is reduced to [ ] at [ ]% RH (non-condensing).
- Test E2: A minimum 8-hour period with the ambient temperature at [ ] with [ ]% (non-condensing).

- Tests T1 and T2: A transition period of [ ] during which the test chamber is brought back to ambient room temperature and humidity.

As specified in EPRI TR-107330, operability checks or validation tests are required at various points during the test to ensure that the platform continues to operate normally. The specific test period minimum durations are depicted in Figure 6.

Figure 6. Environmental Stress Test Profile

Note: The black dots on the graph designate the operability check points required by the EPRI standard.

B.5. Procedures

The following procedures were used during the environmental test:

- TP901-302-02, VV0115 Environmental Stress Test Procedure (Reference 16): Through this procedure, the HFC-FPGA Qualification Test Specimen received additional configuration in the test chamber for Environmental Stress Test. The performance of the HFC-FPGA Qualification Test Specimen was monitored throughout application of the Environmental Stress Test conditions.
- TP901-115-01, VV0115 Qualification Operability Test Procedure (Reference 13): This procedure includes a series of tests defined in Section 5.3 of EPRI TR-107330 that verified acceptable performance of the HFC-FPGA Qualification Test Specimen in accordance with the manufacturer's specifications for the HFC-FPGA platform. During each phase of Environmental Stress Test, specified portions of this procedure was performed. A complete repetition of this test procedure was performed as part of the Post Environment Stress Test.
- TP901-115-02, VV0115 Qualification Prudency Test Procedure (Reference 14): This procedure includes a series of tests defined in Section 5.4 of EPRI TR-107330 that verified acceptable performance of the HFC-FPGA Qualification Test Specimen in accordance with the manufacturer's specifications for the HFC-FPGA platform. During each phase of Environmental Stress Test, specified portions of this procedure was performed. A complete repetition of this test procedure was performed as part of the Post Environment Stress Test.

B.6. Test Specimen Mounting

The Environmental Stress Test was conducted at [
]. The Qualification Test Specimen and HPAT were disassembled at the HFC facility, transported to the [ ] facility, and set up for testing by HFC personnel. All components of the Test Specimen were installed in the environmental chamber as shown in Figure 7, and the HPAT, workstation, and monitoring equipment were set up outside the chamber. During installation of the equipment, the Qualification Test Specimen hardware and cables were inspected for any sign of mechanical damage before conducting the pre-test functional verification. [ ] personnel were responsible for installing temperature / humidity sensors and connecting them to a chart recorder.

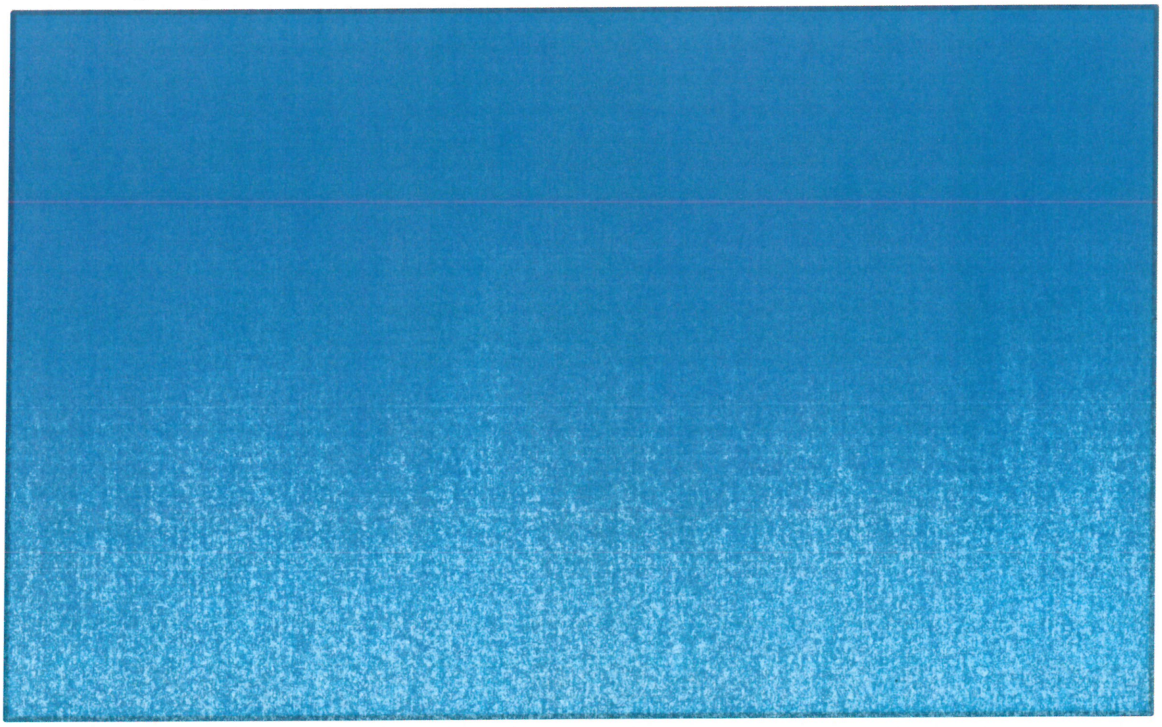


Figure 7. Test Specimen Arrangement in Environmental Stress Test Chamber

B.7. Service Conditions

Environmental Stress Test levels for temperature and relative humidity were determined from EPRI TR-107330, with a 5% margin added. These conditions were used as a generic environmental condition, in place of plant-specific measured conditions. Environmental conditions for this test are sketched in Figure 6 and detailed in Figure 8.

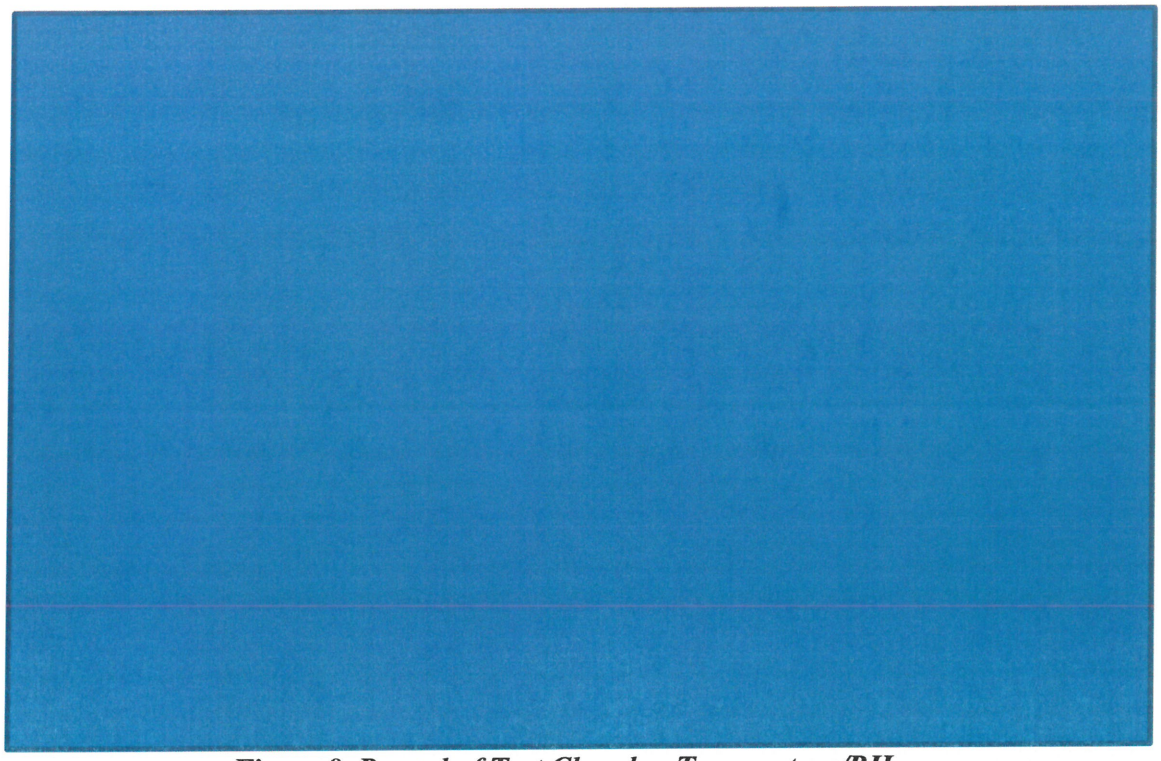


Figure 8. Record of Test Chamber Temperature/RH

B.8. Test Levels

The test levels (supply power and I/O signal and load levels) applied to the HFC-FPGA Test Specimen during the Environmental Stress Test were set as specified in corresponding test procedures (References 13, 14, and 16).

B.9. Performance Monitoring

Performance monitoring of the HFC-FPGA Test Specimen during the Environmental Stress Test were set as specified in corresponding test procedures (References 13, 14, and 16).

B.10. Acceptance Criteria

Acceptance criteria for performance monitoring of the HFC-FPGA Test Specimen during the Environmental Stress Test were set as specified in corresponding test procedures (References 13, 14, and 16). They are summarized in Table 8.

Table 8. Acceptance Criteria for Environmental Stress Test

Test	Sub-Test	Acceptance Criteria
Configuration: Pre-Test Setup and Inspection	Output Level of Power Supplies Verification	
	Qualification Test Specimen Status Verification	
	Alarm Status Verification	
Test E1: High Temperature Heat Stress	N/A	
Operability and Prudency Check: High Temperature	Operability - Automated Analog Accuracy Test	
	Operability - Automated Response Time Test	
	Operability - Communication Operability Test	
	Operability - Automated Timer Test	
	Operability - Loss of Power Test	

Test	Sub-Test	Acceptance Criteria
	Prudency - Analog and Digital Burst of Events Test	
Test T1: Ramp Down to Low Temperature	N/A	
Test E2: Low Temperature Cold Stress	N/A	
Operability and Prudency Check: Low Temperature	Operability - Automated Analog Accuracy Test	
	Operability - Automated Response Time Test	
	Operability - Communication Operability Test	
	Operability - Automated Timer Test	
	Operability - Loss of Power Test	

Test	Sub-Test	Acceptance Criteria
	Prudency - Analog and Digital Burst of Events Test	
Test T2: Ramp Up to Ambient Temperature	N/A	
Operability and Prudency Check: Ambient Temperature	Accuracy Test (Automatic)	
	Response Time Test (Digital)	
	Communication Operability Test	
	Timer Test	
	Loss of Power Test	

Test	Sub-Test	Acceptance Criteria
	Burst of Events Test	
Operability Test: Environmental Post Test	Accuracy Test (Automatic and Manual)	
	Response Time Test (Digital and Analog)	
	Discrete Input Operability Test	
	Discrete Output Operability Test	
	Communication Operability Test	
	Timer Test	

Test	Sub-Test	Acceptance Criteria
	Failure to Complete Scan Detection	
	Failover Test	
	Redundancy Test	
	Loss of Power Test	

Test	Sub-Test	Acceptance Criteria
Prudency Test: Environmental Post Test	Burst of Events Test	
	Serial Port Failure / Noise Test	

B.11. Documentation

The following attachments in TR901-302-01 (Reference 9) were prepared as records by HFC to document the results of HFC-FPGA prequalification test:

- Environmental Stress Test
  - Attachment 13.19: [ ] Certificate of Test 13999
  - Attachment 13.9 Completed record of TP901-302-02, VV0115 Environmental Stress Test Procedure
- Operability and Prudency Check
  - Attachment 13.10 Completed record of TP901-115-01, Operability Test Procedure for high temperature operability check
  - Attachment 13.11 Completed record of TP901-115-02, Prudency Test Procedure for high temperature operability check
  - Attachment 13.12 Completed record of TP901-115-01, Operability Test Procedure for low temperature operability check
  - Attachment 13.13 Completed record of TP901-115-02, Prudency Test Procedure for low temperature operability check
  - Attachment 13.14 Completed record of TP901-115-01, Operability Test Procedure for ambient temperature operability check
  - Attachment 13.15 Completed record of TP901-115-02, Prudency Test Procedure for ambient temperature operability check
- Post Environmental Stress Test
  - Attachment 13.16 Completed record of TP901-115-01, Operability Test Procedure for Post-Environmental tests
  - Attachment 13.17 Completed record of TP901-115-02, Prudency Test Procedure for Post-Environmental tests

B.12. Test Results

Detailed test results of the Environmental Stress Test were reported in TR901-302-01 (Reference 9), which are summarized in Table 9.

Table 9. Summary of Environmental Stress Test Results

Test	Sub-Test	Redmine or CR	Sub-Test Result	Overall Result

Test	Sub-Test	Redmine or CR	Sub-Test Result	Overall Result

B.13. Resolution of Test Discrepancies

HFC uses a Condition Report Microsoft Access Database and a Redmine project management and issue tracking tool to record all the issues encountered during Equipment Qualification.

During Environmental Stress Test, below issues were tracked and resolved:

Redmine issue 622, created on 6/09/2016, FPUD01 goes into alarm briefly when chamber temperature was about 61~66 degrees C, then alarm clears automatically. [

]

Redmine issue 623, created on 6/09/2016, FPUM2 goes into alarm briefly then alarm clears automatically. [

]

Redmine issue 628, created on 6/15/2016, FCPUX goes into alarm while ramping up to high temperature/humidity. FCPU redundancy interface down alarm was toggling every few seconds. [

]

CR2020-0014, created on 1/30/2020, engineers were assigned to investigate symptoms described in Redmine issue 628. High temperature environment was recreated at HFC facility, attempting to verify if the FCPUX RIF down alarm symptom can be duplicated. [

]

Appendix C. Qualification Test Summary – EMI/RFI Test

C.1. Purpose

This test summary describes the EMI/RFI Test performed on the HFC-FPGA Qualification Test Specimen. The purpose is to establish the range and magnitude of RF radiation produced by the Qualification Test Specimen, and the impact of electromagnetic interference (EMI) on the reliable operation of the Qualification Test Specimen.

C.2. Objective

The objective of EMI/RFI Test was to demonstrate the suitability of the HFC-FPGA platform for qualification as a safety-related device with respect to EMI/RFI emissions measurements and susceptibility test levels. EMI/RFI testing of the HFC-FPGA Qualification Test Specimen was performed in accordance with RG 1.180, Revision 1, using additional guidance from EPRI TR-107330 as applicable.

C.3. Equipment Tested

The equipment tested were the HFC-FPGA Qualification Test Specimen. Table 2 identifies the specific items that are part of the Qualification Test Specimen.

C.4. Sequence of Testing

The EMI/RFI Test was performed after completion of the Environmental Stress Test and had two phases. The first phase was during the period from 6/27/2016 to 9/26/2016, and the second phase was on 2/11/2017. Based on Table 10, the EMI/RFI Test includes the following tests:

- Configuration: Pre-Test Setup and Inspection
- Conducted Emission Test CE102
- Conducted Emission Test CE101
- Conducted Susceptibility Test CS114
- Radiated Susceptibility Test RS101
- Conducted Susceptibility Test CS115
- Conducted Susceptibility Test CS116
- Radiated Susceptibility Test RS103
- Radiated Emission Test RE101
- Conducted Susceptibility Test CS101
- Radiated Emission Test RE102
- Operability Test: Post EMI/RFI Test
- Prudency Test: Post EMI/RFI Test

C.5. Procedures

The following procedures were used during the prequalification test:

- TP901-302-03, VV0115 Qualification System EMI/RFI Test Procedure (Reference 17): Through this procedure, the HFC-FPGA Qualification Test Specimen received additional configuration in the test chamber for EMI/RFI Test. The performance of the HFC-FPGA Qualification Test Specimen was monitored throughout application of the EMI/RFI conditions.
- TP901-115-01, VV0115 Qualification Operability Test Procedure (Reference 13): This procedure includes a series of tests defined in Section 5.3 of EPRI TR-107330 that verified acceptable performance of the HFC-FPGA Qualification Test Specimen in accordance with the manufacturer's specifications for the HFC-FPGA platform. A complete repetition of this test procedure was performed as part of the Post EMI/RFI Test.
- TP901-115-02, VV0115 Qualification Prudency Test Procedure (Reference 14): This procedure includes a series of tests defined in Section 5.4 of EPRI TR-107330 that verified acceptable performance of the HFC-FPGA Qualification Test Specimen in accordance with the manufacturer's specifications for the HFC-FPGA platform. A complete repetition of this test procedure was performed as part of the Post EMI/RFI Test.

C.6. Test Specimen Mounting

The EMI/RFI Test was conducted by [
] for HF Controls. The Qualification Test Specimen and HPAT were disassembled at the HFC facility, transported to the [ ] facility. [ ] personnel were responsible for installing the Test Specimen in the test chamber, and then HFC personnel conducted a functional pre-test. General test setups for various EMI/RFI tests are shown in Figure 9 to Figure 18.

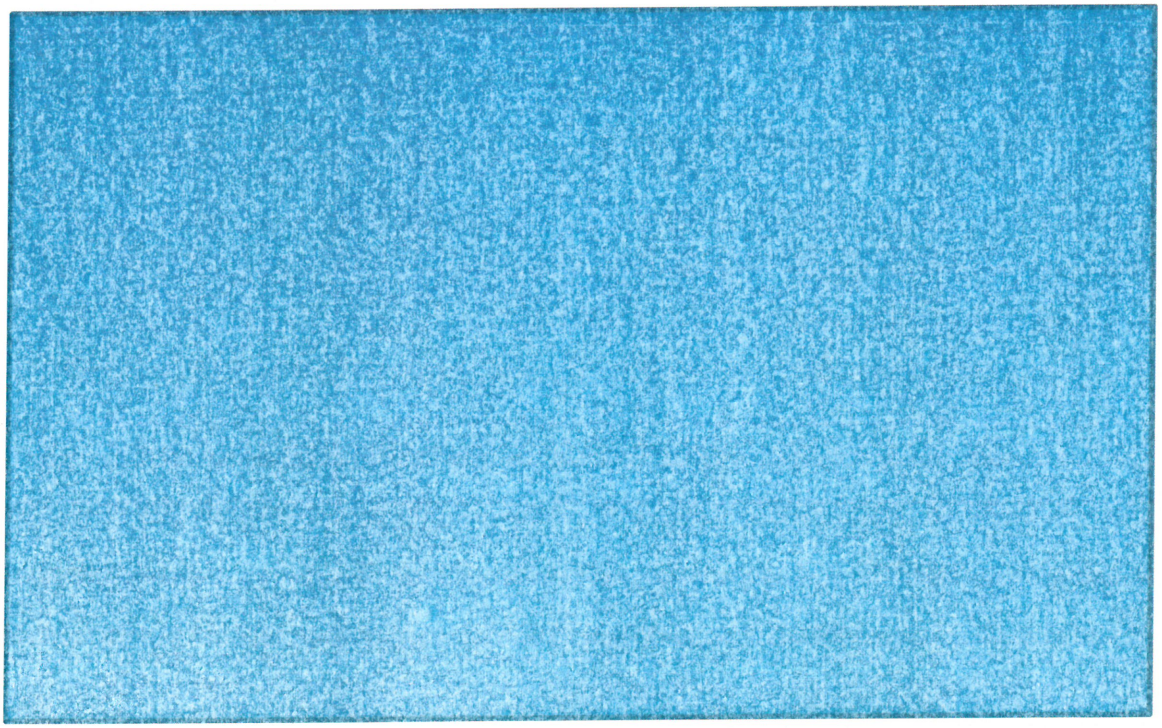


Figure 9. Line Test Setup for CE101

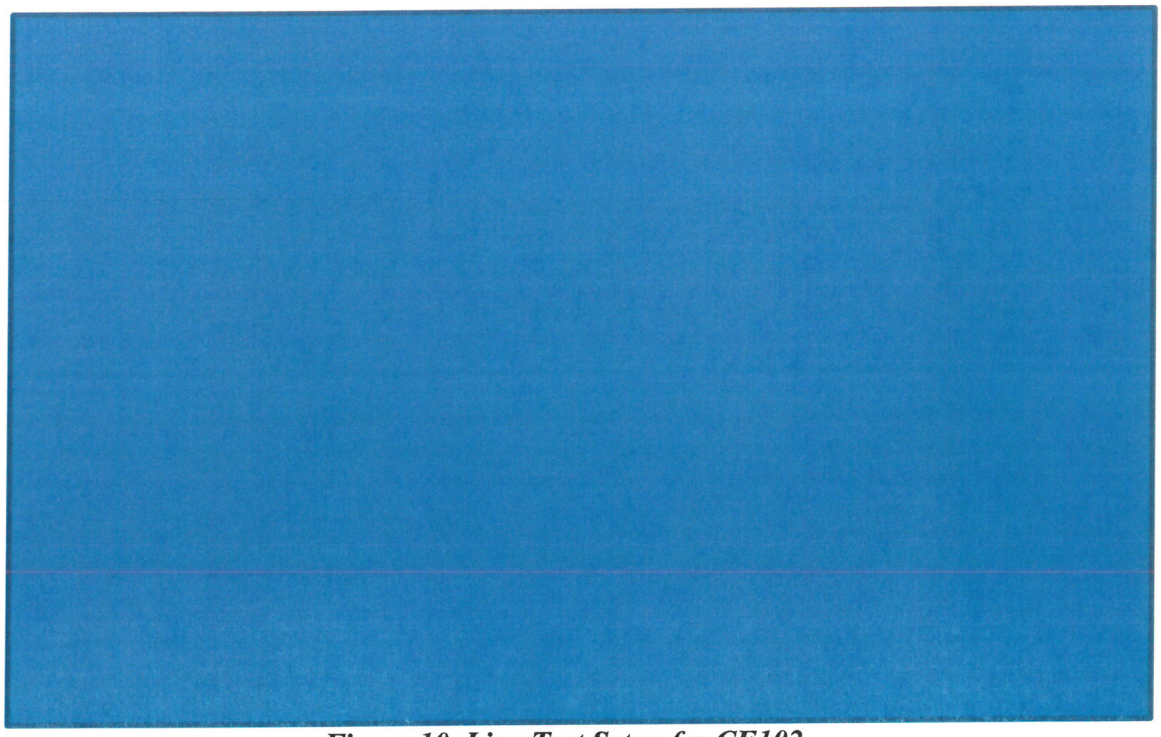


Figure 10. Line Test Setup for CE102

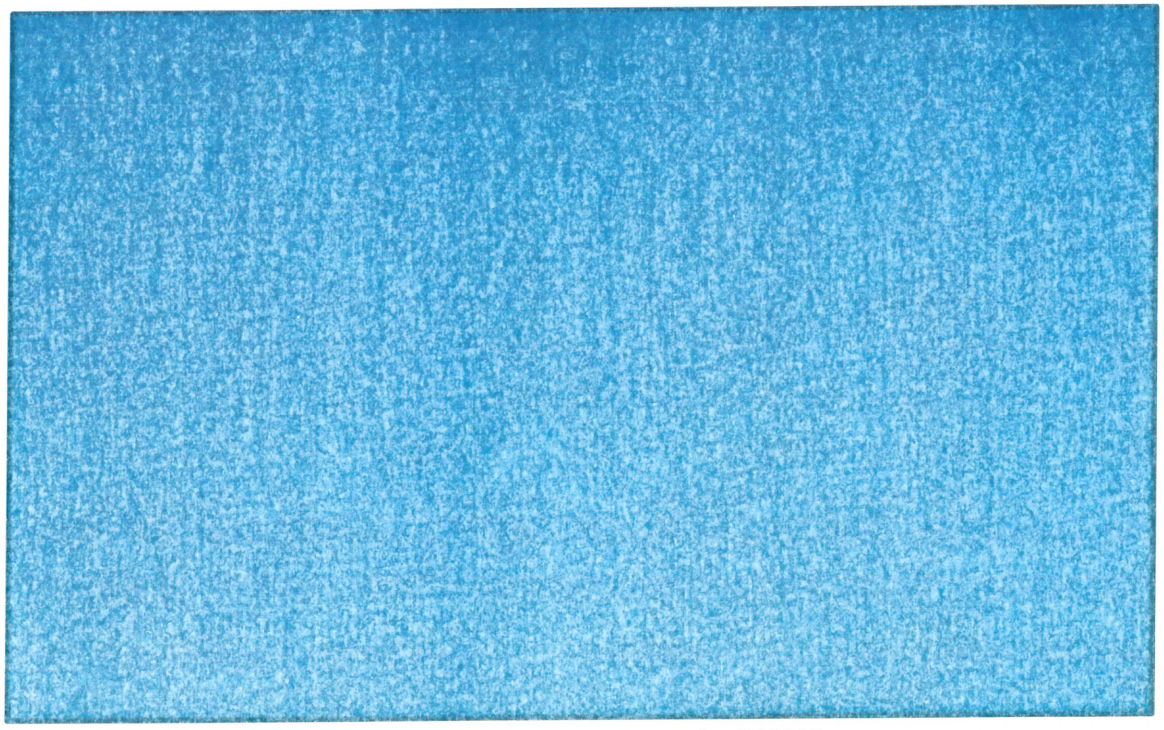


Figure 11. General Test Setup for RE101

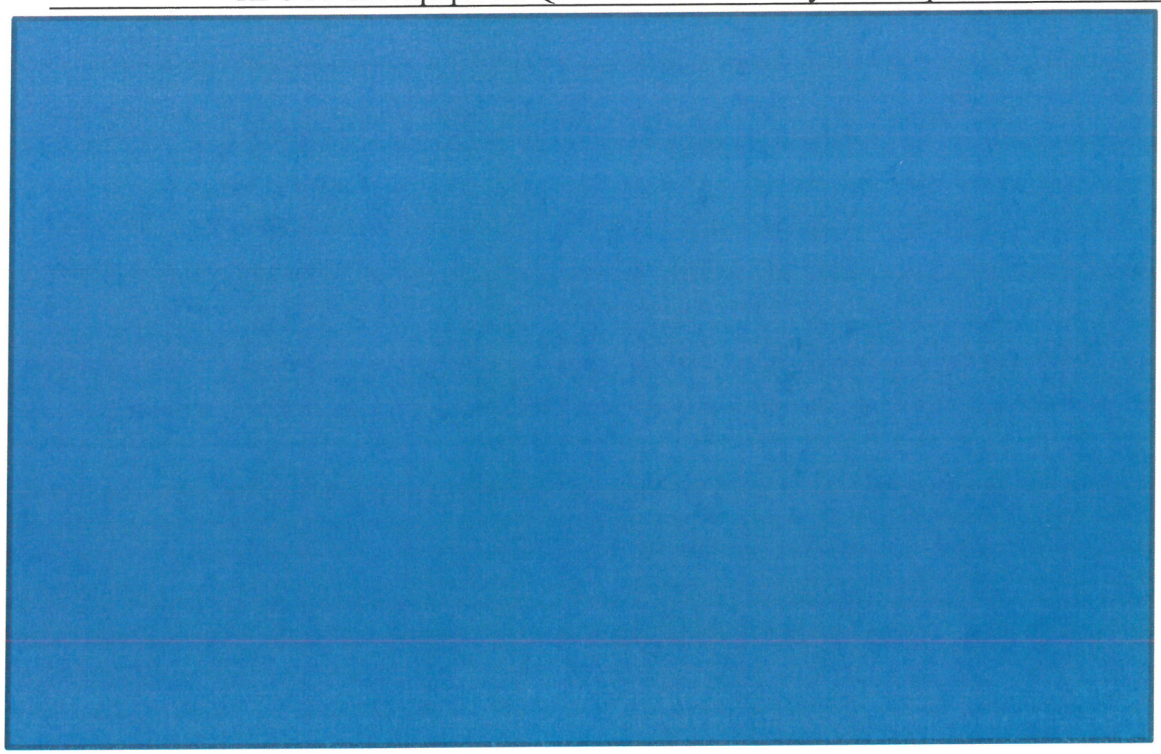


Figure 12. General Test Setup for RE102

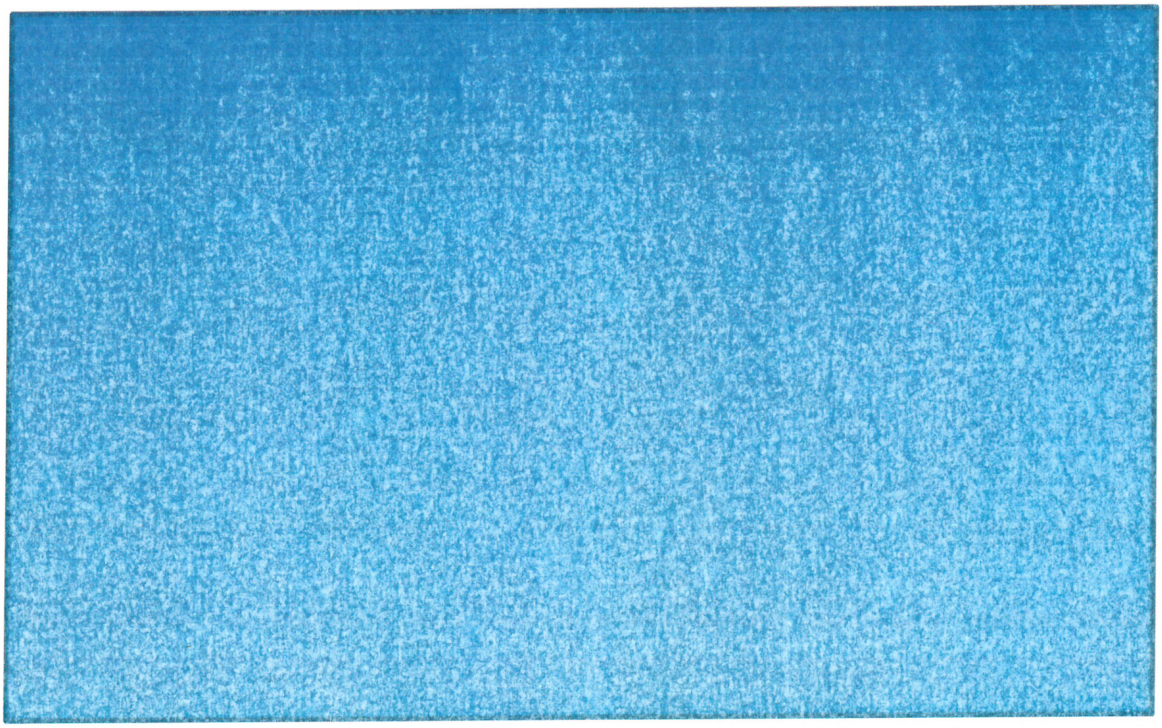


Figure 13. General Test Setup for CS101

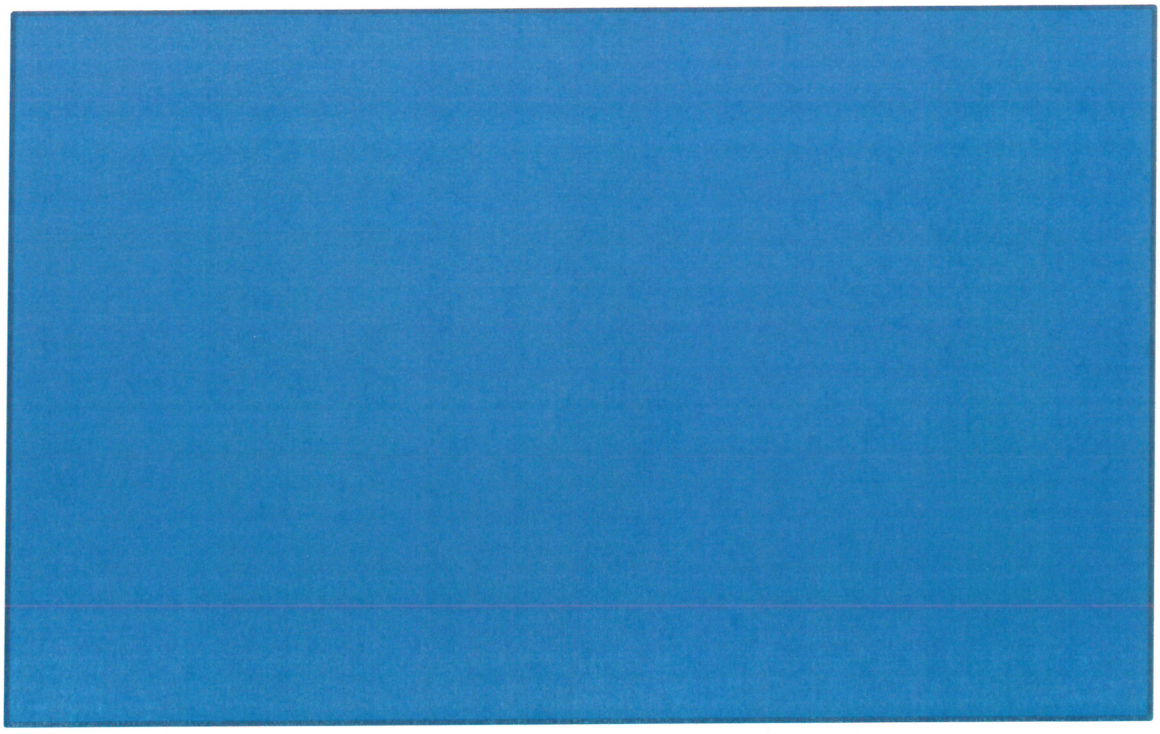


Figure 14. General Test Setup for CS114

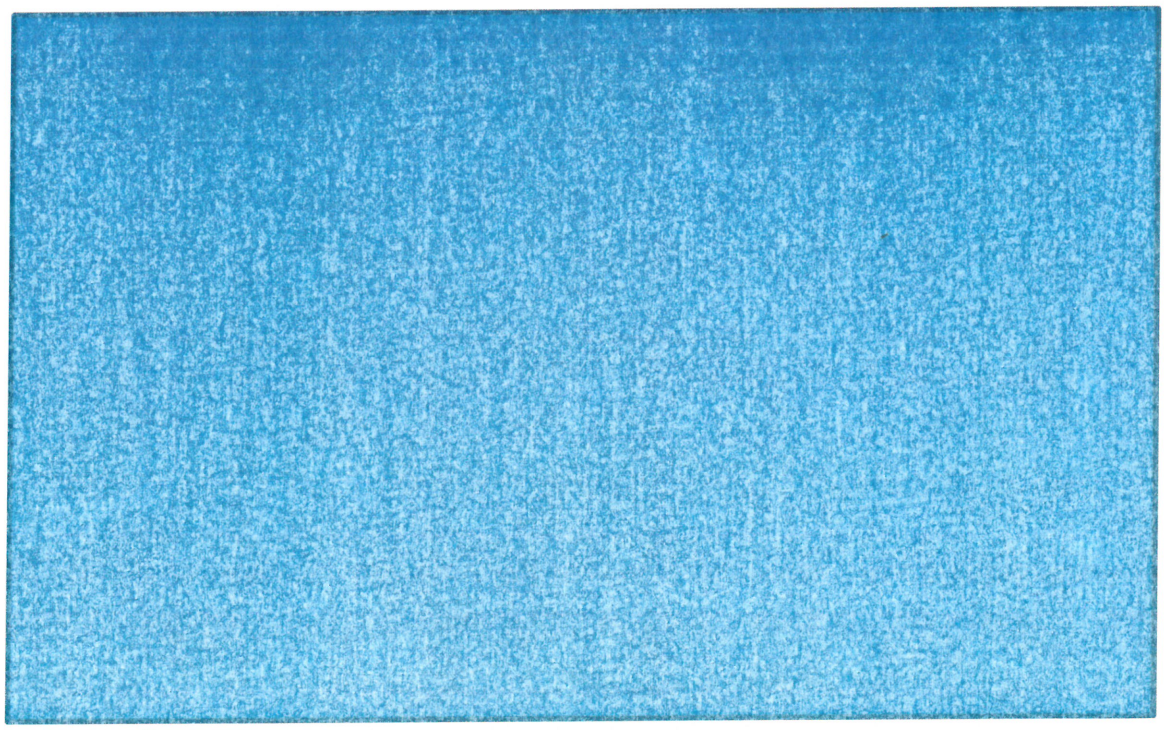


Figure 15. General Test Setup for CS115

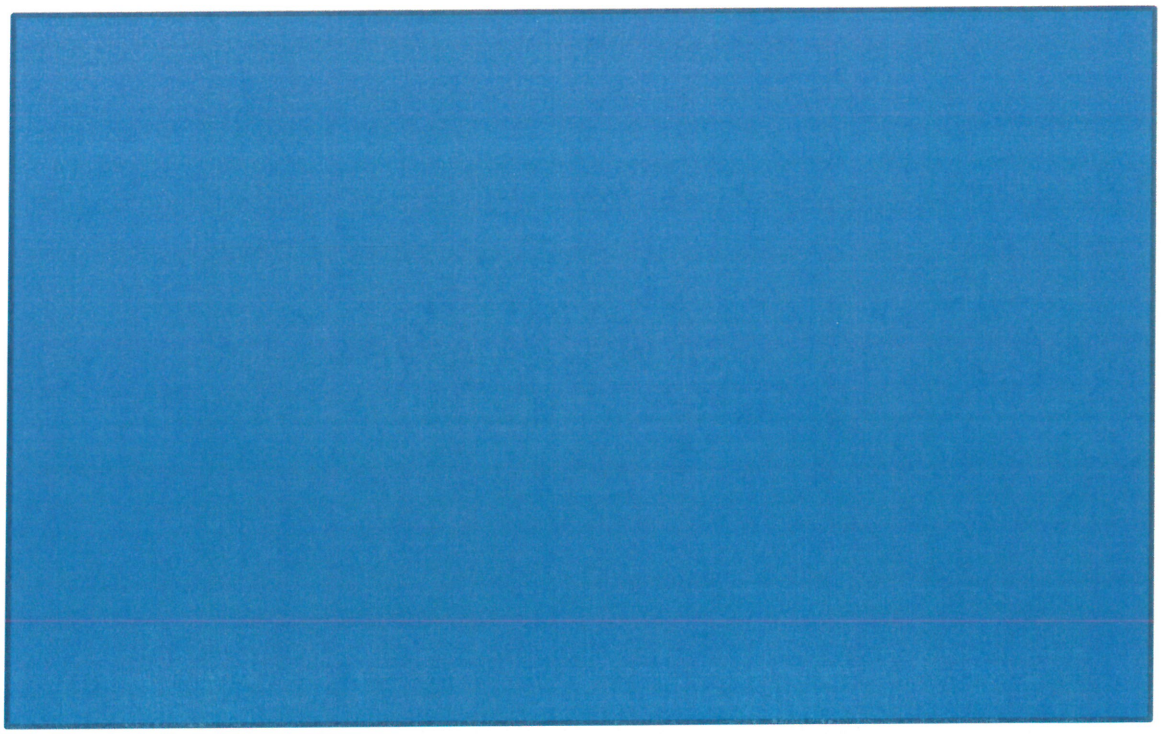


Figure 16. General Test Setup for CS116

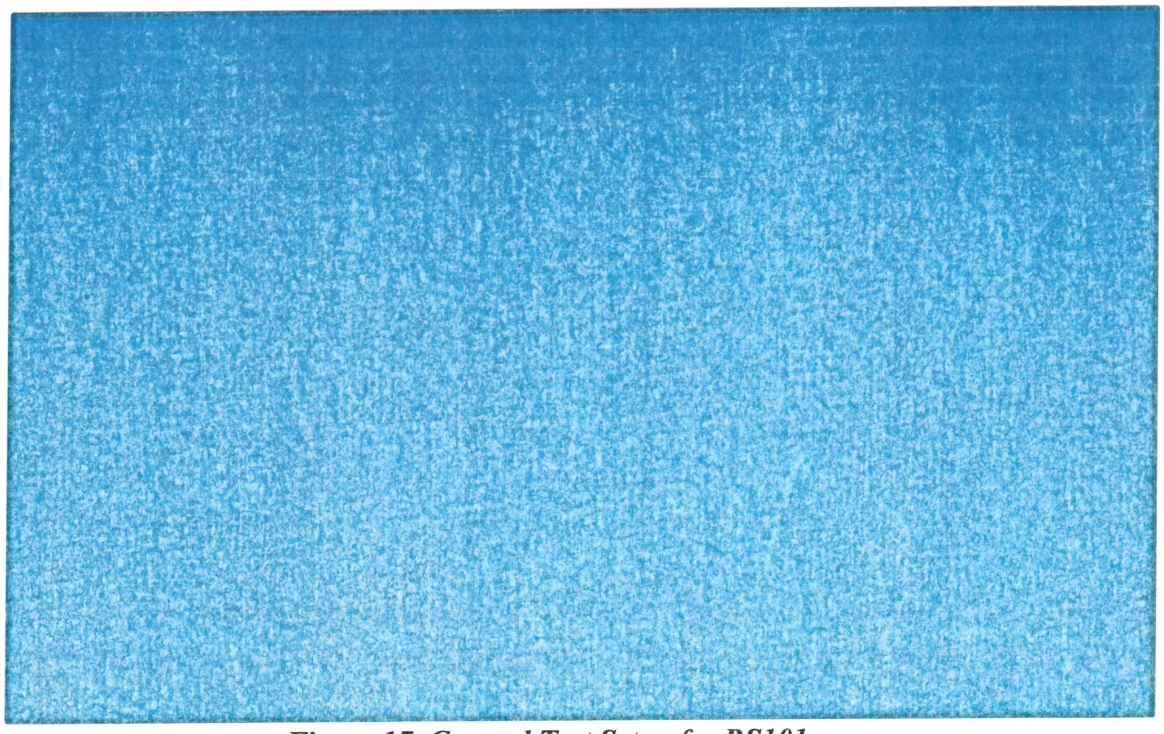


Figure 17. General Test Setup for RS101

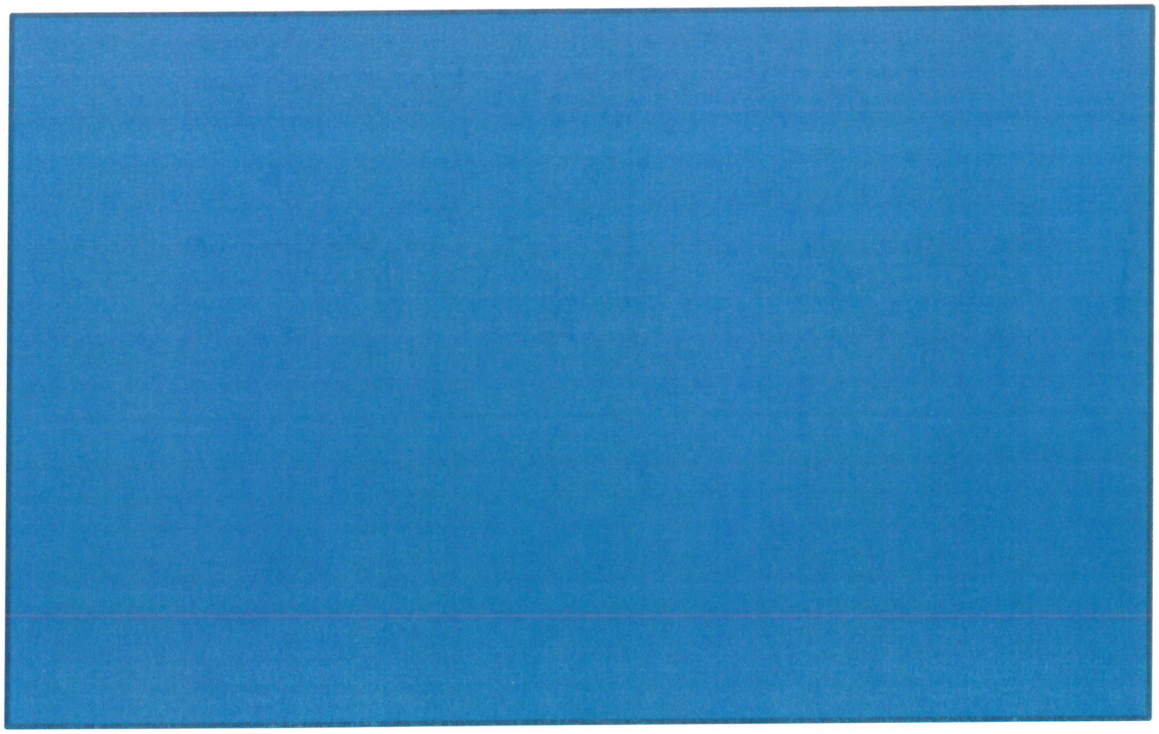


Figure 18. General Test Setup for RS103

C.7. Service Conditions

EMI/RFI qualification levels were determined from NRC RG 1.180. For radiated and susceptibility tests, the MIL-STD-461E methods were used to determine the appropriate testing levels. The purpose of these tests was to demonstrate that the components of the Qualification Test Specimen would not emit significant EMI/RFI noise that could interfere with the operation of nearby plant equipment, and that it was not susceptible to the level of EMI/RFI noise likely to be present in a plant environment.

- The emissions tests RE101, RE102, CE101, and CE102 were performed with the Automated Operability and Burst of Events tests running to simulate normal equipment activity.
- The susceptibility tests RS101, RS103, CS101, CS114, CS115, and CS116 were performed with the Automated Operability and Burst of Events tests running to simulate normal equipment activity.

C.8. Test Levels

The test levels (supply power and I/O signal and load levels) applied to the HFC-FPGA Test Specimen during the EMI/RFI Test were set as specified in corresponding test procedures (References 13, 14, and 17).

The specific EMI/RFI tests performed are shown in Table 10.

Table 10. EMI/RFI Test Requirements

Test Method	Sections	Frequency Range	Test Points
Conducted Emissions	CE101		
	CE102		
Radiated Emissions	RE101		
	RE102		
Conducted Susceptibility	CS101		
	CS114		
	CS115		
	CS116		
Radiated Susceptibility	RS101		
	RS103		

* HFC-FPGA System is a [ ] driven unit, for AC Application, MIL-STD-461E dictates that the frequency should start from the second harmonic of power supply frequency, which is 60Hz in this case.

C.9. Performance Monitoring

Performance monitoring of the HFC-FPGA Test Specimen during the EMI/RFI Test were set as specified in corresponding test procedures (References 13, 14, and 17).

C.10. Acceptance Criteria

Acceptance criteria for performance monitoring of the HFC-FPGA Test Specimen during the EMI/RFI Test were set as specified in corresponding test procedures (References 13, 14, and 17). They are summarized in Table 11.

Table 11. Acceptance Criteria for EMI/RFI Test

Test	Sub-Test	Acceptance Criteria
Configuration: Pre-Test Setup and Inspection	Output Level of Power Supplies Verification	
	Qualification Test Specimen Status Verification	
	Alarm Status Verification	
Conducted Emissions Test	CE101	
	CE102	

Test	Sub-Test	Acceptance Criteria
Radiated Emissions Test	RE101	
	RE102	
Conducted Susceptibility Test	CS101	
	CS114	
	CS115	
	CS116	
Radiated Susceptibility Test	RS101	

Test	Sub-Test	Acceptance Criteria
	RS103	
Operability Test: EMI/RFI Post Test	Accuracy Test (Automatic and Manual)	
	Response Time Test (Digital and Analog)	
	Discrete Input Operability Test	
	Discrete Output Operability Test	
	Communication Operability Test	
	Timer Test	
	Failure to Complete Scan Detection	

Test	Sub-Test	Acceptance Criteria
	Failover Test	
	Redundancy Test	
	Loss of Power Test	
Prudency Test: EMI/RFI Post Test	Burst of Events Test	
	Serial Port Failure / Noise Test	

C.11. Documentation

The following attachments in TR901-302-01 (Reference 9) were prepared as records by HFC to document the results of HFC-FPGA prequalification test:

- EMI/RFI Test
  - Attachment 13.18 Doosan PR037435 TP901-302-03 04 05 Test Report Rev. 1
  - Attachment 13.20 Completed record of TP901-302-03, VV0115 Qualification System EMI/RFI Test Procedure
- Post EMI/RFI Test
  - Attachment 13.23 Completed record of TP901-115-01, Operability Test Procedure for Post-EMI tests
  - Attachment 13.24 Completed record of TP901-115-02, Prudency Test Procedure for Post-EMI tests

C.12. Test Results

Detailed test results of the EMI/RFI Test were reported in TR901-302-01 (Reference 9), which are summarized in Table 12.

Table 12. Summary of EMI/RFI Test Results

Test	Sub-Test	Redmine or CR	Sub-Test Result	Overall Result
Configuration: Pre-Test Setup and Inspection	Output Level of Power Supplies Verification			
	Qualification Test Specimen Status Verification			
	Alarm Status Verification			
Conducted Emissions Test	CE101			
	CE102			
Radiated Emissions Test	RE101			
	RE102			
Conducted Susceptibility Test	CS101			
	CS114			
	CS115			
	CS116			
Radiated Susceptibility Test	RS101			
	RS103			

Test	Sub-Test	Redmine or CR	Sub-Test Result	Overall Result
Operability Test: EMI/RFI Post Test	Accuracy Test			
	Response Time Test			
	Discrete Input Operability Test			
	Discrete Output Operability Test			
	Communication Operability Test			
	Timer Test			
	Failure to Complete Scan Detection			
	Redundancy Test			
	Failover Test			
	Loss of Power Test			
Prudency Test: EMI/RFI Post Test	Burst of Events Test			
	Serial Port Failure / Noise Test			

C.13. Resolution of Test Discrepancies

HFC uses a Condition Report Microsoft Access Database and a Redmine project management and issue tracking tool to record all the issues encountered during Equipment Qualification.

During EMI/RFI Test, below issues were tracked and resolved:

Redmine issue 687, created on 7/22/2016. During analysis of EMI/RFI data, it was discovered that LDS1 board 1 timer test SOE points see minutes transition backwards instead of forward. This seems to be an issue with incrementing of SOE minute counter. [

]

Redmine issue 714, created on 8/01/2016. RE102 failed between 25 MHz to 30 MHz. After investigation with a sniffer antenna, the only modification that allowed the system to pass is to place a grounded metal plane between antenna and cables. This issue is considered resolved.

Redmine issue 639, created on 7/05/2016. During CS114, the 24Vdc bundle fails at 17 MHz, system lost power. Same issue exists at 13 MHz and 12.2 MHz. Investigate concluded that 24Vdc bundle is outside of the scope of this qualification test. This issue is considered resolved.

Condition Report CR2016-0379, created on 10/10/2016. RE102 did not pass initially. Investigation indicates that termination resistors are needed for FCPU/FCPUX to support F-link and G-link communication. This CR is generated to capture the issue and it was resolved by [ ].

Condition Report CR2016-0361, created on 9/29/2016, five red-line changes to TP901-115-03, EMI/RFI Test Procedure, per errors discovered in VV0115 EMI/RFI testing. [

]

Appendix D. Qualification Test Summary – Electrostatic Discharge Test

D.1. Purpose

This test summary describes the ESD Test performed on the HFC-FPGA Qualification Test Specimen. ESD Testing of the HFC-FPGA Qualification Test Specimen was performed as part of qualification testing to demonstrate compliance with the applicable ESD requirements of EPRI TR-107330, Section 4.3.8.

D.2. Objective

The objective of ESD Test was to demonstrate the suitability of the HFC-FPGA platform for qualification as a safety-related device with respect to ESD withstand level. EPRI TR-107330, Section 4.3.8, requires that the test specimen under qualification be tested for ESD withstand capability in accordance with the requirements of EPRI TR-102323, Revision 1. In accordance with EPRI TR-102323, Revision 1, the specific ESD Test to be performed is IEC 61000-4-2 “Electromagnetic Compatibility (EMC), Part 4-2: Testing and Measurement Techniques, Electrostatic Discharge Immunity Test”.

D.3. Equipment Tested

The equipment tested were the HFC-FPGA Qualification Test Specimen. Table 2 identifies the specific items that are part of the Qualification Test Specimen.

D.4. Sequence of Testing

The ESD Test was performed along with the EMI/RFI Test and had two phases. The first phase was during the period from 9/7/2016 to 9/12/2016, and the second phase was on 2/11/2017. The ESD Test includes the following tests:

- Configuration: Pre-Test Setup and Inspection
- ESD Test
- ESD Post Test

D.5. Procedures

The following procedures were used during the prequalification test:

- TP901-302-05, VV0115 Qualification System ESD Test Procedure (Reference 18): Through this procedure, the HFC-FPGA Qualification Test Specimen received additional configuration in the test chamber for ESD Test. The performance of the HFC-FPGA Qualification Test Specimen was monitored throughout application of the ESD conditions.

D.6. Test Specimen Mounting

The ESD Test was conducted by [ ] for HF Controls. The HFC-FPGA Qualification Test Specimen for EMI/RFI Test was used for the ESD Test with the required ESD test setup. [ ] personnel were responsible for installing the Test Specimen in the test chamber, and then HFC personnel conducted a functional pre-test. General test setups for various ESD test locations are shown in Figure 19 to Figure 26.

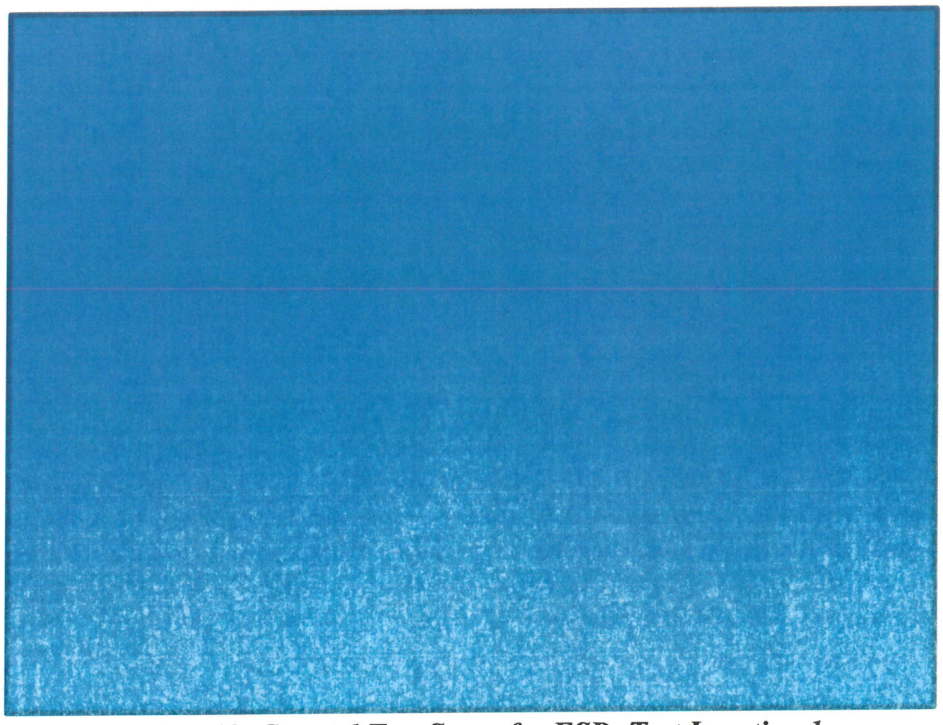


Figure 19. General Test Setup for ESD, Test Location 1

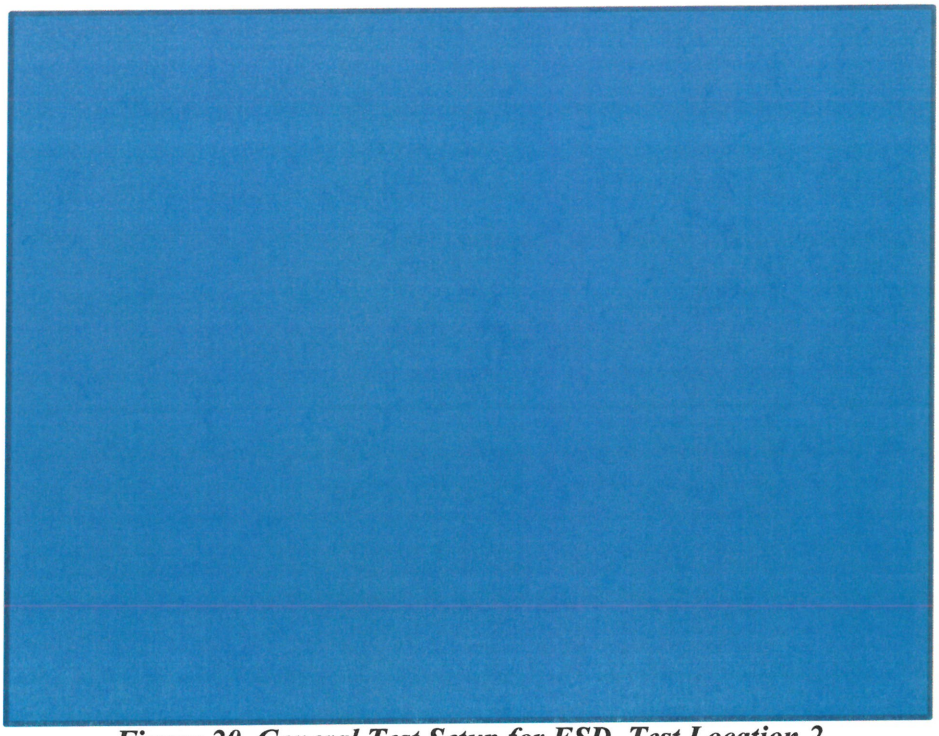


Figure 20. General Test Setup for ESD, Test Location 2

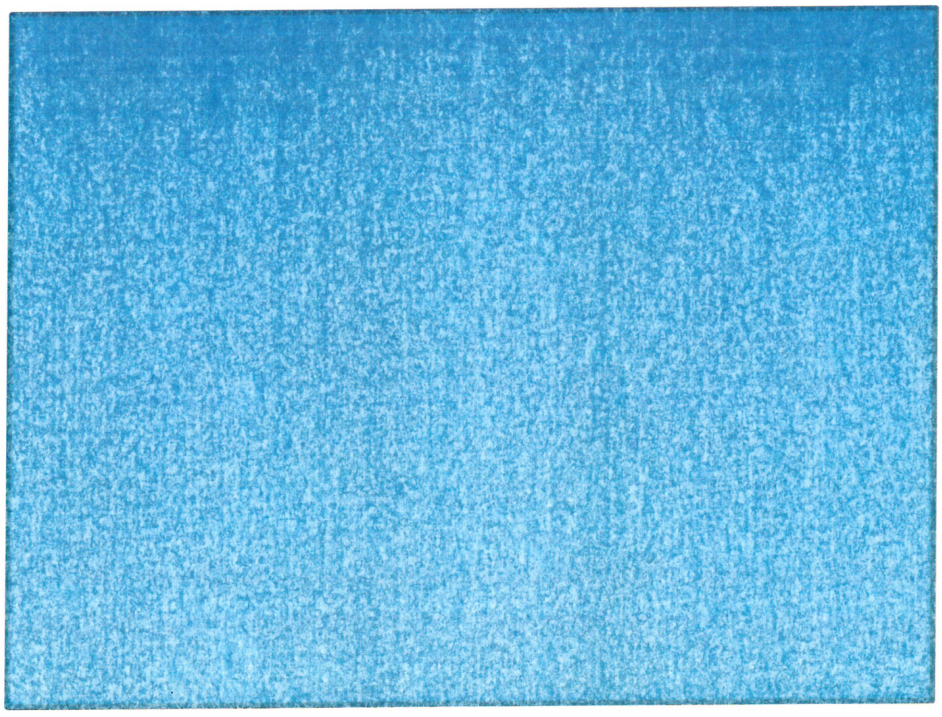


Figure 21. General Test Setup for ESD, Test Location 3

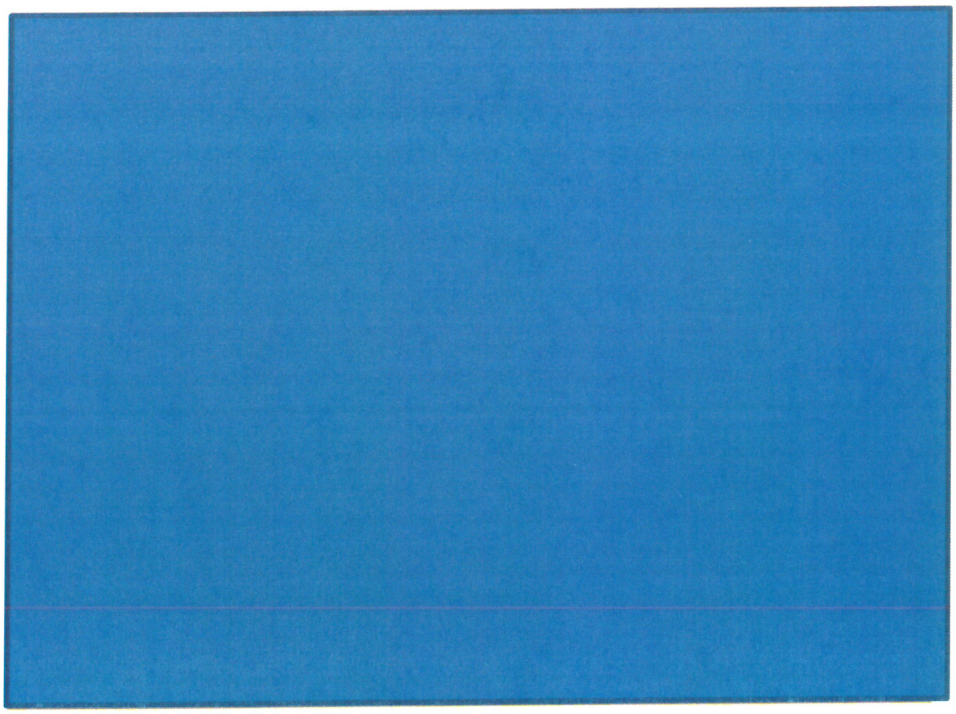


Figure 22. General Test Setup for ESD, Test Location 4

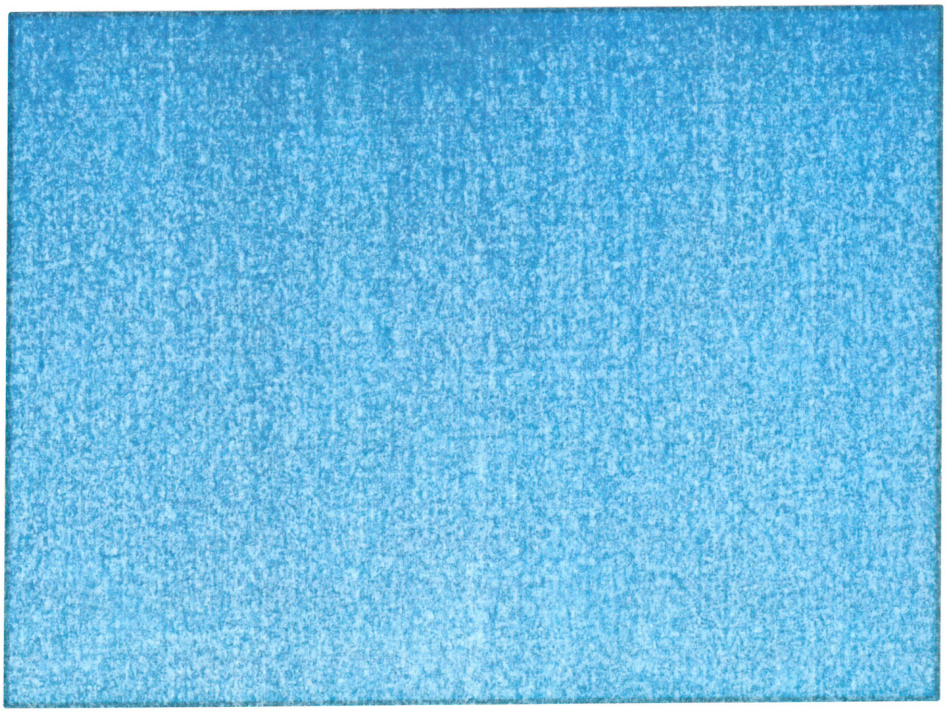


Figure 23. General Test Setup for ESD, Test Location 5

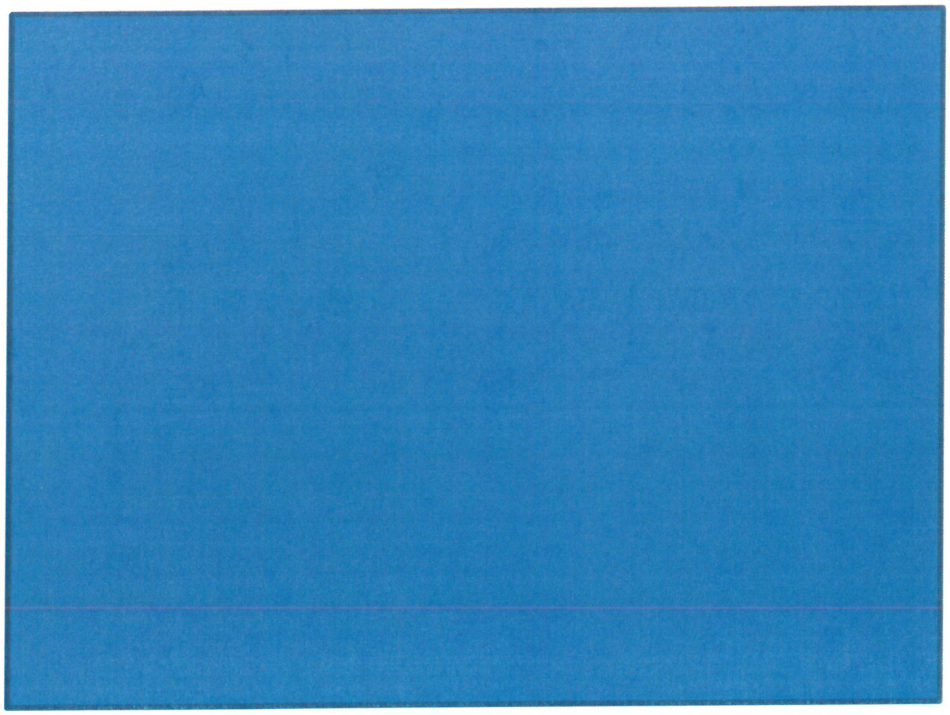


Figure 24. General Test Setup for ESD, Test Location 6

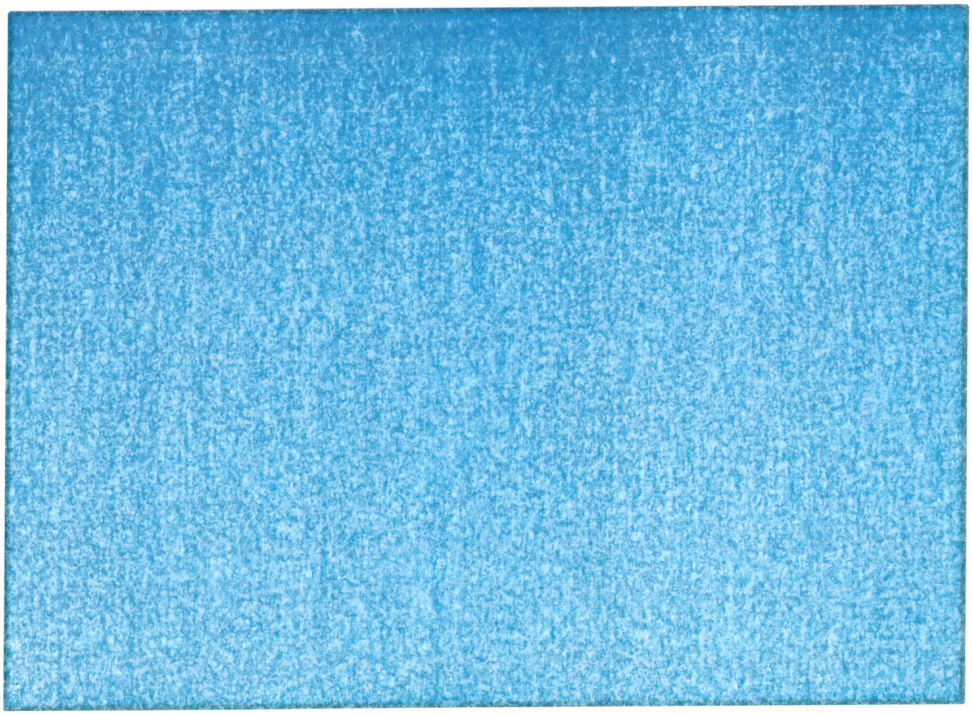


Figure 25. General Test Setup for ESD, Test Location 7

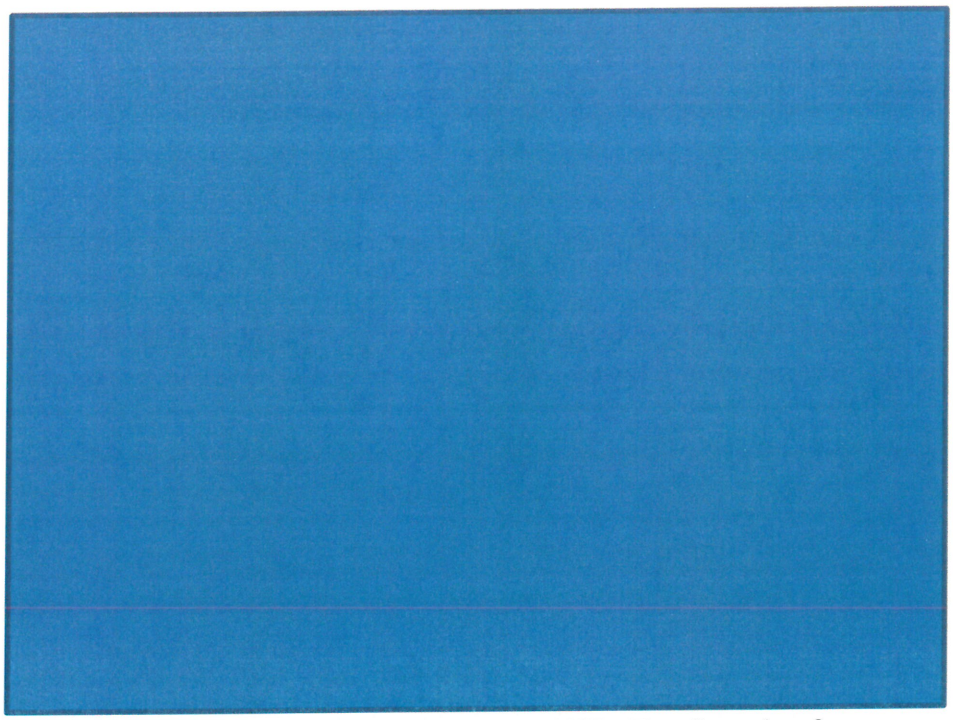


Figure 26. General Test Setup for ESD, Test Location 8

D.7. Service Conditions

Electrostatic Discharge Withstand qualification levels were determined from IEC 61000-4-2. This standard was selected to determine the appropriate test signal levels and testing methodology to demonstrate the ability of the test specimen to perform without significant disruption when exposed to ESD signals likely to be found in a generic industrial environment.

Components of an HFC-FPGA system may be installed in an electrical equipment room as well as at various locations near the field equipment under control. In either case, the potential exists for exposure of sensitive electronic components to high voltage ESD. This test subjected each component of the HFC-FPGA Test Specimen to simulated ESD pulses to establish their capability to withstand such discharges without disabling or disrupting normal operation. Detailed requirements for ESD immunity were defined by IEC 64000-4-2:

- Contact discharge levels were 8 kV, applied ten times at a positive polarity and ten times at a negative polarity to each test point.
- Air discharge levels were 15 kV, applied ten times at a positive polarity and ten times at a negative polarity to each test point.
- All HFC-FPGA module toggle switches and bezels were subjected to ESD testing.
- Points on the VV0115 Test Specimen found to be likely contact points such as power supply switches, tie bars, and mounting screws were subjected to ESD testing.

D.8. Test Levels

The test levels (supply power and I/O signal and load levels) applied to the HFC-FPGA Test Specimen during the ESD Test were set as specified in corresponding test procedures (References 13, 14, and 18).

The specific ESD tests performed are shown in Table 13.

Table 13. ESD Test Requirements

Test Method	Sections	Frequency Range	Test Points
ESD	IEC 61000-4-2	Surge Pulse	Case and Cables

D.9. Performance Monitoring

Performance monitoring of the HFC-FPGA Test Specimen during the ESD Test were set as specified in corresponding test procedures (References 13, 14, and 18).

D.10. Acceptance Criteria

Acceptance criteria for performance monitoring of the HFC-FPGA Test Specimen during the ESD Test were set as specified in corresponding test procedures (References 13, 14, and 18). They are summarized in Table 14.

Table 14. Acceptance Criteria for ESD Test

Test	Sub-Test	Acceptance Criteria
Configuration: Pre-Test Setup and Inspection	Output Level of Power Supplies Verification	[redacted]
	Qualification Test Specimen Status Verification	
	Alarm Status Verification	
ESD Test	N/A	

Test	Sub-Test	Acceptance Criteria
ESD Post Test	N/A	

D.11. Documentation

The following attachments in TR901-302-01 (Reference 9) were prepared as records by HFC to document the results of HFC-FPGA prequalification test:

- ESD Test
  - Attachment 13.18 Doosan PR037435 TP901-302-03 04 05 Test Report Rev. 1
  - Attachment 13.22 Completed record of TP901-302-05, VV0115 Qualification System ESD Test Procedure

D.12. Test Results

Detailed test results of the ESD Test were reported in TR901-302-01 (Reference 9), which are summarized in Table 15.

Table 15. Summary of ESD Test Results

Test	Sub-Test	Redmine or CR	Sub-Test Result	Overall Result
Configuration: Pre-Test Setup and Inspection	Output Level of Power Supplies Verification			
	Qualification Test Specimen Status Verification			
	Alarm Status Verification			
ESD Test	N/A			
ESD Post Test	N/A			

D.13. Resolution of Test Discrepancies

HFC uses a Condition Report Microsoft Access Database and a Redmine project management and issue tracking tool to record all the issues encountered during Equipment Qualification.

During Electrostatic Discharge Test, below issues were tracked and resolved:

Condition Report CR2016-0405, created 10/26/2016. FPC08 had a temporary failure during 8kV discharge to the center of the bezel. Failure caused temporary loss in communication with the Test Specimen. After investigation, it was determined FPC08 isn't grounded properly. A field wire was needed to attach the bezel to chassis ground, in order for the 8kV discharge to the center of the bezel to pass ESD test without impacting the card performance. This CR is considered to be resolved.

Redmine issue 723, created on 9/12/2016. In addition to CR2016-0405, FOT06 experienced temporary loss of function when corner mounting screws undergo 8kV discharge. But since FOT06 are used in redundant pairs, one temporary loss of function did not cause any loss of communication or function of the system as a whole. This issue is considered to be resolved.

Appendix E. Qualification Test Summary – Surge Withstand Test

E.1. Purpose

This test summary describes the Surge Withstand Test performed on the HFC-FPGA Qualification Test Specimen. Surge Withstand Testing of the HFC-FPGA Qualification Test Specimen was performed as part of qualification testing to demonstrate compliance with the applicable Surge Withstand requirements of RG (RG) 1.180, Revision 1.

E.2. Objective

The objective of Surge Withstand Testing was to demonstrate the suitability of the HFC-FPGA platform for qualification as a safety-related device with respect to Surge Withstand levels. The Surge Withstand testing of the HFC-FPGA Qualification Test Specimen will be performed in accordance with RG 1.180, Revision 1, using additional guidance from EPRI TR-107330, as applicable. The specific Surge Withstand Tests performed include:

- IEC 61000-4-4, “Electromagnetic Compatibility (EMC), Part 4-4: Testing and Measurement Techniques, Electrical Fast Transient/Burst Immunity Test”
- IEC 61000-4-5, “Electromagnetic Compatibility (EMC), Part 4-5: Testing and Measurement Techniques, Surge Immunity Test”
- IEC 61000-4-12, “Electromagnetic Compatibility (EMC), Part 4-12: Testing and Measurement Techniques, Oscillatory Waves Immunity Test”.

E.3. Equipment Tested

The equipment tested were the HFC-FPGA Qualification Test Specimen. Table 2 identifies the specific items that are part of the Qualification Test Specimen.

E.4. Sequence of Testing

The Surge Withstand Test was performed along with the EMI/RFI Test during the period from 8/2/2016 to 9/9/2016. The Surge Withstand Test includes the following tests:

- Configuration: Pre-Test Setup and Inspection
- Electrical Fast Transient (EFT) Test
- Combination Waveform Test
- Ring Wave Test

E.5. Procedures

The following procedures were used during the prequalification test:

- TP901-302-04, VV0115 Qualification System Surge Withstand Test Procedure (Reference 19): Through this procedure, the HFC-FPGA Qualification Test Specimen received additional configuration in the test chamber for Surge

Withstand Test. The performance of the HFC-FPGA Qualification Test Specimen was monitored throughout application of the Surge Withstand conditions.

E.6. Test Specimen Mounting

The Surge Withstand Test was conducted by [ ] for HF Controls. The HFC-FPGA Qualification Test Specimen for EMI/RFI Test was used for the Surge Withstand Test with the required Surge Withstand test setup. [ ] personnel were responsible for installing the Test Specimen in the test chamber, and then HFC personnel conducted a functional pre-test. General test setups for various Surge Withstand test locations are shown in Figure 27 to Figure 32.

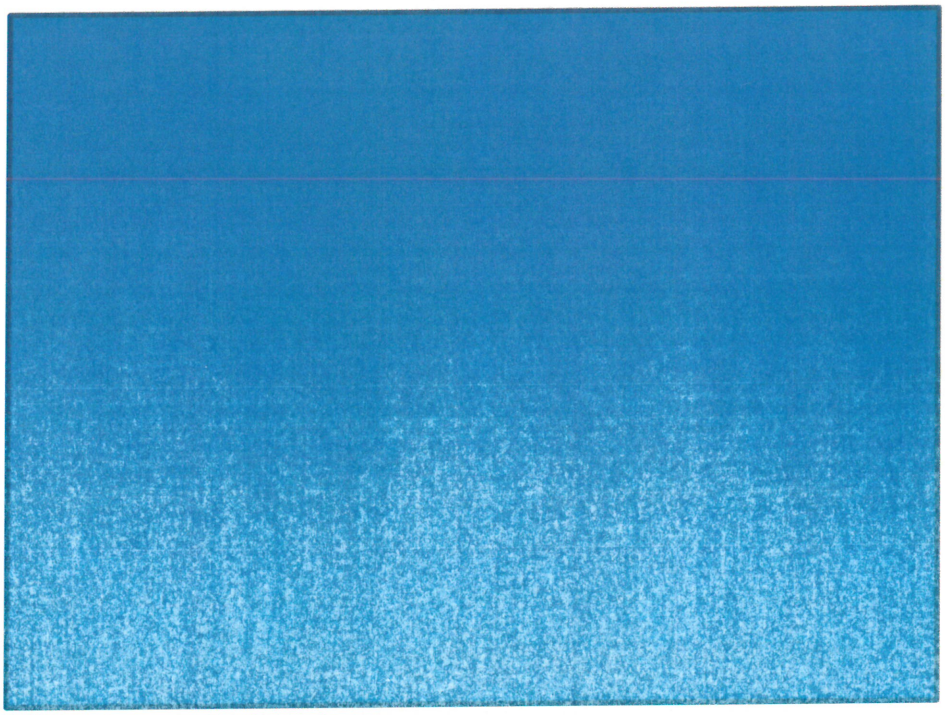


Figure 27. General Test Setup for EFT, AC Power Input

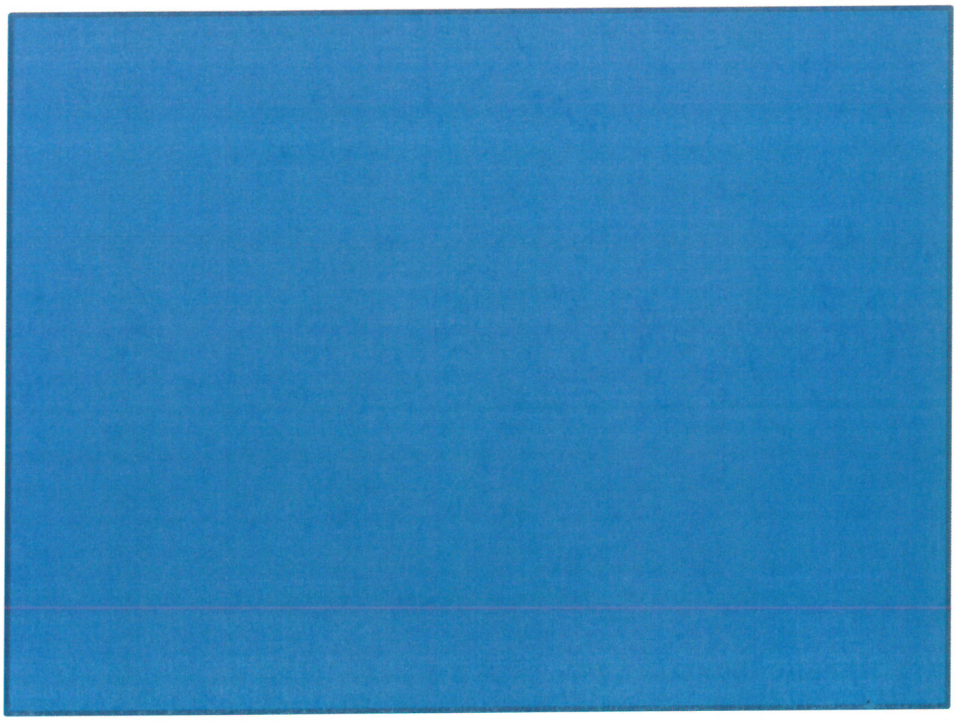


Figure 28. General Test Setup for EFT, J2 Signal Bundle

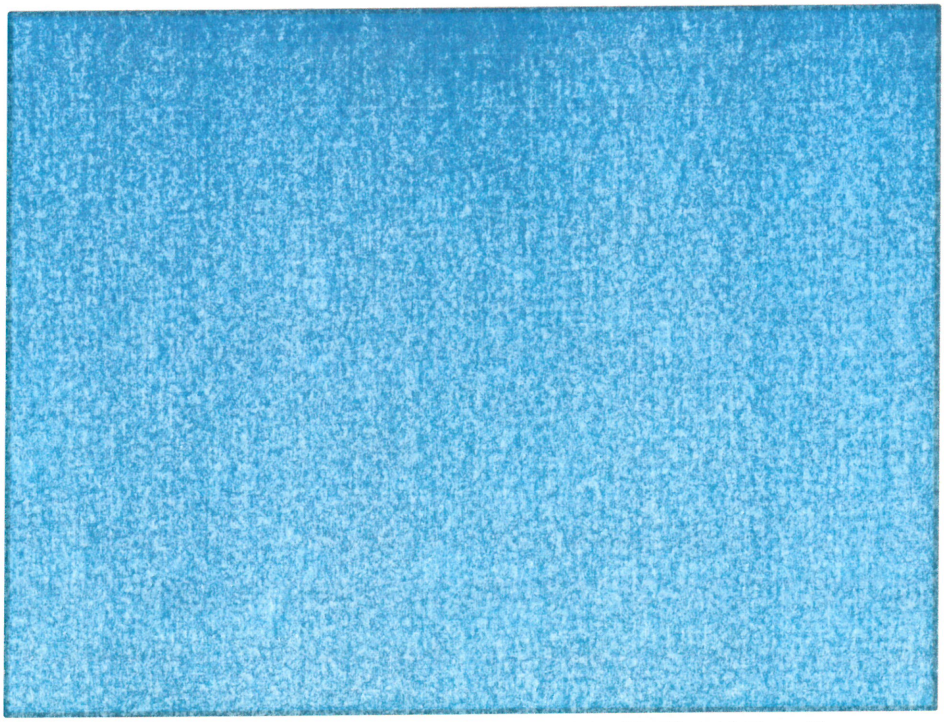


Figure 29. General Test Setup for EFT, J3 Signal Bundle

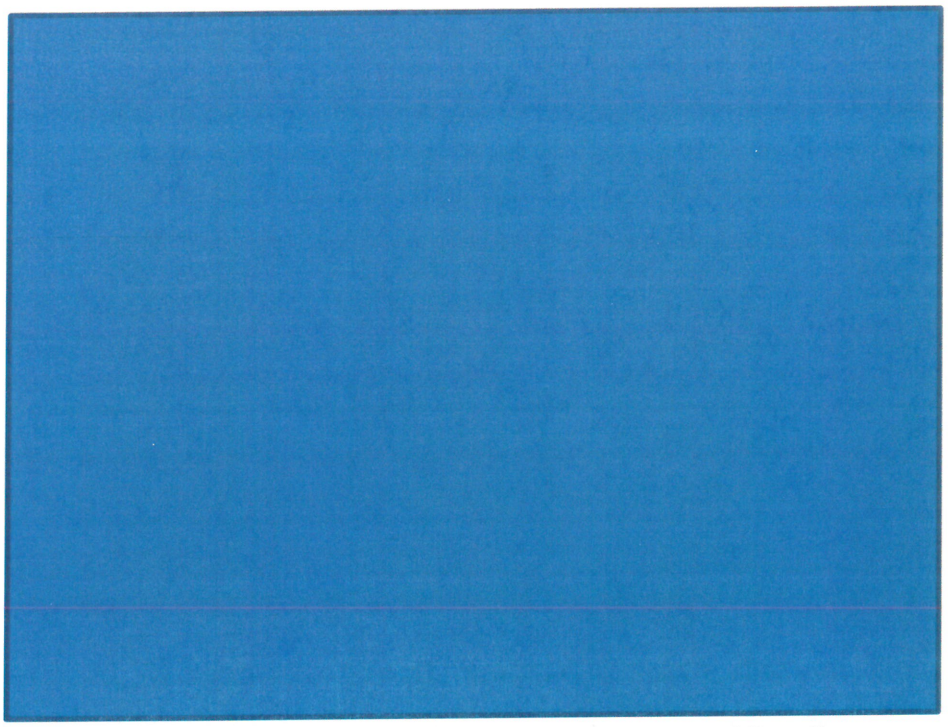


Figure 30. General Test Setup for EFT, J4 Signal Bundle

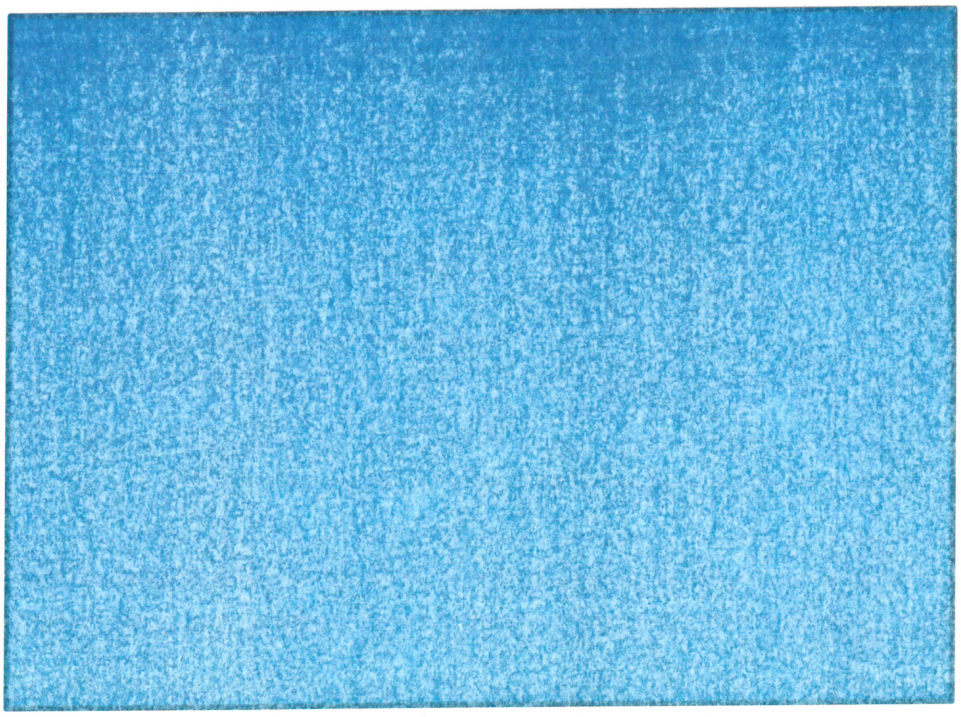


Figure 31. General Test Setup for Combination Waveform, AC Power Input

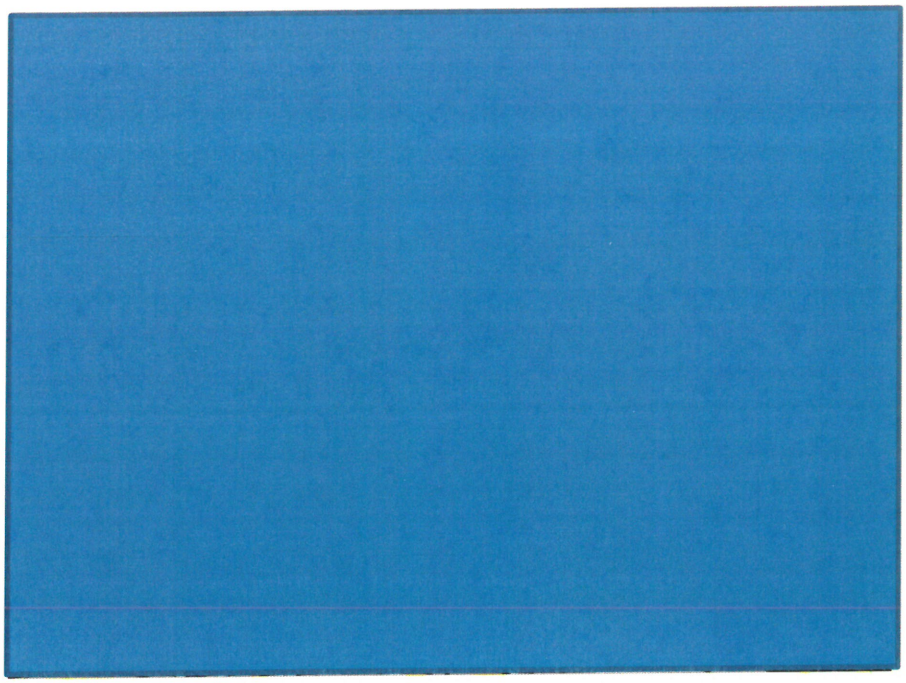


Figure 32. General Test Setup for Ring Waveform, AC Power Input

E.7. Service Conditions

Surge Withstand qualification levels were determined from NRC RG 1.180. The IEC method for Surge Withstand Capability was used to determine the appropriate test signal levels and waveforms. The purpose of these tests was to demonstrate that the components of the test specimen would perform without significant disruption from the injection of these waveforms.

Power, electrical I/O signal lines, and hardwired communication cables may be exposed to high amplitude transient signals in the locations where control system hardware may be installed. These locations include an electrical equipment room and various other locations near the equipment under control. The test covered by this document injects a large amplitude surge waveform at specified points of the Test Specimen. The purpose of this test was to demonstrate that Test Specimen performance characteristics remain within acceptable limits during and after exposure to such discharges. The Test Specimen was powered on and running the TSAP and automated Operability and Prudency tests when the test pulses are being applied to specific circuits in accordance with RG 1.180 Section 5. Four tests were conducted:

- Ring Wave per IEC 61000-4-12, Category B at 4 kV applied to 120 VAC input power.
- Combination Wave per IEC 61000-4-5, Category B at 4 kV / 2 kV applied to 120 VAC input power.
- EFT per IEC 61000-4-4, Category B at 4 kV applied to 120 VAC input power.
- EFT per IEC 61000-4-4 at 500 V, coupled into signal lines.

E.8. Test Levels

The test levels (supply power and I/O signal and load levels) applied to the HFC-FPGA Test Specimen during the Surge Withstand Test were set as specified in corresponding test procedures (References 13, 14, and 19).

The specific ESD tests performed are shown in Table 16.

Table 16. Surge Withstand Test Requirements

Test Method	Sections	Frequency Range	Test Points
Fast Transient	IEC 61000-4-4	Surge Pulse	Power Leads and Cables
Combination Waveform	IEC 61000-4-5	Surge Pulse	Power Leads and Cables
Ring Wave	IEC 610090-4-12	Surge Pulse	Power Leads and Cables

Table 17 presents a summary of the surge strength characteristics specified by the IEEE Std C62.41-1991.

Table 17. Surge Withstand Pulse Levels

Waveform	Category B – Low Exposure	Category B – Medium Exposure
EFT		
Combination Wave		
Ring Wave		

E.9. Performance Monitoring

Performance monitoring of the HFC-FPGA Test Specimen during the Surge Withstand Test were set as specified in corresponding test procedures (References 13, 14, and 19).

E.10. Acceptance Criteria

Acceptance criteria for performance monitoring of the HFC-FPGA Test Specimen during the Surge Withstand Test were set as specified in corresponding test procedures (References 13, 14, and 19). They are summarized in Table 18.

Table 18. Acceptance Criteria for Surge Withstand Test

Test	Sub-Test	Acceptance Criteria
Configuration: Pre-Test Setup and Inspection	Output Level of Power Supplies Verification	

Test	Sub-Test	Acceptance Criteria
	Qualification Test Specimen Status Verification	
	Alarm Status Verification	
EFT Test	N/A	
Combination Wave Test	N/A	

Test	Sub-Test	Acceptance Criteria
Ring Wave Test	N/A	

E.11. Documentation

The following attachments in TR901-302-01 (Reference 9) were prepared as records by HFC to document the results of HFC-FPGA prequalification test:

- Surge Withstand Test
  - Attachment 13.18 Doosan PR037435 TP901-302-03 04 05 Test Report Rev. 1
  - Attachment 13.21 Completed record of TP901-302-04, VV0115 Qualification System Surge Withstand Test Procedure

E.12. Test Results

Detailed test results of the Surge Withstand Test were reported in TR901-302-01 (Reference 9), which are summarized in Table 19.

Table 19. Summary of Surge Withstand Test Results

Test	Sub-Test	Redmine or CR	Sub-Test Result	Overall Result
Configuration : Pre-Test Setup and Inspection	Output Level of Power Supplies Verification			
	Qualification Test Specimen Status Verification			
	Alarm Status Verification			
EFT Test	N/A			
Combination Wave Test	N/A			
Ring Wave Test	N/A			

E.13. Resolution of Test Discrepancies

HFC uses a Condition Report Microsoft Access Database and a Redmine project management and issue tracking tool to record all the issues encountered during Equipment Qualification.

During Surge Withstand Test, below issues were tracked and resolved:

Redmine issue 715, created on 8/02/2016. An Alarm was detected on remote 3 during EFT testing (3, FL,1074). After troubleshooting, it was determined to be an error in VV0115 master database, database has been corrected by 8/12/2016.
Surge withstand test passed after HFC separated AC/DC power into bundles, added grounding to shielded 120 VAC cable. This issue is considered resolved.

Appendix F. Qualification Test Summary – Seismic Test

F.1. Purpose

This test summary describes the Seismic Test performed on the HFC-FPGA Qualification Test Specimen. Seismic Testing of the HFC-FPGA Qualification Test Specimen was performed as part of qualification testing to demonstrate compliance with RG 1.100 and IEEE Standard 344-1987. The purpose of this test was to demonstrate that the physical components on the PCB assemblies, mechanical junctions, and cable assemblies remain in place and operational during and after application of significant inertial forces. It used guidance from EPRI TR-107330 which is compliant with these requirements.

F.2. Objective

The objective of Seismic Testing was to demonstrate the suitability of the HFC-FPGA platform for qualification as a Category 1 seismic device based on seismic withstand testing performed on the HFC-FPGA Qualification Test Specimen in accordance with RG 1.100 and IEEE 344-1987. Section 4.3.9 of EPRI TR-107330 defines the recommended seismic test levels the test specimen is expected to withstand (i.e., the test specimen must continue to meet the manufacturer specified performance levels).

F.3. Equipment Tested

The equipment tested were the HFC-FPGA Qualification Test Specimen. Table 2 identifies the specific items that are part of the Qualification Test Specimen.

F.4. Sequence of Testing

The Seismic Test was the last qualification test performed on 10/17/2016. The Seismic Test includes the following tests:

- Configuration: Pre-Test Setup and Inspection
- Operability and Prudency Check: Pre-Test
- Resonance Search
- Five Operating Basis Earthquakes (OBE)
- One Safety Shutdown Earthquake (SSE)
- Post Seismic Test

Automated Analog Accuracy Test, Response Time Test, Timer Test, Communication Operability Test and Burst of Events Test were performed during OBE.

Automated Analog Accuracy Test, Response Time Test, Timer Test and Communication Operability Test were performed during SSE.

Test sections that were manually executed or takes significant time to complete were not performed during seismic test due to inaccessibility of the qualification test system and short durations of each OBE and SSE.

F.5. Procedures

The following procedures were used during the prequalification test:

- TP901-302-06, VV0115 Qualification Seismic Test Procedure (Reference 20): Through this procedure, the HFC-FPGA Qualification Test Specimen was subjected to resonance search testing and received additional configuration on the test table for Seismic Testing. This procedure required monitoring the performance of the HFC-FPGA Qualification Test Specimen throughout application of the Seismic Test conditions.
- TP901-115-01, VV0115 Qualification Operability Test Procedure (Reference 13): This procedure includes a series of tests defined in Section 5.3 of EPRI TR-107330 that verified acceptable performance of the HFC-FPGA Qualification Test Specimen in accordance with the manufacturer's specifications for the HFC-FPGA platform. A complete repetition of this test procedure was performed as part of the Post Seismic Test.
- TP901-115-02, VV0115 Qualification Prudency Test Procedure (Reference 14): This procedure includes a series of tests defined in Section 5.4 of EPRI TR-107330 that verified acceptable performance of the HFC-FPGA Qualification Test Specimen in accordance with the manufacturer's specifications for the HFC-FPGA platform. A complete repetition of this test procedure was performed as part of the Post Seismic Test.

F.6. Test Specimen Mounting

The Seismic Test was conducted at the facilities of [ ]. General test setups Seismic Test are shown in Figure 27 to Figure 32.

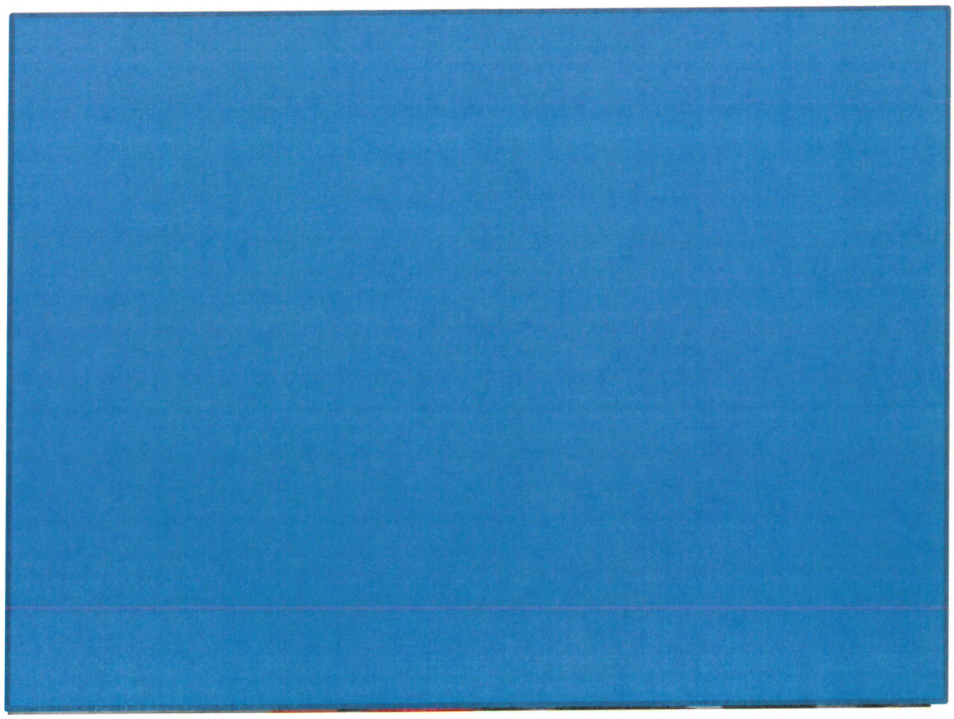


Figure 33. Seismic Test – Setup

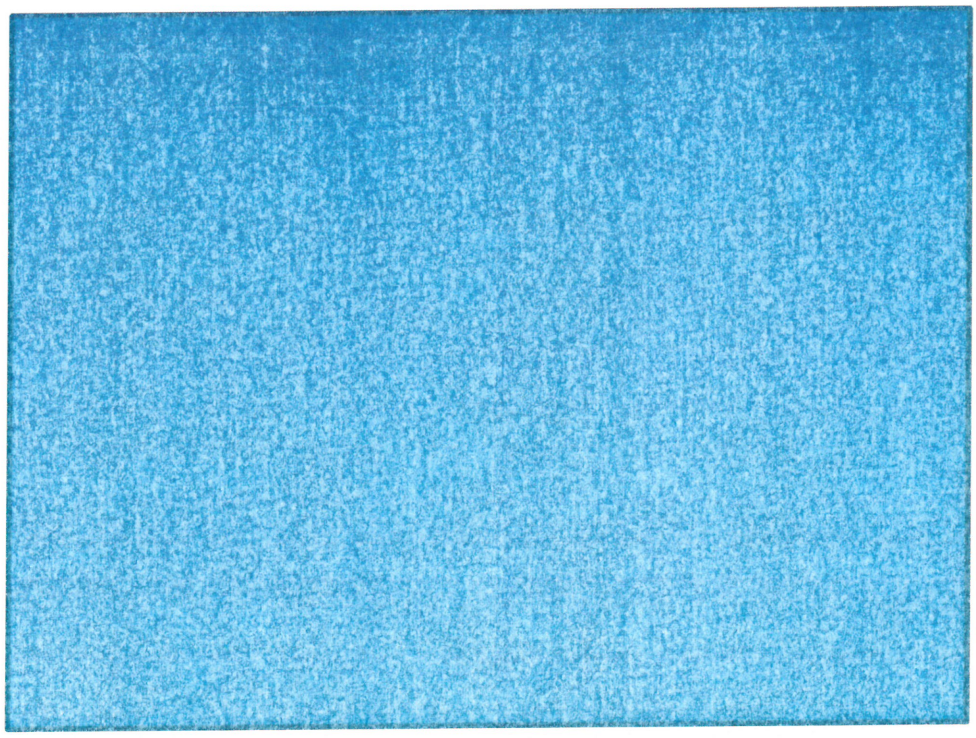


Figure 34. Seismic Test – Pre-Test 1

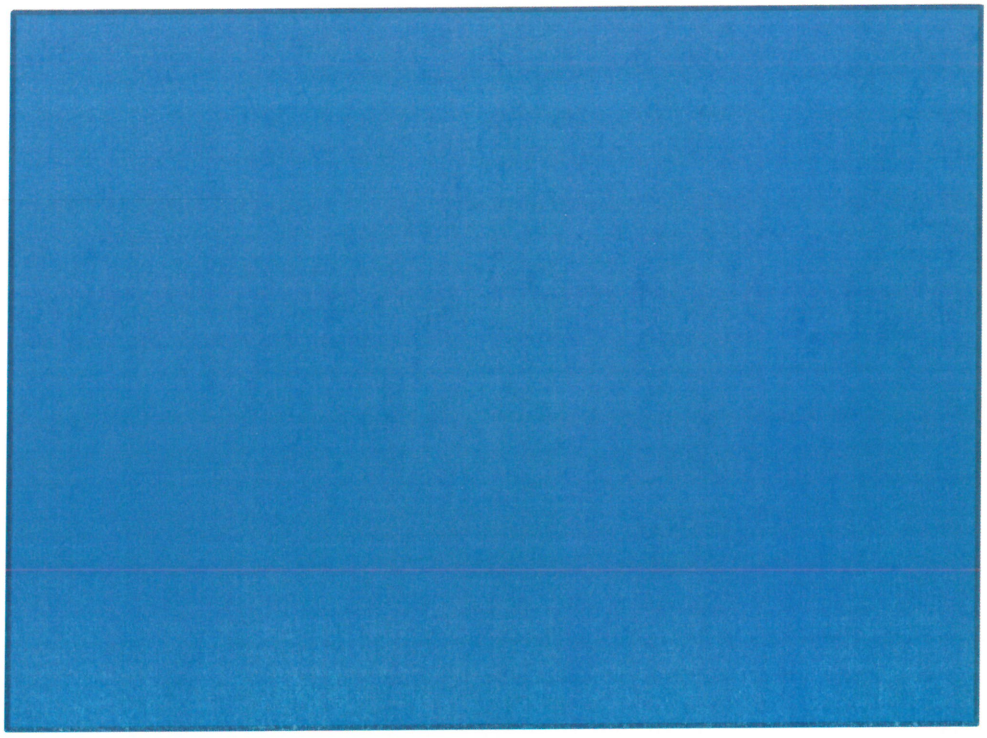


Figure 35. Seismic Test – Pre-Test 2

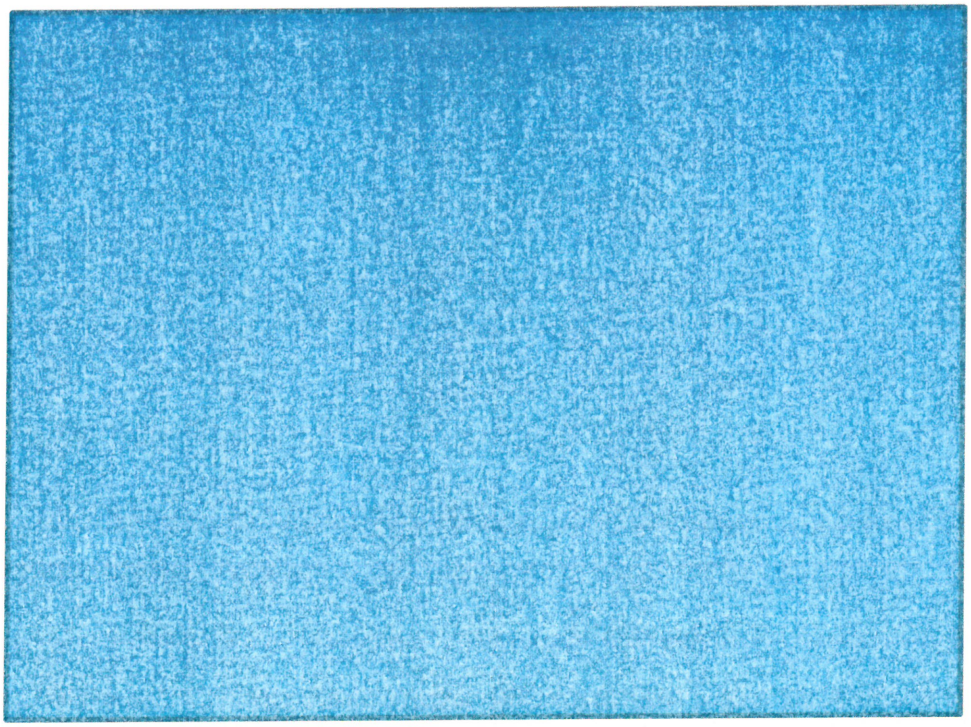


Figure 36. Seismic Test – Post-Test 1

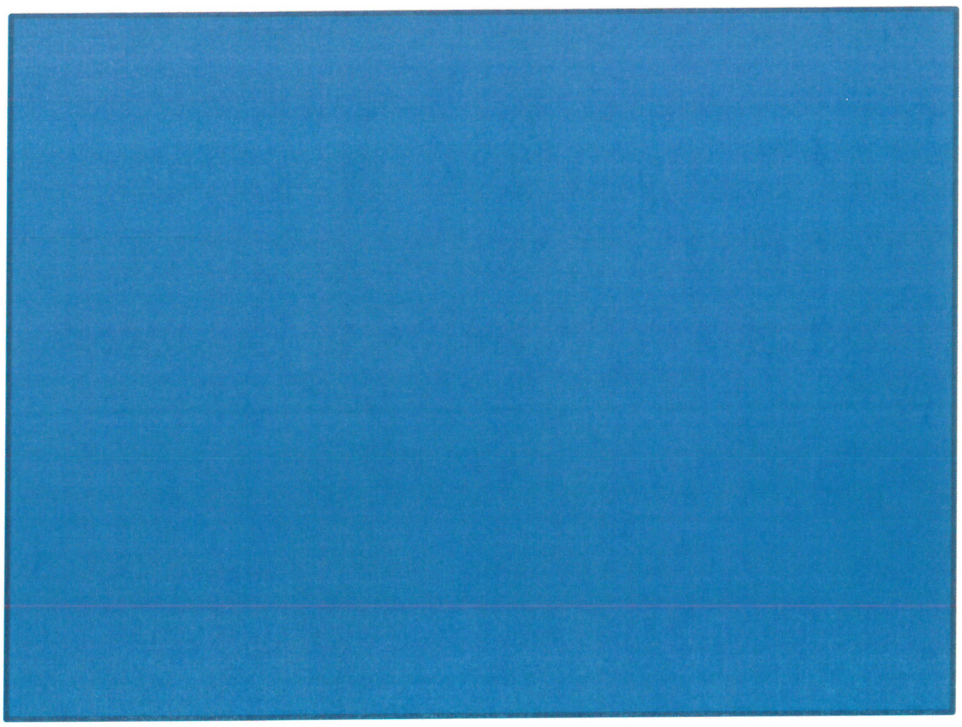


Figure 37. Seismic Test – Post-Test 2

F.7. Service Conditions

The Seismic Test was conducted on a three-axis seismic simulation table using the seismic spectrum illustrated in Figure 38 as the basis. According to the Lab Report, 14149 [ ] Seismic Qualification Test Report, SRS curve that was used starts at 1 Hz and damping used was 5%.

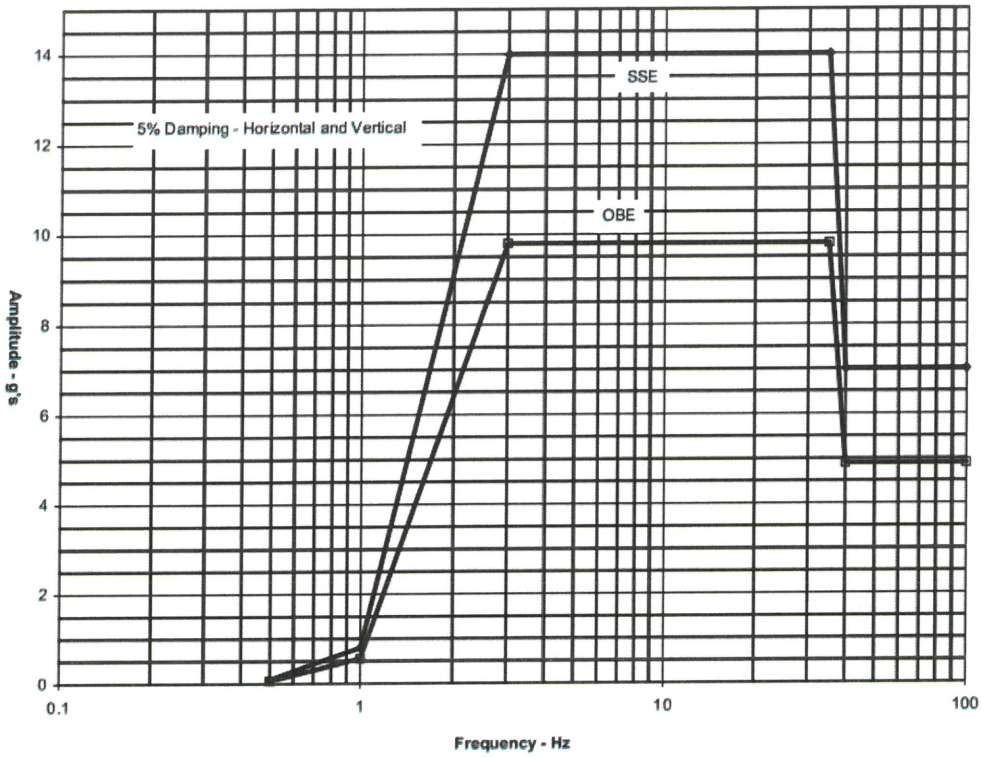


Figure 38. Seismic Test Spectrum

F.8. Test Levels

The test levels (supply power and I/O signal and load levels) applied to the HFC-FPGA Test Specimen during the Seismic Test were set as specified in corresponding test procedures (References 13, 14, and 20).

F.9. Performance Monitoring

Performance monitoring of the HFC-FPGA Test Specimen during the Seismic Test were set as specified in corresponding test procedures (References 13, 14, and 20).

F.10. Acceptance Criteria

Acceptance criteria for performance monitoring of the HFC-FPGA Test Specimen during the Seismic Test were set as specified in corresponding test procedures (References 13, 14, and 20). They are summarized in Table 20.

Table 20. Acceptance Criteria for Seismic Test

Test	Sub-Test	Acceptance Criteria
Configuration: Pre-Test Setup and Inspection	Output Level of Power Supplies Verification	
	Qualification Test Specimen Status Verification	
	Alarm Status Verification	
Operability and Prudency Check: Pre-Test	Operability - Automated Analog Accuracy Test	
	Operability - Automated Response Time Test	
	Operability - Communication Operability Test	
	Operability - Automated Timer Test	
	Operability - Loss of Power Test	
	Prudency - Analog and Digital Burst of Events Test	

Resonance Search	N/A	
OBE Test	N/A	

SSE Test	N/A	
Operability Test: Seismic Post Test	Accuracy Test (Automatic and Manual)	
	Response Time Test (Digital and Analog)	
	Discrete Input Operability Test	
	Discrete Output Operability Test	
	Communication Operability Test	

	Timer Test	
	Failure to Complete Scan Detection	
	Failover Test	
	Redundancy Test	
	Loss of Power Test	

Prudency Test: Seismic Post Test	Burst of Events Test	
	Serial Port Failure / Noise Test	

F.11. Documentation

The following attachments in TR901-302-01 (Reference 9) were prepared as records by HFC to document the results of HFC-FPGA prequalification test:

- Seismic Test
  - Attachment 13.25 14149 IEEE Seismic Qualification Test Report Rev1
  - Attachment 13.26 Completed record of TP901-302-06, VV0115 Qualification Seismic Test Procedure
- Post Seismic Test
  - Attachment 13.27 Completed record of TP901-115-01, Operability Test Procedure for Seismic tests
  - Attachment 13.28 Completed record of TP901-115-02, Prudency Test Procedure for Seismic tests
  - Attachment 13.29 Completed record of TP901-115-01, Operability Test Procedure for Post-Seismic tests
  - Attachment 13.30 Completed record of TP901-115-02, Prudency Test Procedure for Post-Seismic tests

F.12. Test Results

Detailed test results of the Seismic Test were reported in TR901-302-01 (Reference 9), which are summarized in Table 21.

Table 21. Summary of Seismic Test Results

Test	Sub-Test	Redmine or CR	Sub-Test Result	Overall Result
Configuration: Pre-Test Setup and Inspection	Output Level of Power Supplies Verification			
	Qualification Test Specimen Status Verification			
	Alarm Status Verification			
Operability and Prudency Check: Pre-Test	Operability - Automated Analog Accuracy Test			
	Operability - Automated Response Time Test			
	Operability - Communication Operability Test			
	Operability - Automated Timer Test			
	Operability - Loss of Power Test			
	Prudency - Analog and Digital Burst of Events Test			
Resonance Search	N/A			
OBE Test	N/A			
SSE Test	N/A			
Operability Test: Seismic Post Test	Accuracy Test (Automatic and Manual)			
	Response Time Test (Digital and Analog)			
	Discrete Input Operability Test			
	Discrete Output Operability Test			
	Communication Operability Test			
	Timer Test			
	Failure to Complete Scan Detection			
	Failover Test			
	Redundancy Test			
	Loss of Power Test			

Test	Sub-Test	Redmine or CR	Sub-Test Result	Overall Result
Prudency Test: Seismic Post Test	Burst of Events Test			
	Serial Port Failure / Noise Test			

F.13. Resolution of Test Discrepancies

HFC uses a Condition Report Microsoft Access Database and a Redmine project management and issue tracking tool to record all the issues encountered during Equipment Qualification.

During Seismic Test, below issues were tracked and resolved:

Condition Report CR2016-0400, created on 10/24/2016. During each OBE and SSE, the remote 1 RIF alarm occurs. Investigation shows the RIF cable was the issue, the resolution was to replace the cables. This CR is considered resolved.