Westinghouse Electric Corporation
Energy Systems

Nuclear Services Division
Box 355
Pittsburgh Pennsylvania 15230-0355

April 15, 1997
CAW-97-1095

Document Control Desk
U.S. Nuclear Regulatory Commission
Washington, DC 20555

Attention: Mr. Samuel L. Collins

APPLICATION FOR WITHHOLDING PROPRIETARY
INFORMATION FROM PUBLIC DISCLOSURE

Subject: "Presentation Material Entitled, "ASIC Based Reactor Control and Protection System Replacement Modules for Westinghouse Design Nuclear Units," March 18, 1997 (Proprietary)

Dear Mr. Collins:

The proprietary information for which withholding is being requested in the above-referenced report is further identified in Affidavit CAW-97-1095 signed by the owner of the proprietary information, Westinghouse Electric Corporation. The affidavit, which accompanies this letter, sets forth the basis on which the information may be withheld from public disclosure by the Commission and addresses with specificity the considerations listed in paragraph (b)(4) of 10 CFR Section 2.790 of the Commission's regulations.

Accordingly, this letter authorizes the utilization of the accompanying Affidavit by the Westinghouse Owners Group.

Correspondence with respect to the proprietary aspects of the application for withholding or the Westinghouse affidavit should reference this letter, CAW-97-1095, and should be addressed to the undersigned.

Very truly yours,

N. J. Liparulo, Manager
Equipment Design and Regulatory Engineering

Enclosures

cc: Kevin Bohrer/NRC (12H5)

CAW-97-1095

AFFIDAVIT

COMMONWEALTH OF PENNSYLVANIA:

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COUNTY OF ALLEGHENY:

Before me, the undersigned authority, personally appeared Nicholas J. Liparulo, who, being by me duly sworn according to law, deposes and says that he is authorized to execute this Affidavit on behalf of Westinghouse Electric Corporation ("Westinghouse") and that the averments of fact set forth in this Affidavit are true and correct to the best of his knowledge, information, and belief:

Nicholas J. Liparulo, Manager
Equipment Design and Regulatory Engineering

Sworn to and subscribed
before me this 15th day
of April, 1997

Notary Public

Notarial Seal
Janet A. Schwab, Notary Public
Monroeville Boro, Allegheny County
My Commission Expires May 22, 2000
Member, Pennsylvania Association of Notaries

2607C-RJS-1:041597

(1) I am Manager, Equipment Design and Regulatory Engineering, in the Nuclear Services Division, of the Westinghouse Electric Corporation and as such, I have been specifically delegated the function of reviewing the proprietary information sought to be withheld from public disclosure in connection with nuclear power plant licensing and rulemaking proceedings, and am authorized to apply for its withholding on behalf of the Westinghouse Energy Systems Business Unit.

(2) I am making this Affidavit in conformance with the provisions of 10CFR Section 2.790 of the Commission's regulations and in conjunction with the Westinghouse application for withholding accompanying this Affidavit.

(3) I have personal knowledge of the criteria and procedures utilized by the Westinghouse Energy Systems Business Unit in designating information as a trade secret, privileged or as confidential commercial or financial information.

(4) Pursuant to the provisions of paragraph (b)(4) of Section 2.790 of the Commission's regulations, the following is furnished for consideration by the Commission in determining whether the information sought to be withheld from public disclosure should be withheld.

(i) The information sought to be withheld from public disclosure is owned and has been held in confidence by Westinghouse.

(ii) The information is of a type customarily held in confidence by Westinghouse and not customarily disclosed to the public. Westinghouse has a rational basis for determining the types of information customarily held in confidence by it and, in that connection, utilizes a system to determine when and whether to hold certain types of information in confidence. The application of that system and the substance of that system constitutes Westinghouse policy and provides the rational basis required.

Under that system, information is held in confidence if it falls in one or more of several types, the release of which might result in the loss of an existing or potential competitive advantage, as follows:

(a) The information reveals the distinguishing aspects of a process (or component, structure, tool, method, etc.) where prevention of its use by any of Westinghouse's competitors without license from Westinghouse constitutes a competitive economic advantage over other companies.

(b) It consists of supporting data, including test data, relative to a process (or component, structure, tool, method, etc.), the application of which data secures a competitive economic advantage, e.g., by optimization or improved marketability.

(c) Its use by a competitor would reduce his expenditure of resources or improve his competitive position in the design, manufacture, shipment, installation, assurance of quality, or licensing a similar product.

(d) It reveals cost or price information, production capacities, budget levels, or commercial strategies of Westinghouse, its customers or suppliers.

(e) It reveals aspects of past, present, or future Westinghouse or customer funded development plans and programs of potential commercial value to Westinghouse.

(f) It contains patentable ideas, for which patent protection may be desirable.

There are sound policy reasons behind the Westinghouse system which include the following:

(a) The use of such information by Westinghouse gives Westinghouse a competitive advantage over its competitors. It is, therefore, withheld from disclosure to protect the Westinghouse competitive position.

(b) It is information which is marketable in many ways. The extent to which such information is available to competitors diminishes the Westinghouse ability to sell products and services involving the use of the information.

(c) Use by our competitor would put Westinghouse at a competitive disadvantage by reducing his expenditure of resources at our expense.

(d) Each component of proprietary information pertinent to a particular competitive advantage is potentially as valuable as the total competitive advantage. If competitors acquire components of proprietary information, any one component may be the key to the entire puzzle, thereby depriving Westinghouse of a competitive advantage.

(e) Unrestricted disclosure would jeopardize the position of prominence of Westinghouse in the world market, and thereby give a market advantage to the competition of those countries.

(f) The Westinghouse capacity to invest corporate assets in research and development depends upon the success in obtaining and maintaining a competitive advantage.

(iii) The information is being transmitted to the Commission in confidence and, under the provisions of 10CFR Section 2.790, it is to be received in confidence by the Commission.

(iv) The information sought to be protected is not available in public sources or available information has not been previously employed in the same original manner or method to the best of our knowledge and belief.

(v) The proprietary information sought to be withheld in this submittal is that which is appropriately marked in presentation material entitled, "ASIC Based Reactor Control and Protection System Replacement Modules for Westinghouse Design Nuclear Units," March 18, 1997 (Proprietary) on behalf of the Westinghouse Owners Group by the Westinghouse Electric Corporation, being transmitted by the Westinghouse Owners Group letter and Application for Withholding Proprietary Information from Public Disclosure, Mr. Thomas V. Greene, Chairman, Westinghouse Owners Group

to the Document Control Desk, Attention Mr. Samuel J. Collins. The proprietary information as submitted for use by the Westinghouse Owners Group is applicable to other licensee submittals.

This information is part of that which will enable Westinghouse to:

(a) Provide the NRC with detailed design information related to the ASIC Based Replacement Modules.

(b) Provide the NRC with the design, test, and qualification process information.

Further this information has substantial commercial value as follows:

(a) Westinghouse and the Westinghouse Owners Group plan to use these modules to replace analog modules in order to support long term maintainability of protection and control systems.

(b) Westinghouse can use aspects of the design in future products and services.

Public disclosure of this proprietary information is likely to cause substantial harm to the competitive position of Westinghouse because it would enhance the ability of competitors to provide similar products for commercial power reactors without commensurate expenses. Also, public disclosure of the information would enable others to use the information to meet NRC requirements for licensing documentation without purchasing the right to use the information.

The development of the technology described in part by the information is the result of applying the results of many years of experience in an intensive Westinghouse effort and the expenditure of a considerable sum of money.

In order for competitors of Westinghouse to duplicate this information, similar design programs would have to be performed and a significant manpower effort, having the

requisite talent and experience, would have to be expended for the development of replacement modules.

Further the deponent sayeth not.

Copyright Notice

The reports transmitted herewith each bear a Westinghouse copyright notice. The NRC is permitted to make the number of copies of the information contained in these reports which are necessary for its internal use in connection with generic and plant-specific reviews and approvals as well as the issuance, denial, amendment, transfer, renewal, modification, suspension, revocation, or violation of a license, permit, order, or regulation subject to the requirements of 10 CFR 2.790 regarding restrictions on public disclosure to the extent such information has been identified as proprietary by Westinghouse, copyright protection notwithstanding. With respect to the non-proprietary versions of these reports, the NRC is permitted to make the number of copies beyond those necessary for its internal use which are necessary in order to have one copy available for public viewing in the appropriate docket files in the public document room in Washington, DC and in local public document rooms as may be required by NRC regulations if the number of copies submitted is insufficient for this purpose. Copies made by the NRC must include the copyright notice in all instances and the proprietary notice if the original was identified as proprietary.

Proprietary Information Notice

Transmitted herewith are proprietary and/or non-proprietary versions of documents furnished to the NRC in connection with requests for generic and/or plant-specific review and approval.

In order to conform to the requirements of 10 CFR 2.790 of the Commission's regulations concerning the protection of proprietary information so submitted to the NRC, the information which is proprietary in the proprietary versions is contained within brackets, and where the proprietary information has been deleted in the non-proprietary versions, only the brackets remain (the information that was contained within the brackets in the proprietary versions having been deleted). The justification for claiming the information so designated as proprietary is indicated in both versions by means of lower case letters (a) through (f) contained within parentheses located as a superscript immediately following the brackets enclosing each item of information being identified as proprietary or in the margin opposite such information. These lower case letters refer to the types of information Westinghouse customarily holds in confidence identified in Sections (4)(ii)(a) through (4)(ii)(f) of the affidavit accompanying this transmittal pursuant to 10 CFR 2.790(b)(1).

Westinghouse Owners Group

Westinghouse Owners Group - EPRI Meeting with the US NRC on ASIC Based Reactor Control & Protection System Replacement Modules for Westinghouse Designed Nuclear Units

March 18, 1997

NRC White Flint Offices

Westinghouse Owners Group - EPRI Meeting with the US NRC

Westinghouse Owners Group

AGENDA

WOG-NRC ASICs Meeting Agenda

DATE: March 18, 1997
TIME: 8:30 - 12:00

PLACE: NRC White Flint Offices
Proprietary Information to be Discussed

PARTICIPANTS:

NRC:	Jim Stewart
	Jerry Mauck
	Diedra Spaulding
	Claudia Craig
Utilities:	Mike Marino (VP)
	Darrell Cooksey (UE)
	Paul Travis (HL&P)
	Dennis Deardorf (SCE&G)
	Bob Queenan (Duke)
	Joe Ruether (NSP)
	John Guider (RGE)
	Pravin Shah (TUE)
	Karl Jacobs (NYPA)
EPRI:	Joe Naser
Westinghouse:	Carl Vitalbo
	Bob Sterdis
	Dick Miller
ORNL:	Ron Battle
ATC:	Mike Natale

AGENDA:

I. Design Update

II. Design, Verification, & Validation Plan

III. Test & Qualification Process
- A. ASIC Chip Test Program
  - 1. Test Vectors
  - 2. Fault Coverage
  - 3. Simulation Results
  - 4. Test Result Summary
- B. Validation Test Plan
- C. Qualification Test Plan

IV. Topical Report Submittal Schedule

V. NRC Summary of "Safety Critical Application for ASICs" Report

VI. Wrap-up

Westinghouse Owners Group - EPRI
Meeting with the US NRC

Westinghouse Owners Group

DESIGN UPDATE

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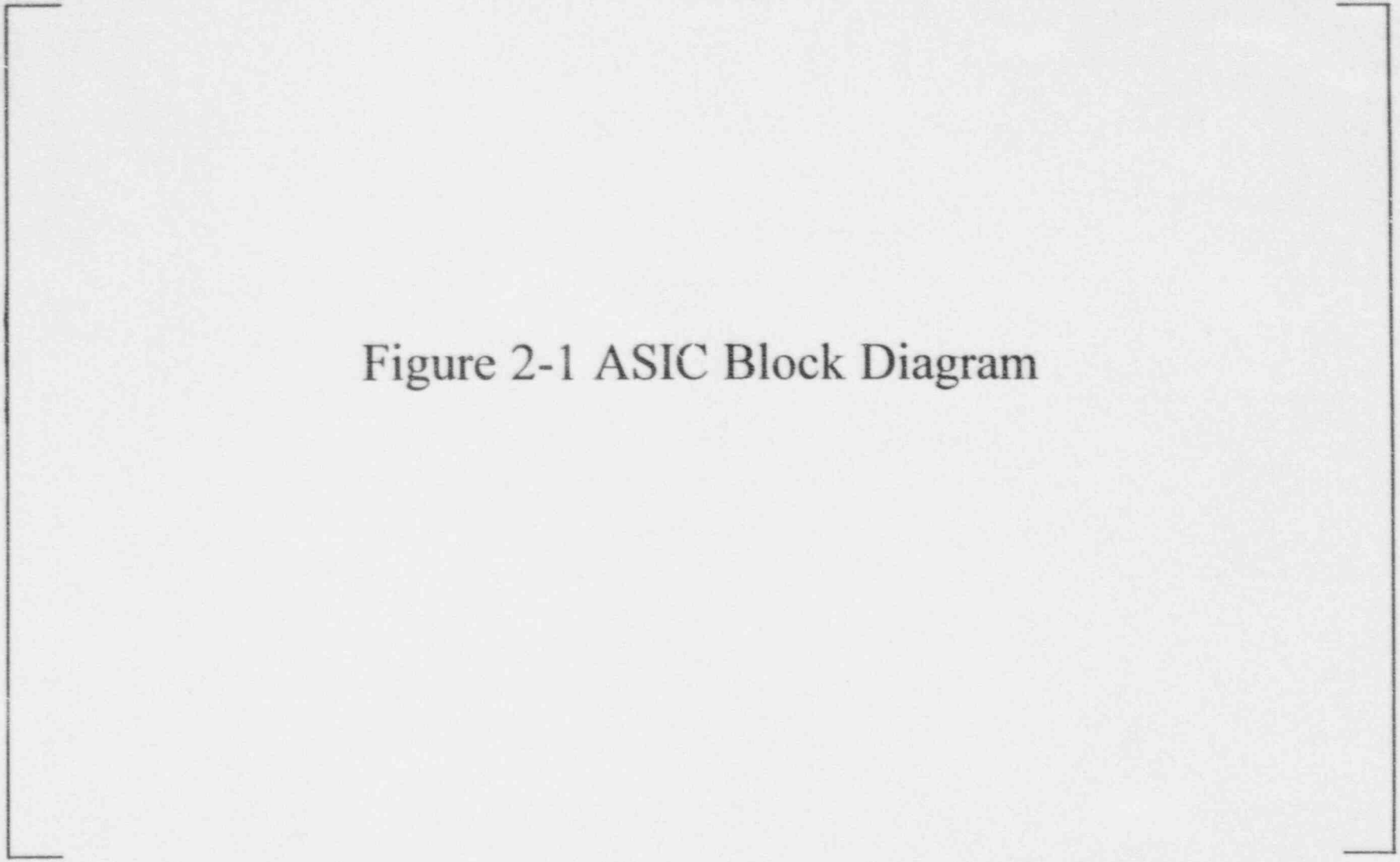

Figure 2-1 ASIC Block Diagram

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ASICs CARD DIAGRAM

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7300A OPERATOR INTERFACE

(Sheet 1 of 2)

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7300A OPERATOR INTERFACE

(Sheet 2 of 2)

Westinghouse Owners Group - EPRI Meeting with the US NRC

Westinghouse Owners Group

Design, Verification, & Validation Plan

ASIC PROGRAM
DESIGN, VERIFICATION & VALIDATION PROGRAM

PURPOSE

- Provide guidance for the design, verification and validation of the ASIC Based RPS Replacement Module Development Program.
- Provide a disciplined development process across multiple design organizations.
- Provide references to applicable codes and standards

ORGANIZATIONAL OVERVIEW

- Westinghouse Electric Company
  - Program Technical Lead
  - Primary design, verification, validation and licensing organization
  - 10CFR50 Appendix B supplier
  - Procedures in place for design, verification and validation activities
  - Responsible for independent review of design activities performed by others
  - Conduct validation tests to confirm adherence to requirements

ASIC PROGRAM
DESIGN, VERIFICATION & VALIDATION PROGRAM

Westinghouse is responsible for the following program activities:

1. Project definition
2. Conceptual design
3. Project specific methods and activities
4. Functional requirement definition (process functions, algorithms, etc.)
5. Hardware requirement definition
6. Analysis
7. Technical integration of all design areas (main board, personality modules, ASIC, Controller)
8. Main board design, layout and assembly
9. Operator Interface design
10. Personality module design, layout and assembly
11. Configuration Management Control
12. Documentation (specifications, design drawings, manufacturing drawings, etc.)
13. Second party review of all ORNL design activities (e.g.. controller algorithm verification)
14. Reliability Assessment and Failure Modes and Effects Analysis
15. Design Reviews (Preliminary, Intermediate and Final)
16. Validation Testing of integrated product
17. Abnormal Conditions and Events Testing (ACEs)
18. Qualification Testing of integrated product
19. Licensing, including regulatory compliance analysis
20. Prototype and production unit fabrication
21. Commercial Dedication of ASIC
22. Technical Manual

ASIC PROGRAM
DESIGN, VERIFICATION & VALIDATION PROGRAM

- Oak Ridge National Laboratory (ORNL)
  - Design of ASIC chip and Controller
  - Not an Appendix B supplier
  - Treated as a commercial vendor

  ORNL is responsible for the following program activities:

  1. ASIC design and layout
  2. ASIC prototype fabrication (ORBIT devices)
  3. Controller design
  4. Controller code development
  5. Implementation of process functions and algorithms in Controller

ASIC PROGRAM
DESIGN, VERIFICATION & VALIDATION PROGRAM

- Northrop Grumman Advanced Technology Center (ATC)
  - Responsible for simulation testing of ORNL ASIC design
  - Fabrication of ASIC devices for qualification & production
  - Comprehensive testing of devices prior to delivery
  - Not an Appendix B supplier
  - Treated as a commercial vendor

Northrop Grumman ATC is responsible for the following program activities:

1. Independent simulation testing of ORNL ASIC design
2. ASIC prototype testing (ORBIT devices)
3. ASIC fabrication for qualification and production
4. ASIC component testing

ASIC PROGRAM
DESIGN, VERIFICATION & VALIDATION PROGRAM

SYSTEM LIFE CYCLE DEVELOPMENT PROCESS

- Eight phases
  - Conceptual/Planning Phase
  - Requirements Phase
  - Design Phase
  - Implementation Phase
  - Integration and Test Phase
  - Installation and Checkout Phase
  - Operation and Maintenance Phase
  - Retirement Phase

DESIGN PROCESS

- Design organization (WEC) is responsible for assuring that design, verification and validation activities are performed in a manner which maintains the review process *independent* from the design process.

- Independence means an *objective second-party review* by competent individual(s) of material which they did not design.
  - Internal second-party review of all design documentation
  - Auditing vendors to assure adherence to the design and review process

ASIC PROGRAM
DESIGN, VERIFICATION & VALIDATION PROGRAM

VERIFICATION PROCESS

- Objective: Independently confirm, by means other than accomplished by the designer, that the final design functions as documented.

- Bottom-Up Review process: Divides the overall system design into smaller "subsystems" for evaluation (for example, an analog input circuit or a digital output circuit). After all "subsystems" are verified, the complete system is evaluated. This design verification philosophy ensures that all subsystems and interfaces between subsystems are reviewed and/or tested

- Conducting formal design reviews
  - Preliminary Design Review during Design Phase

  - Intermediate Design Review during Implementation Phase

  - Final Design Review during Integration and Test Phase

ASIC PROGRAM
DESIGN, VERIFICATION & VALIDATION PROGRAM

- Simulation Testing
- Determines performance of design as separate entity, without actual system hardware.

- Verifies that the functionality of the design meets the applicable design specifications.

- Comprehensively exercises (via computer emulation) the design

- Used to verify the transformation from a "paper design" to actual hardware.

- Test inputs (or test vectors) are developed to exercise all the possible signal paths through a system or component, and operation is compared to expected results.

- For components or system operation not directly observable, a qualitative analysis should be performed to assess the significance of the components not exercised.

- Used to evaluate the system response to potential unintended functions (i.e., transients, noise, etc.). The simulation process can also be used to evaluate interactions between subsystems (i.e., loading, opens, shorts, etc.) and to ascertain postulated failure modes and effects.

- After completion of simulation testing, design is released for fabrication and subsequent system validation testing.

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CONTROLLER DESIGN, VERIFICATION & VALIDATION PROCESS

ASIC PROGRAM
DESIGN, VERIFICATION & VALIDATION PROGRAM

VALIDATION PROCESS

- Demonstrates that the system design meets the system functional requirements on the target hardware

- System Validation Plan defines a methodology that must be followed to perform a series of functional requirement based tests which compliment the reviews and simulations conducted during the design verification phase.

(1) Functional Requirements Testing

- Insures that the design meets the functional requirements and that good design practice was utilized

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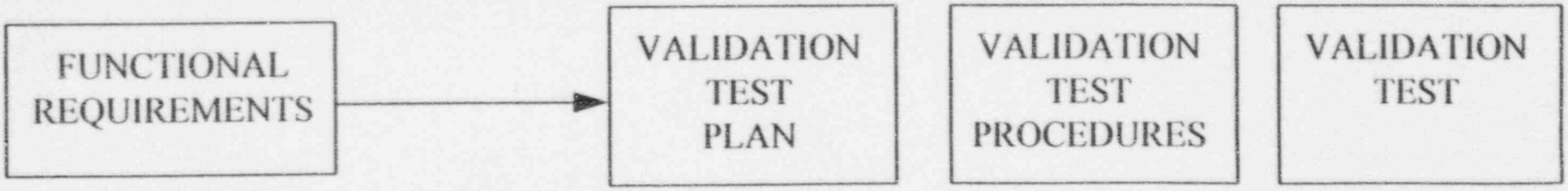


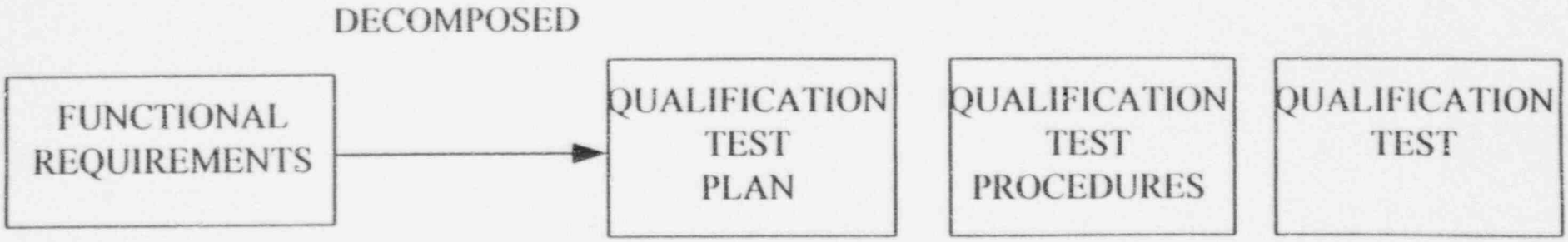
- Good engineering practice
  - a. Interfaces between other systems, subsystems or components.
  - b. Maintenance and calibration features.
  - c. Diagnostics and alarms.
  - d. Component placement for manufacturability.
  - e. Location of operator interface controls.

ASIC PROGRAM
DESIGN, VERIFICATION & VALIDATION PROGRAM

(2) Qualification Testing

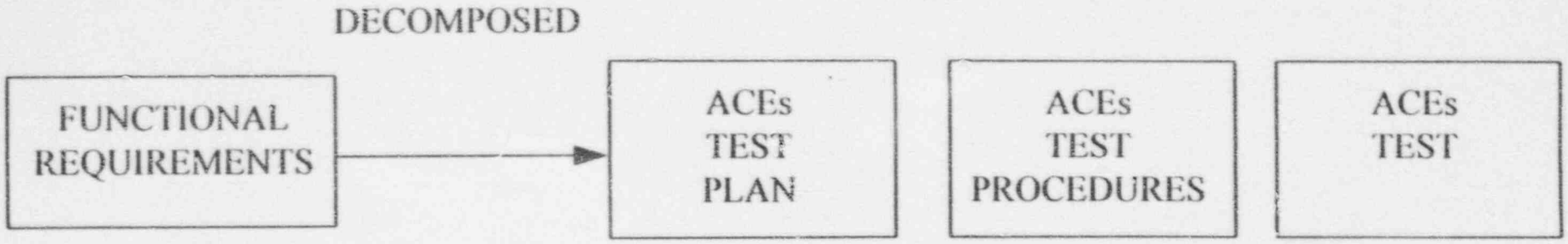
- Insures that the design operates within predefined acceptance criteria when subjected to anticipated extremes of the environment, seismic disturbances and electrical interference.

1. Environmental (temperature and humidity)
2. Seismic
3. Electro-Magnetic Interference (EMI) and Radio Frequency Interference (RFI).
4. Electrical Noise.
5. Electrical Fault.
6. Electrical Surge.



ASIC PROGRAM
DESIGN, VERIFICATION & VALIDATION PROGRAM

(3) Abnormal Conditions and Events (ACEs) Testing
- Insures that the design operates in a known and predictable manner under abnormal mode conditions.



PROBLEM REPORTING & RESOLUTION

DESIGN, VERIFICATION & VALIDATION REPORTS
- Validation Test Report
- Qualification Test Report
- ACE Test Report

ASIC PROGRAM
DESIGN, VERIFICATION & VALIDATION PROGRAM

GUIDELINES FOR COMMERCIAL GRADE ITEM DEDICATION

- When applying the guideline to the commercial grade item dedication of the ASIC chip, the following process results:

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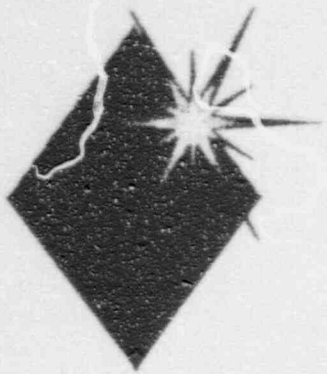
Westinghouse Owners Group - EPRI
Meeting with the US NRC

Westinghouse Owners Group

Test & Qualification Process



ASIC-Based Replacement Modules

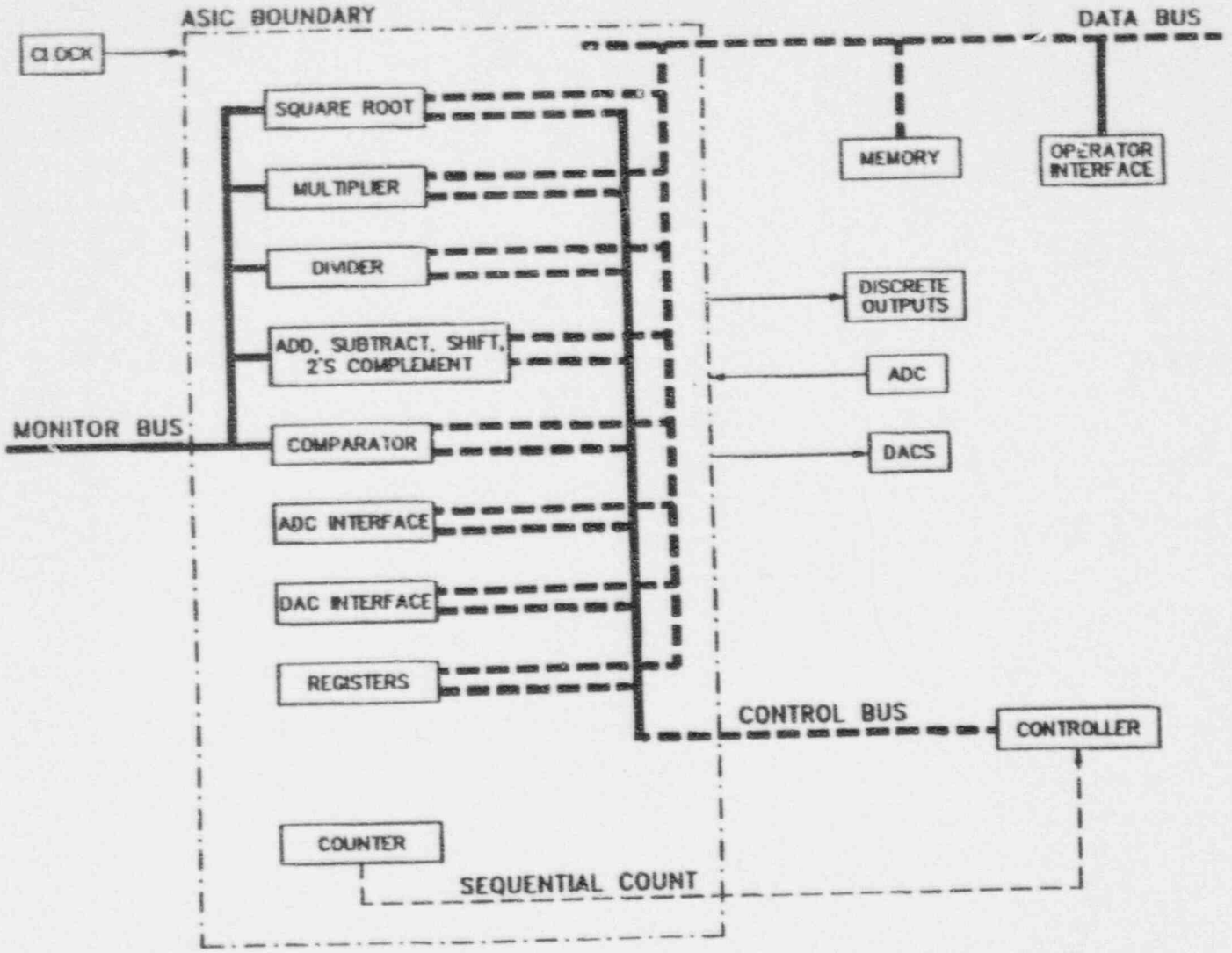
R. E. Battle

ORNL

March 18, 1997

ASIC Consists of Functional Blocks for RPS

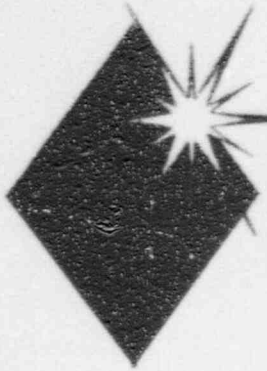
- Blocks input data, manipulate data, store data, and output data
- High level blocks were selected to implement RPS card functions
- Data bus connects blocks and provides input and output
- Functions are selected by a control PROM that is stepped by an ASIC counter



DAC: DIGITAL–TO–ANALOG CONVERTER
ADC: ANALOG–TO–DIGITAL CONVERTER

Design and Functional Tests Started at Lowest Level

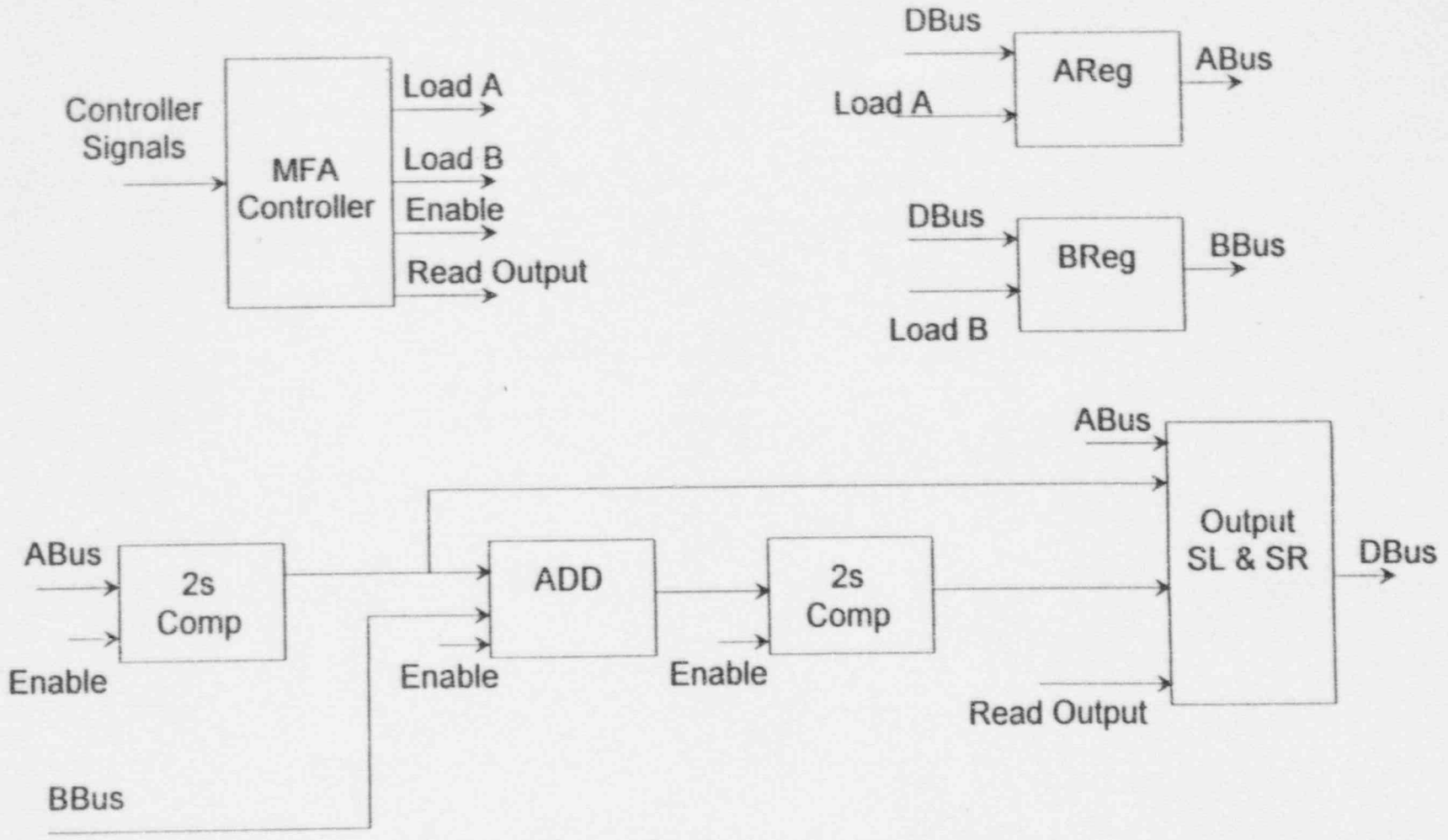
- Top level functions for RPS were selected
- Lowest level circuits were designed and tested by the designer prior to moving to next higher level
- The low-level circuits were combined and then tested at the next level
- Finally, top level ASIC functions and the core were tested
- All possible controller instructions were input for each function, which operated each device and moved data between them



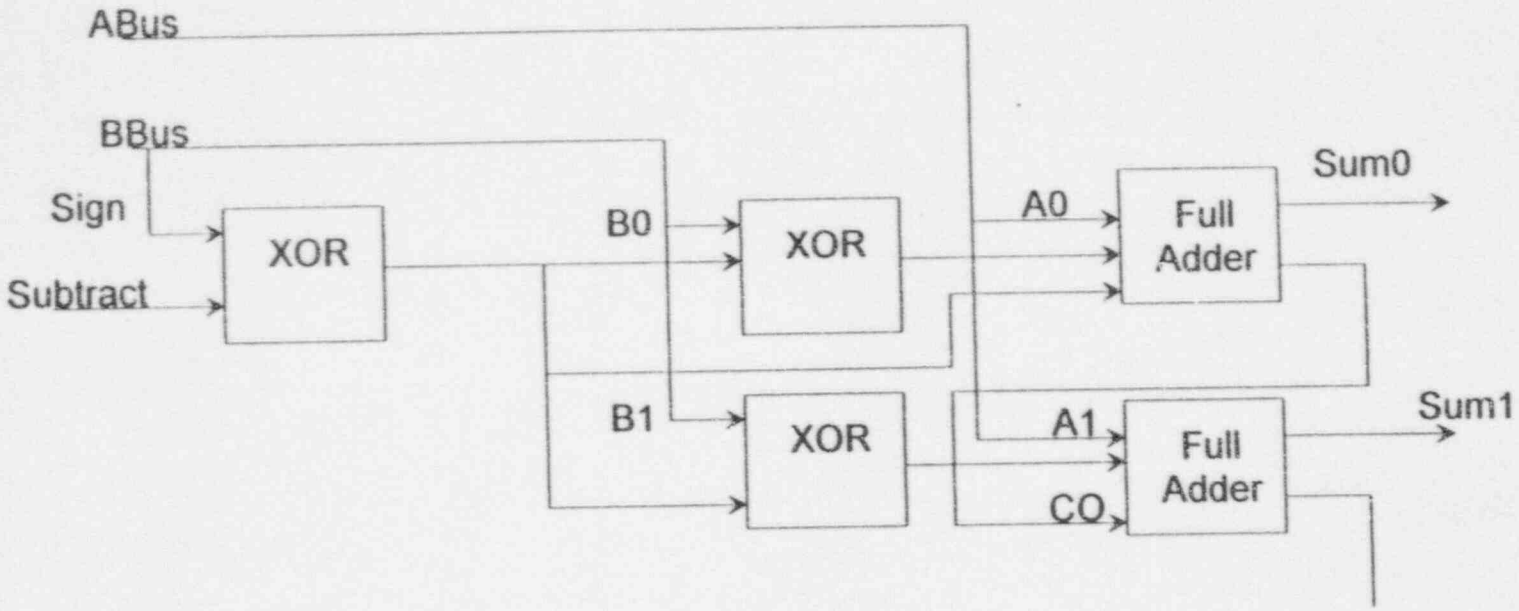
Functional Tests Used Hierarchical Architecture

- At the lowest level, detailed functional tests were conducted
- Higher levels consisted of replicated circuits that were tested at lower level
- Normal and boundary value numbers were tested. All combinations of signed numbers were tested
- All interfaces between functions were tested
- Hierarchical circuits connect to outside circuits at top level only
- Access to functional blocks by external data bus reduces the number of tests

Top-Level Block for Adder



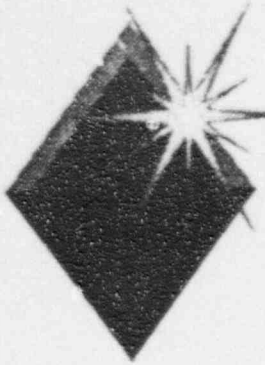
Low-Level Circuits for the ADD Block



These circuits are repeated 40 times plus a block for overflow

Functional Testing Used Two Simulators

- Logic simulations done at each level ensured they function properly
- Analog simulations of layout ensured there were no timing problems
- Timing simulations were done at 4 MHz for circuits intended to operate at 1 MHz
- All the functional tests were run on the analog simulation
- Single, low-speed clock and synchronous circuits essentially eliminate timing problems



Enhanced Test Vectors Test the Fabricated ASIC

- 40-bit vectors were divided into 10 hexadecimal components
- These tests include normal and boundary value vectors designed to detect stuck-at faults
- Hex components test many of the circuits simultaneously by operating them in parallel
- Typical vectors selected included alternating 0s and 1s; 1s and 0s; all 1s; all 0s; sequentially increasing numbers; and other combinations
- A monitor-bus is available to observe inside some of the functions

Operating Features of the ASIC Increase Reliability

- There are no undefined states. Only a hardware failure can cause continued misoperation
- The controller is designed without loops, interrupts, or branches. Only the data vary between scans
- The ASIC circuits are deterministic in that they respond to enable commands and complete their operation regardless of other external signals
- A single low-speed clock connected to synchronous circuits ensures timing problems will not occur

Summary

- Hierarchical design and bottom-to-top testing make design reliable
- Functional tests were done at each level prior to designing the next level
- Logic- and analog-based simulations were done to test the design and the layout
- Enhanced test vectors were developed to test the fabricated ASIC

Northrop Grumman RPS ASIC Test and Fabrication

M. R. Natale

18 March 1997

ASIC Simulation Testing

- Functional Simulation Files Transferred and Re-Run at ATC
- Performed Independent Review to Confirm Fault Coverage of Simulation Vectors
- Recommended and Received Additional Fault Coverage Simulations From ORNL to Supplement Functional Simulations
  - 9,046 Functional Vectors
  - 149,571 Fault Vectors
  - 65,536 Command Address Vectors
  - >224K
- Reformatted and Added Initiation Sequence To Functional and Fault Simulations to Create Test Vectors

Test Vector Evaluation

- Functional Vectors Individually Exercise All ASIC Functions
- Test of Outputs of All ASIC Functions Aided By Access To Internal Nodes by Monitor Bus
- Extended Vector Set (Fault Vectors) Provides Additional Tests, Combinations of Inputs in Addition to Expected Operational Signals
- Monitor Bus Design and Fault Vectors Provide Extremely High Degree of Fault Coverage

ASIC Tests Are Comprehensive

- Functions Tests - All Individual Functions: Add, Subtract, Shift, 2's Complement, Multiply, Divide, Comparator, ADC & DAC Interfaces

- Combinations of Functions - As Applied in Operation: Square Root-Multiply-Divide, for Example

- System Simulation - Calculates $Y=[-X^2+2(|10X-3|^5)]/3.5$

- Fault Vectors Apply Exhaustive Data Patterns
  - All Possible Bit Patterns in Four Bit Sections
  - Walking one Patterns Applied to Test Sections Interaction
  - All ADC & DAC Channels Tested Simultaneously
  - Differing Patterns in Each ADC & DAC Channel

ASIC Test and Fabrication Summary

- Simulation Testing and Evaluation Complete
- High Fault Coverage Test Established with ORNL
- Prototype Parts Pass This Test
- Northrop Grumman Parts Pass Function Test at Wafer
- Production Parts Are In Assembly and Quality Screening

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ASIC TEST & QUALIFICATION PROCESS

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ASIC TEST & QUALIFICATION PROCESS (cont)

ASIC TEST & QUALIFICATION PROCESS (cont)

SUMMARY

1. INDEPENDENT REVIEW OF ORNL DESIGN WAS CONDUCTED BY ATC
   - Simulation testing of design was conducted by ATC
   - Enhanced test vectors developed to thoroughly test the device

2. DIVERSITY OF REVIEW PROCESS
   - Different People
   - Different Process
   - Different Procedures
   - Different Tools

3. ALL DEVICES TESTED PRIOR TO DELIVERY

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4. COMMERCIAL GRADE ITEM DEDICATION PROCESS

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5. CONCLUSION: ASIC CHIP WILL OPERATE RELIABLY

FPGAs USED IN REPLACEMENT CARD DESIGN

OPERATOR INTERFACE FPGA

- USED TO ENTER/CHANGE/STORE SETPOINTS AND TUNING CONSTANTS
- USED TO PERFORM ANALOG INPUT AND ANALOG OUTPUT CALIBRATION

RAMLogic FPGA

- USED DIVIDE 4MHz CLOCK FREQUENCY DOWN TO 1MHz
- PERFORM PARALLEL TO SERIAL CONVERSION FOR DATA FROM ASIC TO DAC
- PERFORMS COMBINATORIAL LOGIC FOR GENERAL AND TROUBLE ALARMS
- CONTAINS EXTERNAL (SCRATCH PAD) MEMORY FOR INTERMEDIATE CALCULATIONS

FPGAs ARE USED IN CONJUNCTION WITH A PROM THAT CONTAINS THE CONFIGURATION INFORMATION

FEATURES OF DESIGN THAT SUPPORT LICENSING UNDER 10CFR50.59

1. DESIGN PROCESS
   - Controlled & orderly process according to Design, Verification & Validation Plan
   - Using established tools that have wide commercial usage

2. CONFIDENCE LEVEL OF THE CONFIGURATION PROCESS
   - Serial configuration scheme has proven reliable in 1000's of designs & millions of devices
   - CRC codes provide excellent protection against errors
   - 100% protection against erroneous configuration files, defective configuration data sources (PROM), synchronization errors between PROM & FPGA, PCB defects (open/shorted tracks)

3. DATA INTEGRITY (CONFIGURATION, SETPOINTS & TUNING CONSTANTS)
   - Stored values cannot change inadvertently

4. TESTABILITY OF THE CONFIGURED DEVICE
   - Tested as part of integrated assembly during Validation, Qualification and ACEs testing
   - Device functions are simple & can be thoroughly tested
   - Setpoints & Tuning Constants can be tested after card is installed in rack

5. RELIABILITY OF THE FPGA
   - Hardware: Protection provided against abnormal conditions & environment provides assurance of high data integrity in noisy environments
   - Using high quality devices with wide commercial usage, from reputable manufacturer

FEATURES OF DESIGN THAT SUPPORT LICENSING UNDER 10CFR50.59

6. CONSEQUENCES OF FAILURE OF THE OPERATOR INTERFACE FPGA

A. FAILURE TO CONFIGURE
- When card is inserted into slot, FPGA configures from PROM
- During this time, the GA indicator is OFF & the TA indicator is ON
- Upon completion of successful configuration, the GA indicator turns ON (indicating NORMAL operation) & the TA indicator turns OFF
- After this point, any failure is considered a *hardware* failure (such as a gate)

B. FAILURE DURING SETTING SETPOINTS & TUNING CONSTANTS
- Circuit is only active during entering/changing/storing of setpoints & tuning constants
- A failure would result in the wrong value being entered/stored
- Failure would be detectable during the functional test conducted after the change

C. FAILURE DURING CALIBRATION OPERATION
- Only active when enabled by operator (not automatic or "on-line")
- Failure results in inability to calibrate analog inputs or analog outputs
- Failure would be detectable during the functional test conducted after the change (accuracy)

FEATURES OF THE DESIGN THAT SUPPORT LICENSING UNDER 10CFR50.59

7. CONSEQUENCES OF FAILURE OF THE RAMLogic FPGA

A. FAILURE TO CONFIGURE: SAME AS THE OI FPGA

B. FAILURE OF THE CLOCK DIVIDER CIRCUIT
- Divides 4 MHz oscillator frequency down to 1 MHz operational frequency
- Failure could cause operational frequency to go high, low or to zero
- If high or low, the process functions that are time dependent (lag, derivative, lead/lag) will not function correctly because the actual cycle time would be different from the SP & TC which were based on a one millisecond cycle time. This will be detectable during periodic ACOT testing.
- If zero, the dead man timer circuit will time-out, causing the GA to activate
- Failures would be similar to component (capacitor, resistor, op-amp) failure in analog system
- ASIC component tested at 4 MHz during post manufacturing testing

C. FAILURE OF THE PARALLEL-TO-SERIAL CONVERTER
- Converts parallel data bus from ASIC into serial data bus to DAC
- Failure would corrupt data to DAC, resulting in wrong output values
- Failure would be detectable during periodic ACOT testing (accuracy, incorrect indication)
- Failures would be similar to component (capacitor, resistor, op-amp) failure in analog system

FEATURES OF THE DESIGN THAT SUPPORT LICENSING UNDER 10CFR50.59

D. FAILURE OF THE COMBINATORIAL LOGIC

- Monitors internal diagnostic signals & generates GA and TA
- Failure results in either a spurious GA, spurious TA, no GA or no TA
- Circuit is not part of process signal path. If false alarm, output of card will still be correct. If a GA or TA failed to activate, the output of the card will be incorrect because the condition causing the alarm also causes an error in the signal processing (ex. clock failure)
- The ASIC design enhances the GA feature of the 7300 System. In current analog system, the GA activates only when power, or the card fuse, fails.

E. FAILURE OF THE EXTERNAL MEMORY (SCRATCH-PAD)

- Stores intermediate values during string calculations being performed by the ASIC math function
- Failure results in data corruption during READ or WRITE operations, or a stuck bit (gate failure)
- If error is in LSB area, the card output may still be within specified accuracy. If error is in MSB area, results of calculation will be wrong and card output will not be within specified accuracy.
- ASIC chip design cannot lock-up. If error was intermittent, a "glitch" may appear at the end of the current cycle, but will be correct next cycle if error disappears. If error is permanent, then output will be wrong and detectable during periodic ACOT testing.

TEST PLAN
for
Electromagnetic Compatibility (EMC), Abnormal Environments, Seismic & Fault Testing

Equipment Identification

7300 (NXX) ASIC-based Reactor Protection System Replacement Modules

Associated Personality Modules

March 17, 1997

EMC TESTING

- Immunity and Emissions requirements Provided by EPRI 102323 Rev. 1 (DRAFT)
- No Exceptions to Frequency Ranges
- Emissions Effect on Adjacent 7300 Analog Card Addressed in Validation Test Plan
- Modules in Card Cage, in Cabinet, Configured as Typical Process Channels
- Conducted Emissions
  30 Hz to 400 MHz
- Radiated Emissions
  30 Hz to 1GHz
- Radiated Immunity - Continuous Wave
  30 Hz to 1GHz, 10 V/m
- Conducted Immunity - Continuos Wave
  30 Hz to 50 KHz, 6.3 VRMS
  50 KHz to 400 MHz, 7 VRMS

- Electrostatic Discharge
  8 kV Contact
- Fast Transient/Impulse
  3 kV into 50 ohm load
- Surge Tests
  3 kV peak

ABNORMAL ENVIRONMENT

Environmental Conditions

Cycle	Duration (hours)	Temperature (°F)	R.H. (%)	D.C. Voltage (Volts)
1	12	158	20	22
2	12	83	95	22
3	12	158	20	27
4	12	82	95	27

- Modules mounted in card cage, configured as typical process channel

SEISMIC TESTING

- Modules mounted in card cage, configured as typical process channel
- Attached to rigid test fixture
- Identical mounting and test parameters as 7300 analog card test

FAULT TESTS

- Faults applied to all non-1E connections
- Short Circuit
- Line to Ground
- Line to Line
- Fault Voltages
  125 VAC, 60 Hz
  580 VAC, 60 Hz
  125 VDC
  250 VDC

ACCEPTANCE CRITERIA

EMC

- Emissions per EPRI 102323
- Immunity
  - Maintain ability to perform safety function
  - No change of state

Abnormal Environment Test

Maintain accuracy deviation to a maximum of 0.1% of span per 50 °F change

Seismic Testing

- Maintain ability to perform safety function during and after SSE, zero residual effects
- Contact outputs shall not chatter 2 msec or greater
- No change of state

Fault Tests

- Maintain ability to perform safety function

Westinghouse Owners Group - EPRI Meeting with the US NRC

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Topical Report Submittal Schedule

WOG ASICS PROGRAM
PROPOSED NRC SUBMITTAL
SCHEDULE

MARCH	NRC MEETING
APRIL/MAY	System Description Design, Verification, & Validation Plan ASIC Chip test results
JUNE	NRC MEETING
JULY/AUGUST	NRC audit of Design, Verification, & Validation process Visit to ORNL/ATC/Westinghouse
SEPTEMBER	FMEA Results
OCTOBER	Validation test results
NOVEMBER	NRC MEETING
JANUARY '98	EQ Test results EMI/RFI test results Safety evaluation
FEBRUARY	NRC MEETING Resolve open items
MARCH	NRC issues SER

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NRC Summary of "Safety Critical Application for ASICs" Report

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Wrap-up