ARKANSAS NUCLEAR ONE - UNIT 2

DOCKET 50-368

CEN-71(A)-NP
SUPPLEMENT 1-NP
CORE PROTECTION CALCULATOR
SINGLE CHANNEL QUALIFICATION
TEST REPORT

SEPTEMBER 22, 1978

COMBUSTION ENGINEERING, INC.
NUCLEAR POWER SYSTEMS
POWER SYSTEMS GROUP
WINDSOR, CONNECTICUT

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CPC SINGLE CHANNEL QUALIFICATION TEST REPORT
SUPPLEMENT 1-P

1.0 INTRODUCTION

All changes to CPC/CEAC algorithm software and data constants made after completion of design qualification of the ANO-2 Cycle 1 software will be performed in accordance with Reference 1. In accordance with NRC Position 19.C, the assembly language implementation of these changes will undergo static and dynamic testing on an "acceptable test system". Reference 2 describes the Windsor Single Channel Test Facility and the verification tests to be performed to verify its acceptability for assembly language implementation testing of software modifications. Reference 3 describes verification tests that have been performed to ensure the acceptability of the Windsor Single Channel Test Facility for such testing of CPC/CEAC algorithm modifications.

Supplemental Single Channel Qualification testing has been required by the NRC in addition to the testing documented in Reference 3. The additional requirements are to define and execute a test program that demonstrates the Single Channel System is a qualified system for:

(a) Testing multi-variable transients,

(b) Execution of either option on CPC high power selection, and

(c) Testing of all interfaces between the CEAC, CPC, and Operators' Module.

The purpose of this document is to describe the supplemental verification testing performed on the test facility and to present the results and conclusions of those tests. This report is intended to fulfill all current outstanding testing requirements required by the NRC on the Windsor CPC/CEAC Single Channel Facility.

Multi-variable transient capability has been added to the Single Channel system in the form of a Dynamic Software Verification Test. The DSVT is a software test in which portions of the CPC executive and unused core are overlayed in order to process pre-determined time-variant CPC inputs to the CPC protection algorithms and data base. The CPC protection algorithms execute in an identical manner to on-line operation, however the inputs are "ideal" in that they can be synchronized with inputs vs. time that are used in corresponding CPC FORTRAN test cases. Thus, uncertainties associated with live analog input signal generation and transmission (signal generator accuracy and stability, line noise, CPC and signal generator timing, etc.) are eliminated. All inputs can be made to vary with time, synchronous with the FORTRAN code. The test is similar in concept and structure to the input-sweep test described in Reference 4, in that the overlays are used to match CPC and FORTRAN inputs while the protection algorithms and data are unchanged, and differences in results as compared to FORTRAN are attributable to either machine processing differences or software error.

Qualification testing was performed on the DSVT program with the execution of five Phase II dynamic test cases. The results of the DSVT test cases were compared to FORTRAN generated acceptance criteria for trip times.

Execution of either option on CPC high power selection is achieved by matching the calibrated neutron flux power to the core thermal power. This is performed by adjusting the value of the thermal power calibration constant (Point I.D. 068) to 1.0. All dynamic test cases performed in Reference 3 were re-executed with the thermal power calibration constant equal to 1.0. The results of these dynamic test cases were compared to FORTRAN generated acceptance criteria for trip times.

The qualification testing of CPC/CEAC/Operator's Module interfaces is achieved by the addition of a CEA Calculator to the Single Channel Test Facility. Dynamic test case #21, a non-target CEA drop, was re-executed using the CEAC to generate and transmit the resulting penalty factor. Acceptance criteria generated by the FORTRAN code was compared with the results of this test. The Operator's Module interface with the CPC and CEAC was exercised including check-out of status lamps, Point I.D.'s, and changes to addressable constants. All CPC/CEAC interface modes were also exercised.

2.0 SINGLE PARAMETER TEST DESCRIPTION

The single parameter testing consisted of execution of five single variable transients at nominal 100% power conditions. The transients were executed in order to satisfy the NRC requirements for exeuction of either option on CPC high power selection and testing of all interfaces between the CPC,CEAC,and Operator's Module. These five dynamic test cases are described in detail in Reference 3.

Execution of either option an CPC high power selection was accomplished by setting the thermal power calibration constant (P.I.D. 068) equal to 1.0. The testing of all interfaces between the CPC, CEAC, and Operator's Module consisted of verifying all interactions between these components. The verification included checkout of all status lamps on the operators' module, displaying point I.D.'s,changing addressable constants, and simulating all modes of penalty factor transmission.

2.1 SINGLE PARAMETER ACCEPTANCE CRITERIA

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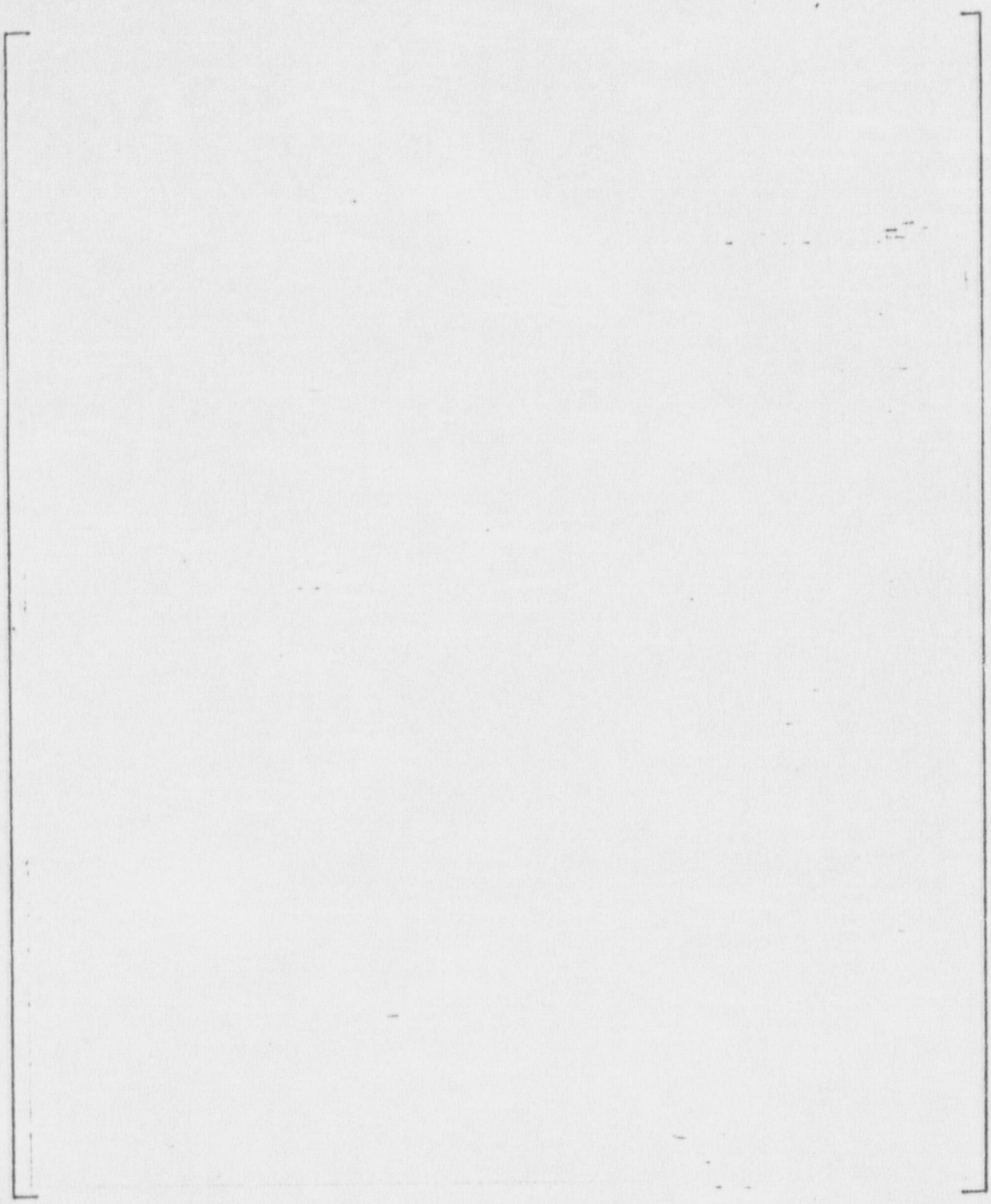


TABLE 2.1

SINGLE PARAMETER ACCEPTANCE CRITERIA

CASE NUMBER	TRIP TIME (MINIMUM)	TRIP TIME (MAXIMUM)
[redacted]		

DYNAMIC CASE 17 - PUMP SPEED DECREASE OF 10 PERCENT.

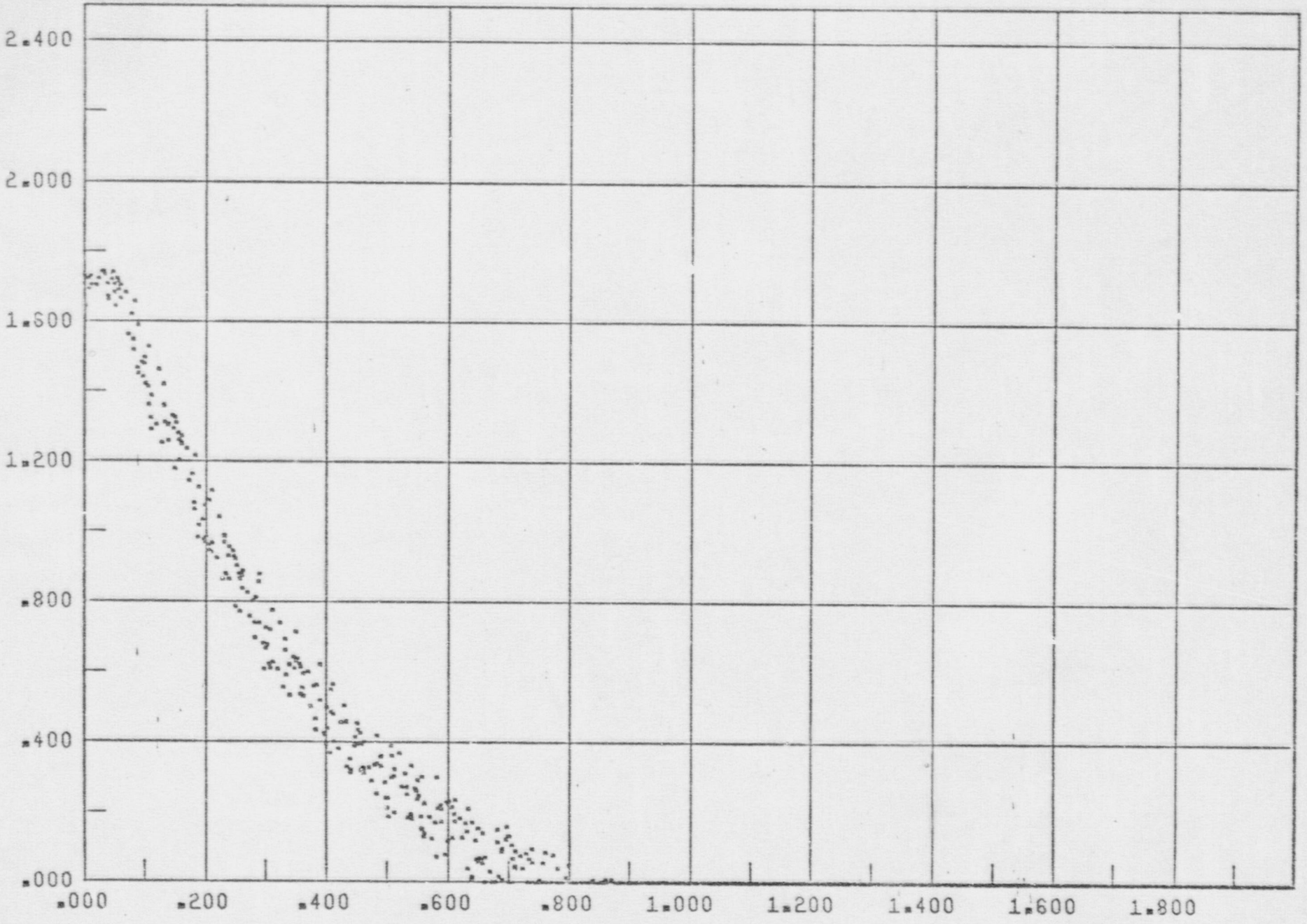


FIGURE 2.1

DYNAMIC CASE 17 - PUMP SPEED DECREASE . LEGEND =
OF 10 PERCENT.

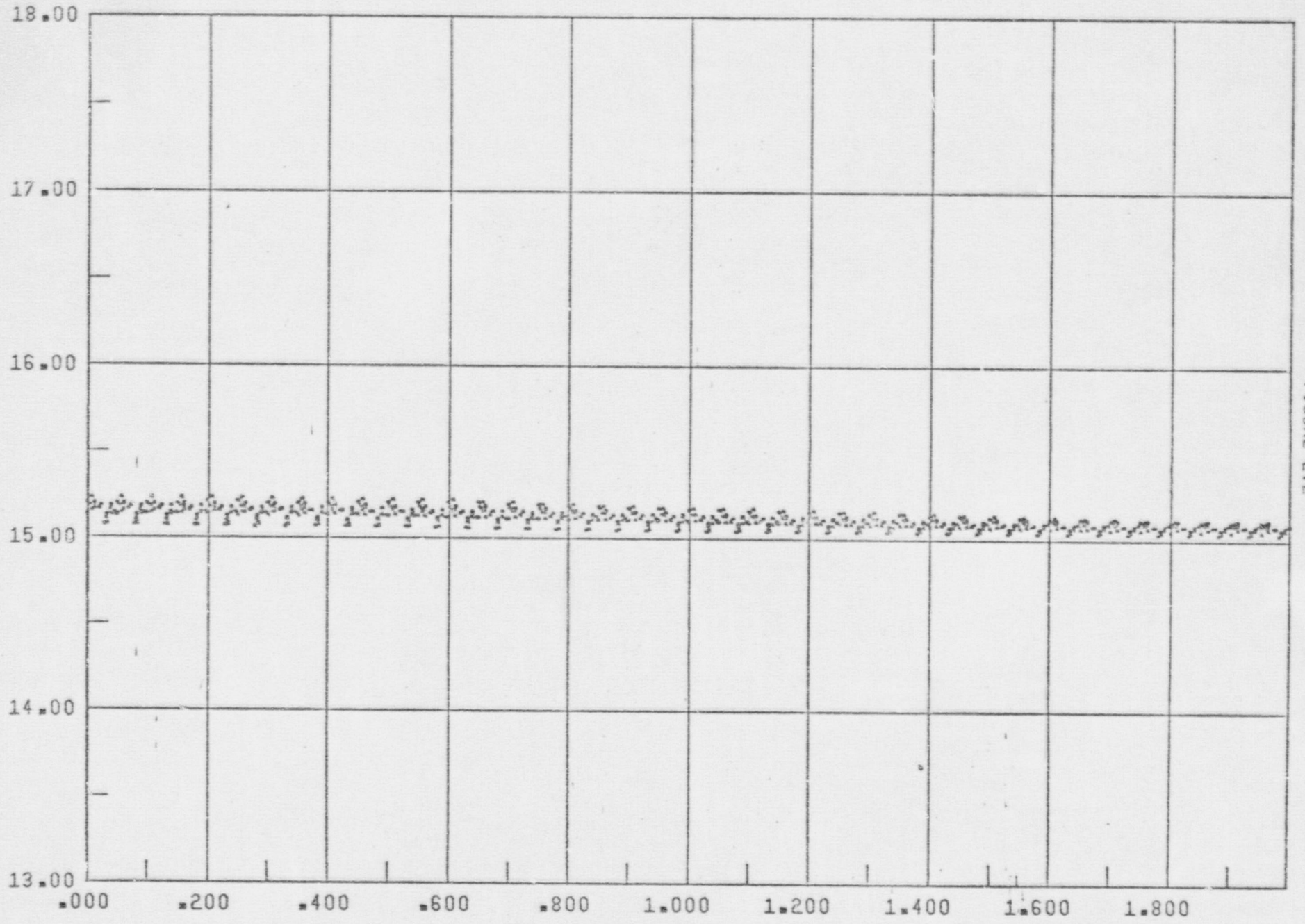


FIGURE 2.2

DYNAMIC CASE 18 - EXCORE DETECTOR INCR. EASE BY 20 PERCENT

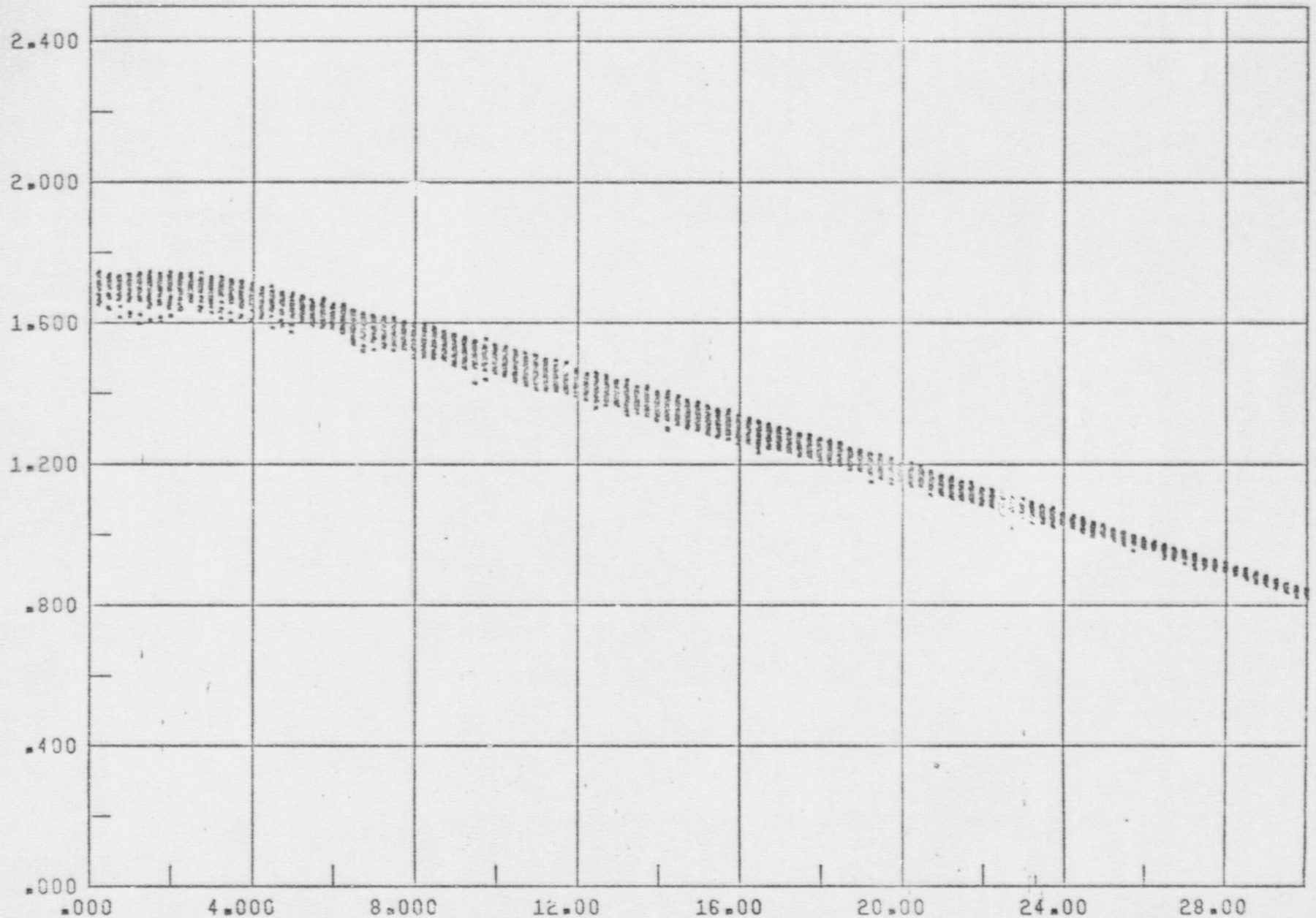


FIGURE 2.3

DYNAMIC CASE 18 - EXCORE DETECTOR INCR. EASE BY 20 PERCENT

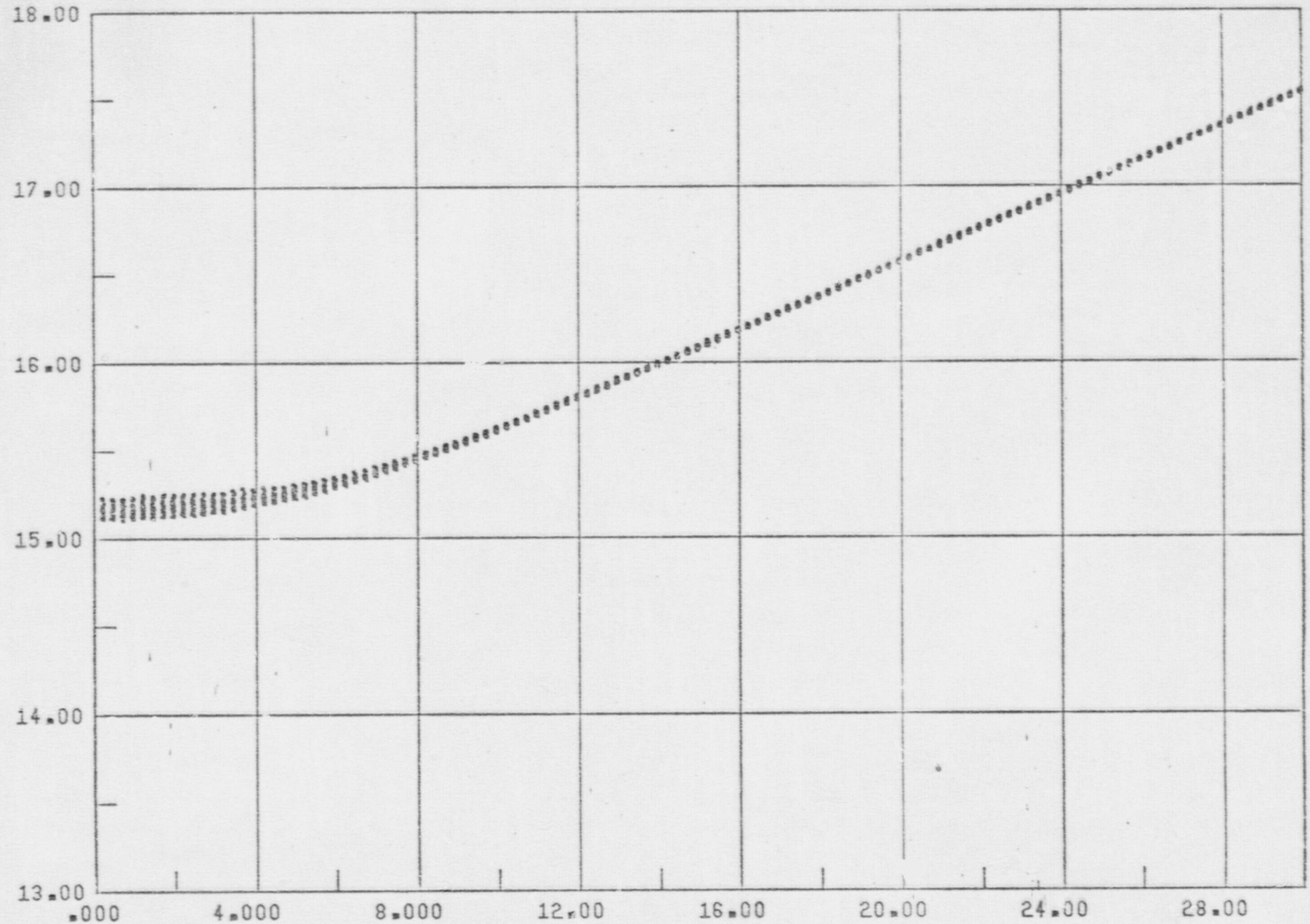


FIGURE 2.4

DYNAMIC CASE 19 - TC INCREASES BY 20 D. LEGEND =
EGREES.

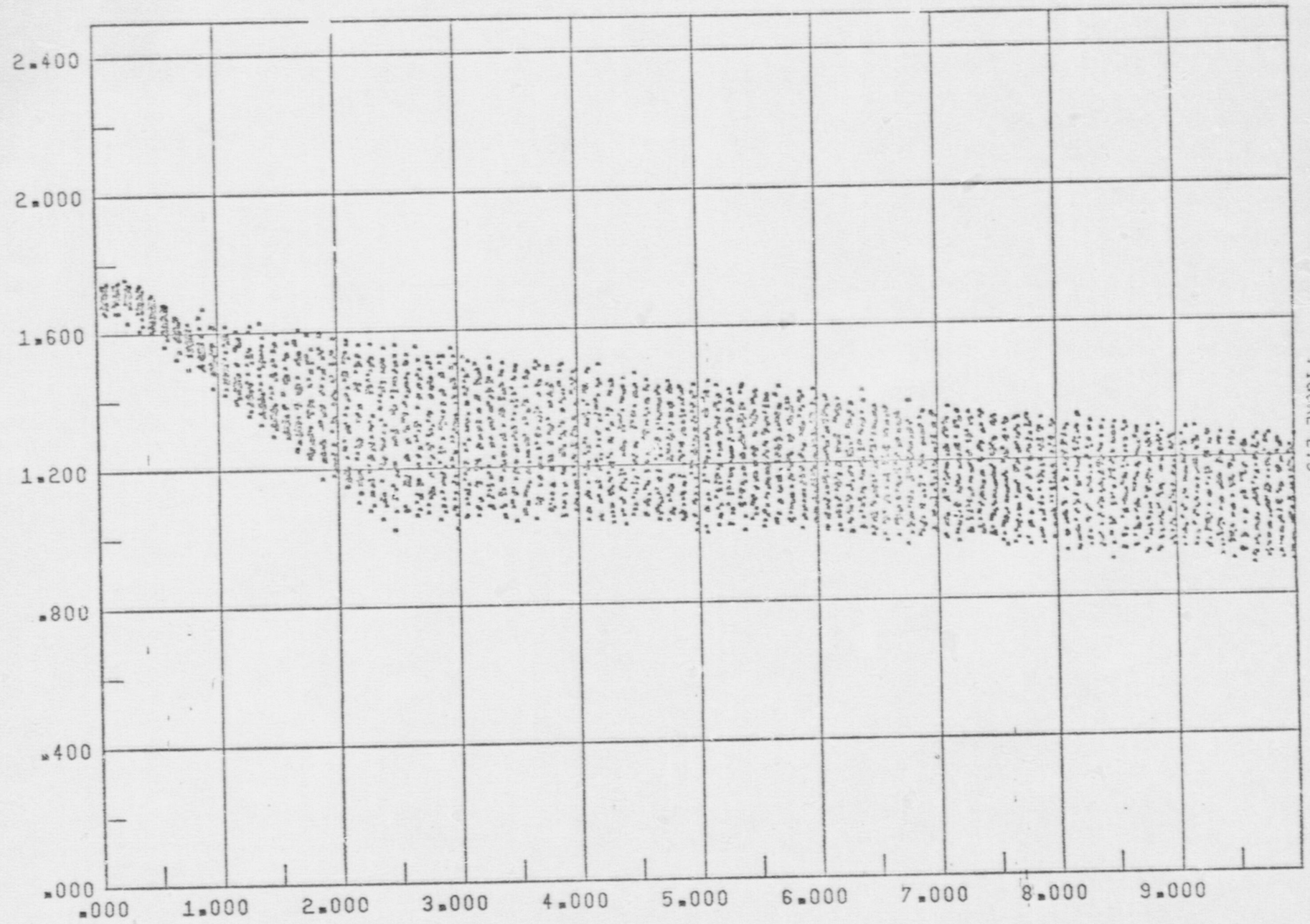


FIGURE 2.5

DYNAMIC CASE 19 - TC INCREASES BY 20 D. LEGEND
EGREES.

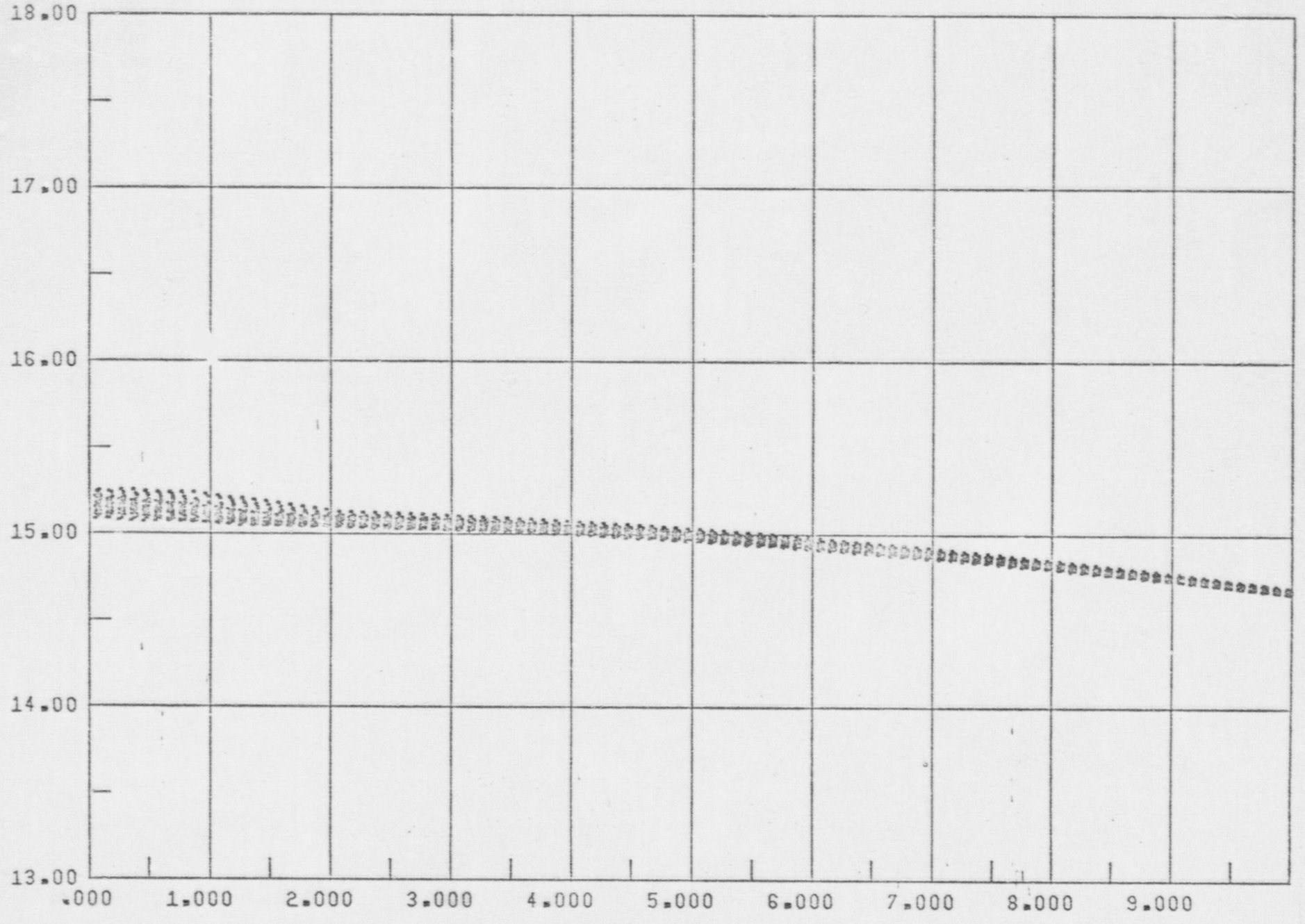


FIGURE 2.6

DYNAMIC CASE 20 - PRESSURE DECREASES B. LEGEND =
Y 200 PSIA.

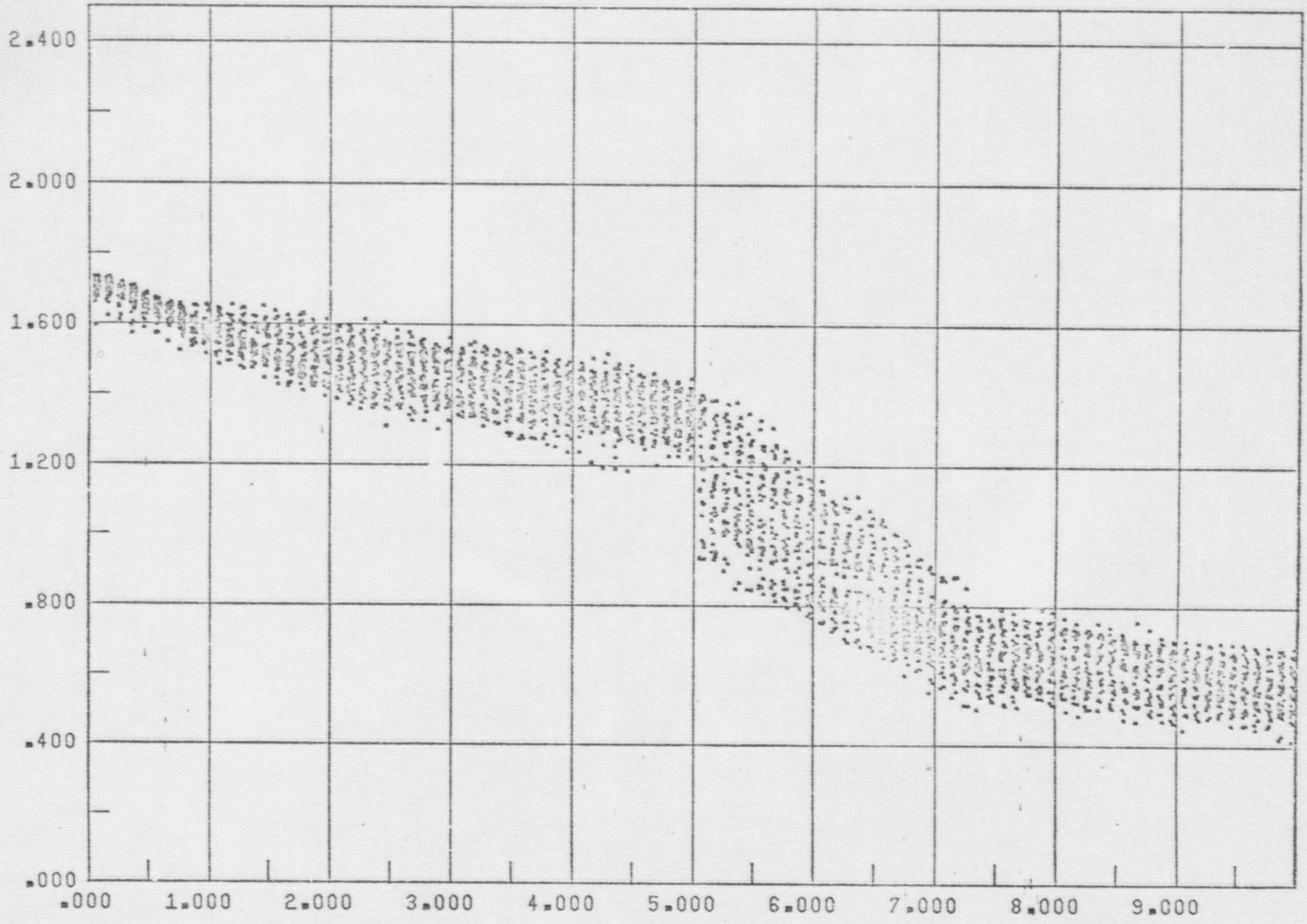


FIGURE 2.7

DYNAMIC CASE 20 - PRESSURE DECREASES B. LEGEND =
Y 200 PSIA.

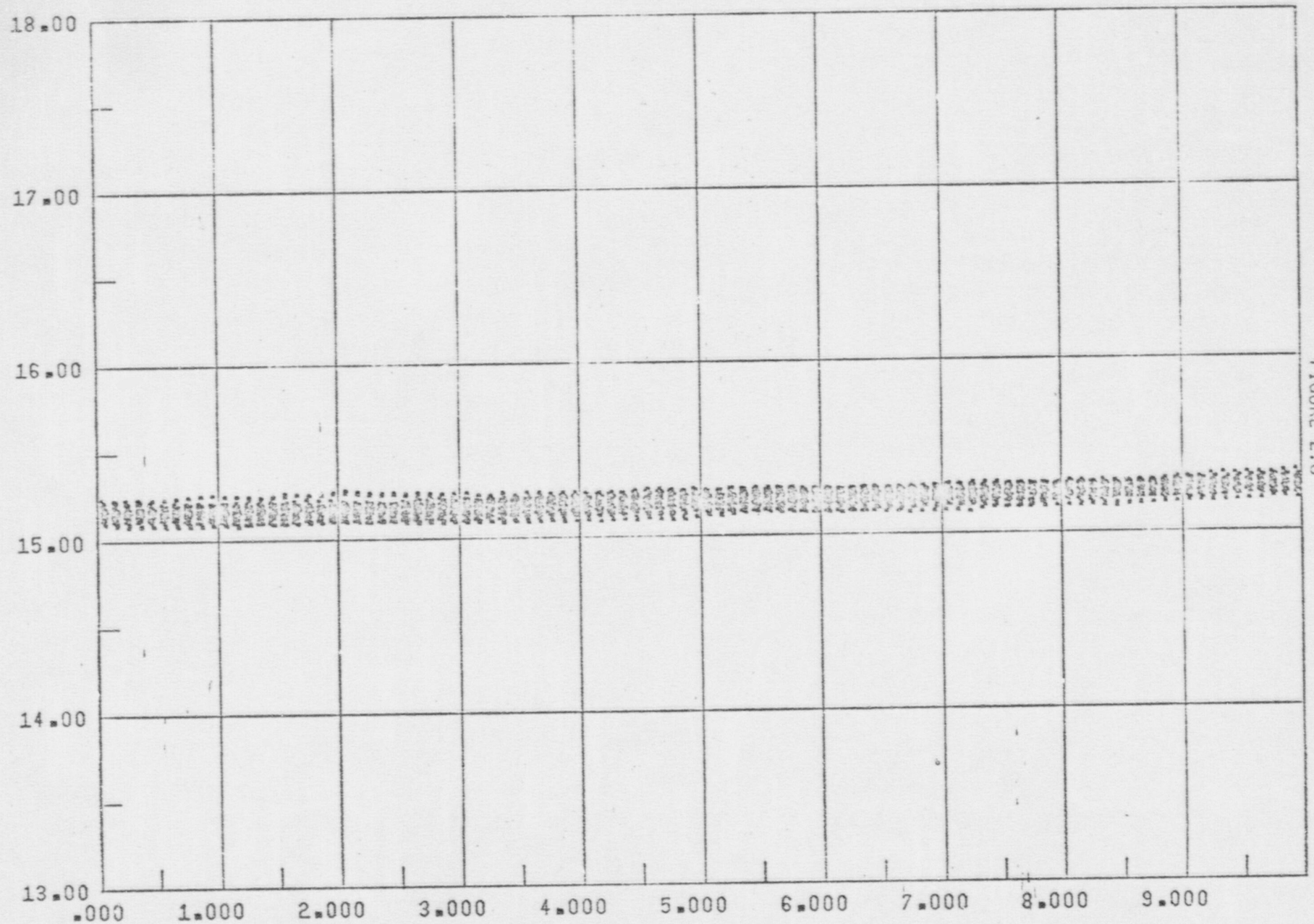


FIGURE 2.8

DYNAMIC CASE 21 - NON-TARGET CEA DROP

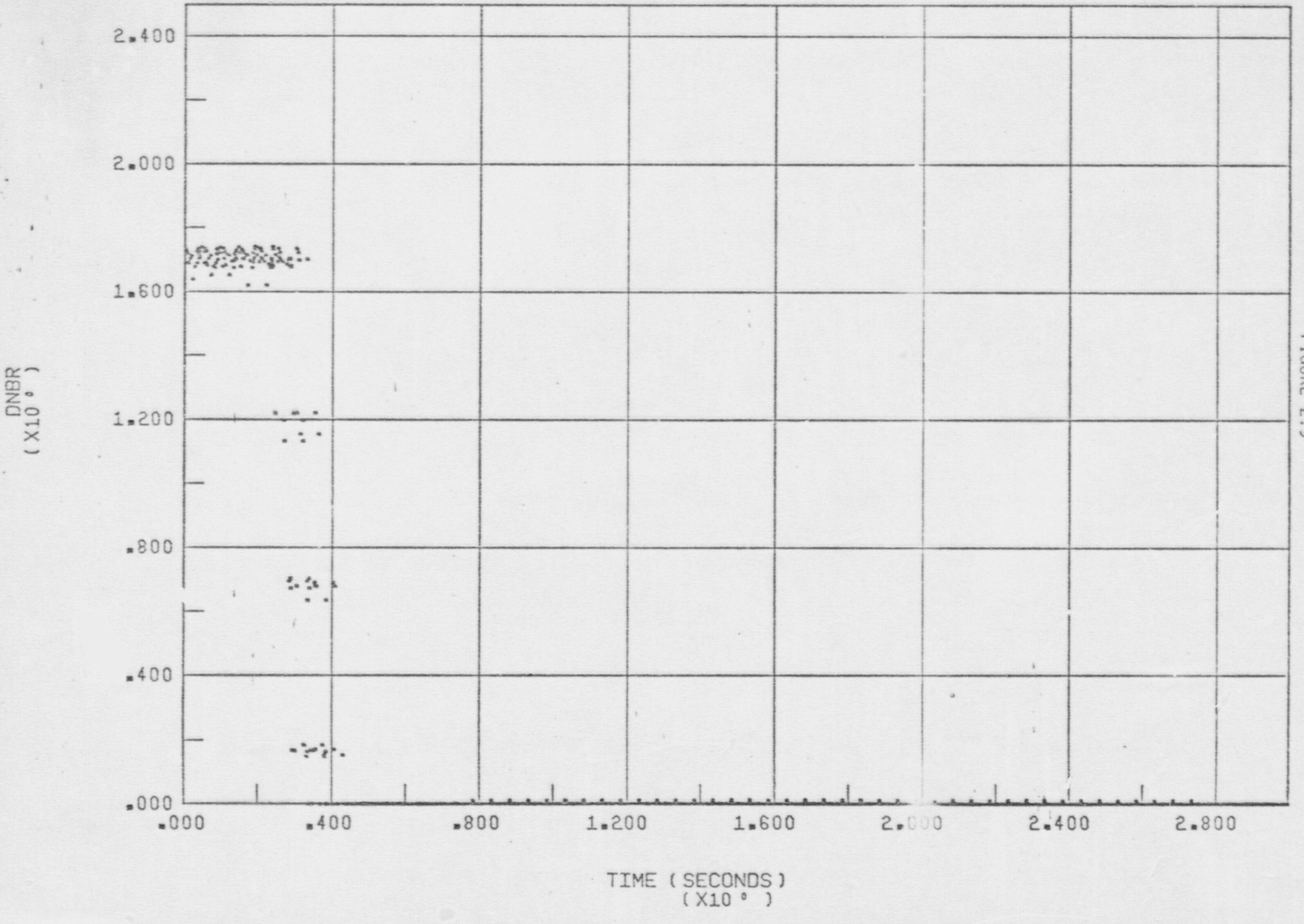


FIGURE 2.9

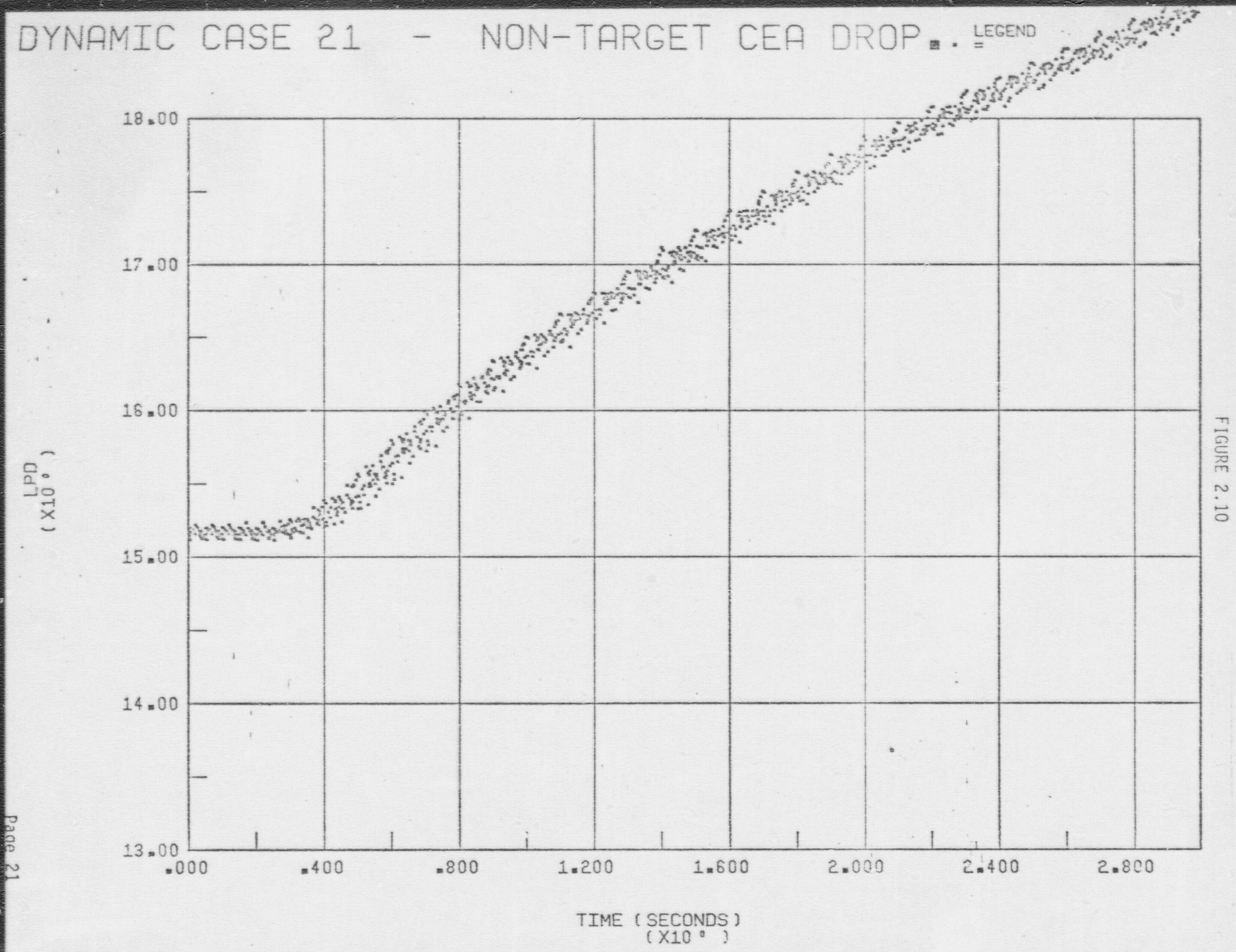

DYNAMIC CASE 21 - NON-TARGET CEA DROP..
LEGEND
=
18.00
17.00
16.00
15.00
14.00
13.00
LPD
(X10°)
.000
.400
.800
1.200
1.600
2.000
2.400
2.800
TIME (SECONDS)
(X10°)

FIGURE 2.10

2.2 DYNAMIC CASE 21 TEST PROCEDURE

Reference 3 contains test procedures for the five dynamic test cases. The procedure contained below replaces the procedure in Reference 3 for Dynamic Case 21. This modification reflects the addition of the CEA Calculator to the test.

(1) Configure the hardware per Figure 2.11.

(2) Ensure that the appropriate CPC/CEAC software has been loaded into the Single Channel system and is functioning properly.

(3) Adjust the CPC System I/O Simulator for the inputs required by Table 1.3.6 of Reference 3.

(4) Adjust the TR-48 analog computer and make the appropriate connections from the TR-48 to the CPC System I/O Simulator jack panel to produce the required ramp rate listed in Section 1.3 of Reference 3 for Dynamic Case 21. Detailed information concerning TR-48 adjustment and connection for Dynamic Case 21 may be found in Appendix A.

(5) Ensure that the DNBR (margin) analog output, LPD (margin) analog output, input voltage ramp, timing signal, and DNBR contact closure output are connected to the strip chart recorder

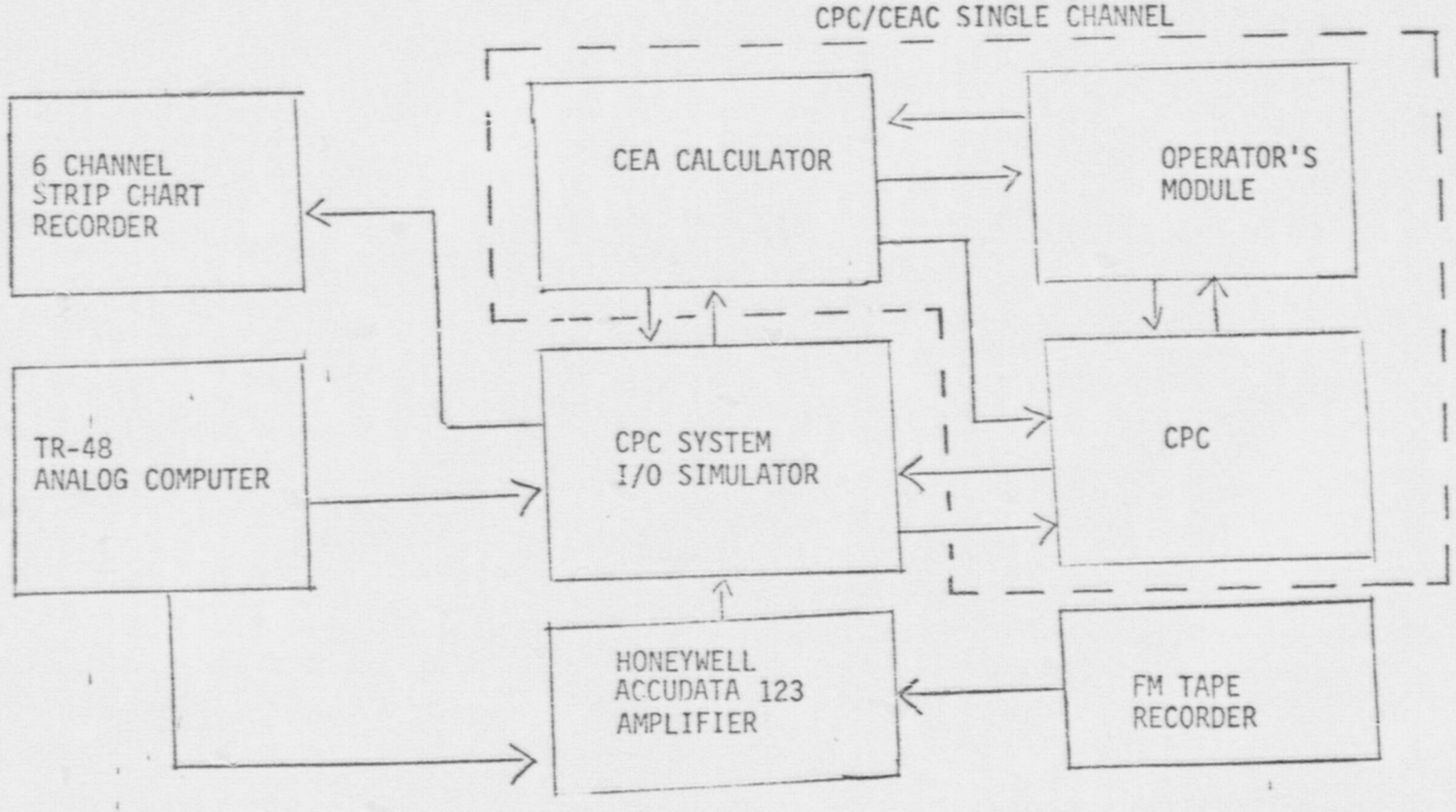
(6) Place the strip chart recorder speed selector to 25 mm/sec.

(7) Initiate the transient (per Appendix A) and halt the strip chart recorder at the conclusion of the transient.

(8) Repeat steps (3) through (7) ten times. Annotate all strip chart recordings with proper identification including case number and channel allocation and sensitivity.

FIGURE 2.11

CPC/CEAC SINGLE CHANNEL TEST FACILITY



2.3 SINGLE PARAMETER TEST RESULTS

The five dynamic test cases were executed in accordance with Section 3.0 of Reference 3 and Section 2.2 of this document. The trip times were determined from strip chart recordings and are contained in Table 2.2. The minimum and maximum trip times for each test case are contained in the following table.

[

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In all cases, the dynamic test results fall within the trip time acceptance criteria given in Table 2.1.

All CPC/CEAC/Operator's Module Interfaces were tested during the single parameter tests and all interface interactions described in Section 2.0 were verified.

TABLE 2.2

SINGLE PARAMETER TEST RESULTS

[

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3.0 DYNAMIC SOFTWARE VERIFICATION TEST DESCRIPTION

The Dynamic Software Verification Test (DSVT) was added to the Single Channel capabilities to provide a means of performing multi-variable transients. Qualification of DSVT as a multi-variable test consisted of execution of five dynamic test cases and comparison of the test results to FORTRAN generated acceptance criteria. The five dynamic test cases were taken from the Phase II test series and are described in Table 3.1. The acceptance criteria for these test cases consisted of trip times.

To facilitate the test results data reduction, the DSVT software automatically records the DNBR and LPD trip times in Point I.D. locations 098 and 096, respectively. The values contained in these Point I.D. locations produced the test results for each test case.

3.1 DSVT ACCEPTANCE CRITERIA

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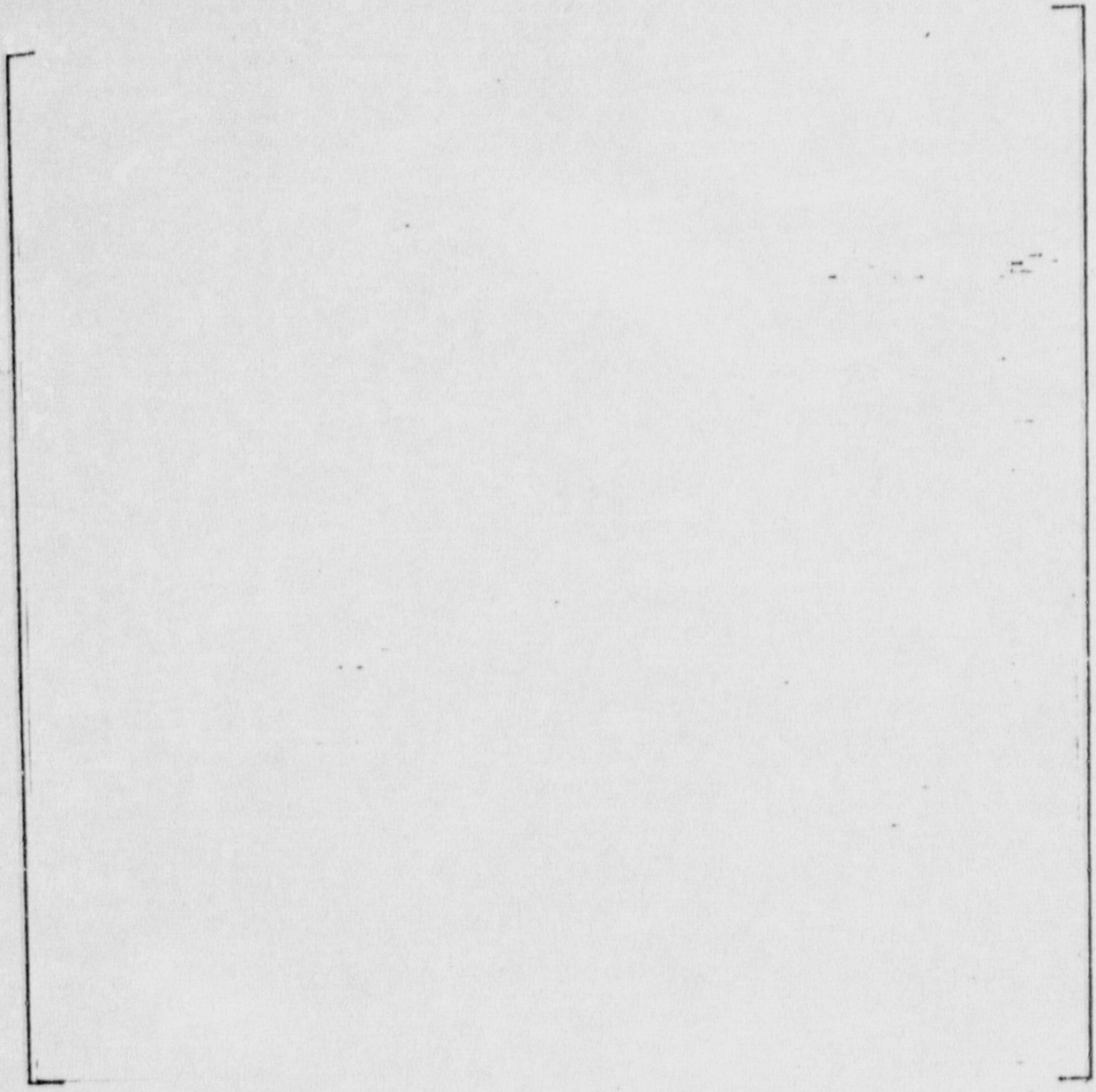

TABLE 3.1

DYNAMIC SOFTWARE VERIFICATION TEST CASES

PHASE II CASE NUMBER	TEST CASE DESCRIPTION
1	4/4 RC Pump Loss of Flow
3	1/3 RC Pump Loss of Flow
7	Single Full Length CEA Drop
12	Uncontrolled Sequential CEA Withdrawal
16	Primary Coolant Depressurization

TABLE 3.2

DSVT ACCEPTANCE CRITERIA
(without 50 millisecond interval modification)

CASE NUMBER	DNBR Trip Time (Minimum)	DNBR Trip Time (Maximum)	LPD Trip Time (Minimum)	LPD Trip Time (Maximum)
[				]

TABLE 3.3

DSVT ACCEPTANCE CRITERIA
(with 50 millisecond interval modification)

CASE NUMBER	DNBR Trip Time (Minimum)	DNBR Trip Time (Maximum)	LPD Trip Time (Minimum)	LPD Trip Time (Maximum)
[				]

3.2 DSVT TEST PROCEDURE

(1) Ensure that the appropriate CPC software has been loaded into the Single Channel CPC.

(2) Load the DSVT overlay via the floppy disk.

(3) Insert the DSVT Input disk in the floppy disk drive.

(4) Type the DSVT test case number desired via the teletype.

(5) Initiate the transient by pushing the white spare button on the operator's module.

(6) Run each of the five test cases indicated in Table 3.1. Record the DNBR and LPD trip times contained in Point I.D.'s 098 and 096, respectively.

3.3 DSVT TEST RESULTS

The five DSVT test cases in Table 3.1 were executed according to the procedure contained in Section 3.2 Trip times for each case were taken from Point I.D. 096 for LPD and Point I.D. 098 for DNBR. The results for each test case are contained in Table 3.4. For all test cases the test results agree with the FORTRAN generated acceptance criteria contained in Table 3.3.

TABLE 3.4

DSVT TEST RESULTS

CASE NUMBER	DNBR TRIP TIME (Point I.D. 098)	LPD TRIP TIME (Point I.D. 096)

4.0 CONCLUSIONS

Five single parameter transients have been executed on the Windsor Single Channel Test Facility and have demonstrated the execution of either option on CPC high power selction. One of the five test cases exercised the CEAC CPC interface through generation of a penalty factor from a simulated CEA drop. Furthur testing was performed to exercise interfaces among the CEAC, CPC, and Operator's Module. Acceptance criteria for the transient test cases were generated as described in Section 2.1. For all test cases the test results fall within the acceptance criteria ranges. Consistent with the objectives in Section 1.1 of Reference 3, the Single Channel Test Facility has been shown to be an acceptable test system for CPC software modifications.

The DSVT qualification tests were executed on the Windsor Single Channel Test Facility. Acceptance criteria for those tests were generated as described in Section 3.1. For all test cases, the test results agree with the acceptance critera. Consistent with the objectives of Section 3.0, DSVT has been shown to be an acceptable multi-variable testing mechanism for Phase II testing of software modifications.

5.0 REFERENCES

(1) CEN-39(A)-P, CPC Protection Algorithm Software Change Procedure, October 1976.

(2) CEN-40(A)-P, CPC Single Channel System Verification Test, October 1976.

(3) CEN-71(A)-P, Core Protection Calculator Single Channel Qualification Test Report, October 1977.

(4) CEN-72(A)-P, Core Protection Calculator System Phase I Design Qualification Test Report, October 1977.

APPENDIX A

A.1 Dynamic Test Case 21

Dynamic Test Case 21 is a single CEA drop from 100% withdrawn to 100% inserted in 3.0 seconds. The dropped CEA is CEA #1.

(1) Voltage Settings:

P(14) = 2.000 v

P(24) = 1.000 v

P(40) = 3.333 v

(2) S(2) = right

(3) Make the above settings. Push RESET and then OPERATE. Connect the output of amplifier 30 to the input of a Honeywell Accudata 123 amp. Adjust the Honeywell amp for a gain of 5 and zero offset. Connect the output of the Honeywell amp to alternate input jack J21 on the front panel of the CPC System I/O Simulator cabinet.

(4) Place the strip chart speed selector to 25 mm/sec immediately prior to initiation of the transient.

(5) The transient is initiated by placing S(2) in the left position. The initial conditions are reset by placing S(2) in its original position.