



ENERGY INCORPORATED

## PROCEDURE

## DESCRIPTION

TEST PROCEDURE FOR PERFORMANCE AND ISOLATION TESTING OF 1E  
ANALOG AND DIGITAL ISOLATORS

PREPARED BY

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DATE

8-30-84

CONTRACT NO. \_\_\_\_\_

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## REVISIONS

NOTE: All revisions are flagged with the symbol  $\triangle N$  in the right margin where N is the number of the revision.

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FOR INFORMATION ONLY

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PROCEDURE NO.

EIP-24

JOB CODE - S/N

PAGE 1 OF 33

## TABLE OF CONTENTS

	<u>PAGE</u>
1.0 PURPOSE.....	6
2.0 RESPONSIBILITIES.....	6
2.1 Test Engineer.....	6
2.2 Quality Control Representative.....	7
3.0 REFERENCE DOCUMENTS.....	7
3.1 Required Documents.....	7
3.2 Other References.....	8
3.3 Test Procedure Use.....	8
3.4 Procedure Documentation.....	8
4.0 TEST EQUIPMENT REQUIRED.....	9
5.0 TEST SIGNAL CHARACTERISTICS.....	9
6.0 SAFETY REQUIREMENTS.....	10
7.0 PRETEST.....	10
8.0 TEST PERFORMANCE.....	11
8.1 Digital Isolator Functional Test.....	11
8.2 Analog Isolator Functional Test.....	12
8.3 HI-Potential Test (DC).....	13
8.4 HI-Potential Test (AC).....	14
8.5 Surge Withstand Capability Test.....	15
8.6 Analog Isolator Thermal Drift.....	18
8.7 Analog Isolator Linearity.....	19
8.8 Analog Isolator Power Supply Drift.....	19
8.9 Analog Isolator Interchannel Effects at Saturation.....	20

REVISION NO.  
0

PROCEDURE NO. EIP-24  
JOB CODE - S/N

PAGE 2 OF 33

TABLE OF CONTENTS (continued)

	<u>PAGE</u>
8.10 Analog Isolator Failure Mode Isolation.....	20
8.11 Analog Isolator Bandwidth.....	21
9.0 POSTTEST.....	22
10.0 ACCEPTANCE CRITERIA.....	23
11.0 RETEST.....	24
12.0 FINAL REVIEW.....	25

REVISION NO.  
0

PROCEDURE NO. EIP-24  
JOB CODE - S/N

PAGE 3 OF 33

LIST OF FIGURES

<u>FIGURE</u>	<u>TITLE</u>	<u>PAGE</u>
1	Test Connector.....	26
2	Digital Isolator Functional Test Configuration.....	27
3	Digital Isolator Isolation Test Configuration.....	28
4	Analog Isolator Functional Test Configuration.....	29
5	Analog Isolator Isolation Test Configuration.....	30
6	Surge Withstand Transverse Mode Test Configuration.....	31
7	Surge Withstand Common Mode Test Configuration.....	32
8	Bandwidth Test Configuration.....	33

REVISION NO.

0

PROCEDURE NO. EIP-24

JOB CODE - S/N

PAGE 4 OF 33

FORM E-036  
REV. 0, 5/81



LIST OF ATTACHMENTS

ATTACHMENT

TITLE

1	TEST PROCEDURES TO BE USED
2	TEST EQUIPMENT USE LOG
3	BURN IN
4	DIGITAL ISOLATOR FUNCTIONAL TEST
5	NOT USED
6A	ANALOG ISOLATOR FUNCTIONAL TEST ASSEMBLY -1, -51, -60
6B	ANALOG ISOLATOR FUNCTIONAL TEST ASSEMBLY -2, -52
6C	ANALOG ISOLATOR FUNCTIONAL TEST ASSEMBLY -3, -58
6D	ANALOG ISOLATOR FUNCTIONAL TEST ASSEMBLY -4, -56
6E	ANALOG ISOLATOR FUNCTIONAL TEST ASSEMBLY -5
6F	ANALOG ISOLATOR FUNCTIONAL TEST ASSEMBLY -6
6G	ANALOG ISOLATOR FUNCTIONAL TEST ASSEMBLY -7
6H	ANALOG ISOLATOR FUNCTIONAL TEST ASSEMBLY -8
6J	ANALOG ISOLATOR FUNCTIONAL TEST ASSEMBLY -9
6K	ANALOG ISOLATOR FUNCTIONAL TEST ASSEMBLY -10
6L	ANALOG ISOLATOR FUNCTIONAL TEST ASSEMBLY -53
7A	DIGITAL ISOLATOR HI-POTENTIAL TEST (DC)
7B	ANALOG ISOLATOR HI-POTENTIAL TEST (DC)
8A	DIGITAL ISOLATOR HI-POTENTIAL TEST (AC)
8B	ANALOG ISOLATOR HI-POTENTIAL TEST (AC)
9	SURGE WITHSTAND CAPABILITY TEST
10	ANALOG ISOLATOR THERMAL DRIFT (3 PAGES)
11	ANALOG ISOLATOR LINEARITY
12	ANALOG ISOLATOR POWER SUPPLY DRIFT (2 PAGES)
13	ANALOG ISOLATOR INTERCHANNEL EFFECT AT SATURATION
14	ANALOG ISOLATOR FAILURE MODE ISOLATION
15	ANALOG ISOLATOR BANDWIDTH

REVISION NO.  
0

PROCEDURE NO. EIP-24  
JOB CODE - S/N

PAGE 5 OF 33

EI-146  
(REV. 5/84)

## 1.0 PURPOSE

This procedure provides a document verifying the performance and electrical isolation of Class 1E analog and digital isolators.

Transient voltages usually are capacitively or magnetically coupled from a high voltage source of electrical noise into secondary circuits or control wiring. Since these voltages may appear unsuppressed across connection points of components associated with the protective system, it must be determined that they will not cause a failure or a misoperation of the system.

## 2.0 RESPONSIBILITIES

### 2.1 Testing Engineer

It is the responsibility of the test engineer to:

- (1) Provide the necessary test equipment.
- (2) Ensure the correct interconnection of the test equipment.
- (3) Perform the test.
- (4) Document the derived data.
- (5) Enter the test records in the appropriate project files.
- (6) Be trained to level II or III per EI QAP 10-2.
- (7) Notify the QC department of the pending test.

REVISION NO.

0

PROCEDURE NO. EIP-24

JOB CODE - S/N

PAGE 6 OF 33

## 2.2 Quality Control Representative

It is the responsibility of the quality control representative to:

- (1) Verify test is conducted per the procedure.
- (2) Verify data taken.
- (3) Verify all equipment used has a current and valid calibration sticker or certificate.
- (4) Verify proper disposition and storage of test records.
- (5) Obtain and maintain the test record copy of the procedure, data sheets, and all applicable drawings.

## 3.0 REFERENCE DOCUMENTS

### 3.1 Required Documents

Use the latest revision of the following documents:

- (1) EI Drawing 00798, Quad Class 1E Analog Isolation Amplifier Assembly.
- (2) EI Drawing 00796, Class 1E Analog Isolation Amplifier Schematic.
- (3) EI Drawing 01026, Class 1E Digital Isolator Amplifier Assembly
- (4) EI Drawing 01030, Class 1E Digital Isolator Amplifier Schematic.

REVISION NO. 0	PROCEDURE NO. <u>EIP-24</u> JOB CODE - S/N	PAGE 7 OF 33
-------------------	---	--------------

### 3.2 Other References

- (1) IEEE Standard Guide, "IEEE 381-1977, Standard Criteria for Type Tests of Class 1E Modules Used in Nuclear Power Generating Stations".
- (2) IEEE Standard Guide, "IEEE 467-1980, Standard Quality Assurance Program Requirements for the Design and Manufacture of Class 1E Instrumentation and Electric Equipment for Nuclear Power Generating Stations".
- (3) IEEE Standard Guide, "IEEE 472-1974, Guide for Surge Withstand Capability (SWC) Tests (ANSI C 37.90-1978)".

### 3.3 Test Procedures Used

The tests to be used are job specific. The tests to be run will be specified by the program manager and listed with applicable attachments on Attachment 1.

### 3.4 Procedure Documentation

Attachments used will (when completed) become part of the test procedure documentation. They will be incorporated into the test record copy of the test and submitted to project management for final review.

## 4.0 TEST EQUIPMENT REQUIRED

- (1) Hipot Tester, Hipotronics Model HD125 or equivalent
- (2) Digital Multimeter (DMM), Fluke Model 8000A or equivalent
- (3) Dual Power Supply  $\pm 15$  VDC output
- (4) 5-Volt Power Supply

REVISION NO. 0	PROCEDURE NO. <u>FIP-24</u> JOB CODE - S/N	PAGE 8 OF 33
-------------------	---	--------------

- (5) 0-150 VDC Power Supply
- (6) Surge Transient Generator, Velonex Model 510 or equivalent
- (7) System Calibrator, Fluke 382A or equivalent
- (8) 4-Card Isolator Test Fixture
- (9) Test Connector, EI (see Figure 1)
- (10) Isolator Frame Assembly, P/N 00645-1 or P/N 01000-1
- (11) Variac - 120 VAC
- (12) Test Leads as Required
- (13) Oscilloscope, Tektronics 465A or equivalent 2 MHz Bandwidth Minimum, with External Trigger
- (14) Function Generator, Square Wave, Exact 734 or equivalent

## 5.0 TEST SIGNAL CHARACTERISTICS

### 5.1 Hi-Potential Isolation Test

5.1.1 Peak Voltage: 3 KVDC, for 15 seconds

5.1.2 Peak Voltage: 1.5 KVAC, 60 Hz for One Minute

### 5.2 Digital Isolator Test

- (1) Input voltages as specified on the data sheet.

REVISION NO.  
0

PROCEDURE NO. EIP-24

JOB CODE - S/N

PAGE 9 OF 33

### 5.3 Analog Isolator Test

- (1) Input voltages or current as specified on the appropriate data sheet.

### 5.4 Surge Withstand Test

- (1) Peak Voltage: 2.5 KV.
- (2) Frequency: 1.0 to 1.5 MHz (no adjustment).
- (3) Waveshape: First half of cycle to be full peak voltage, then envelope decays to 50% of the crest value of the first peak in not less than six  $\mu$ sec from the start of the wave (no adjustment).
- (4) Repetition: The test wave shall be applied to the test specimen 60 times per second for two seconds.
- (5) Source Impedance: 150 ohms.

### 6.0 SAFETY REQUIREMENTS

All safety precautions as noted in the operating manual of the Hipotronics hipot tester will be adhered to.

All safety precautions as noted in the operating manual of the Velonex Surge Transient Generator will be adhered to.

Caution: Lethal voltage will be present during the performance of these tests.

### 7.0 PRETEST

- (1) Fabricate test connector per Figure 1 (if needed).

REVISION NO. 0	PROCEDURE NO. <u>FIP-24</u> JOB CODE - S/N	PAGE 10 OF 33
-------------------	---	---------------



- (2) Remove all keys from edgeboard connectors in prototype isolator frame (if used).
- (3) Record all test equipment used on Attachment 2.
- (4) Connect +5 V and  $\pm 15$  V power to isolator frame per Figure 1.
- (5) Adjust the +5-V power supply for  $5 \text{ V} \pm 10 \text{ mV}$ .
- (6) Adjust the  $\pm 15$ -V power supply for  $\pm 15 \text{ V} \pm 10 \text{ mV}$ .
- (7) Allow all parts to operate for burn-in time specified on Attachment 3.
- (8) Record serial numbers of each group.

## 8.0 TEST PERFORMANCE

### 8.1 Digital Isolator Functional Test

- (1) Install digital isolator cards in the isolator frame. Record the serial numbers of the installed cards on the data sheet (Attachment 4).
- (2) Connect a voltmeter and the calibrator to the test connector in accordance with Figure 2.
- (3) Turn on the 5-volt power supply.
- (4) Raise the calibrator voltage until the output voltmeter reads:  $1 \text{ V} \pm 0.05 \text{ V}$ . Record the calibrator output voltage on the data sheet.

REVISION NO.

0

PROCEDURE NO. EIP-24

JOB CODE - S/N

PAGE 11 OF 33

FORM E-036  
REV. 0, 5/81

- (5) Raise the calibrator voltage until the output voltmeter reads  $3.8 \text{ V} \pm 0.05 \text{ V}$ . Record the calibrator output voltage on the data sheet.
- (6) Raise the calibrator voltage to  $48 \text{ V} \pm 0.1 \text{ V}$ . Record the output voltmeter reading on the data sheet.
- (7) Repeat (2) through (6) for the remaining channels for outputs as listed on Figure 2.
- (8) Repeat steps (2) through (7) for all of the cards.

## 8.2 Analog Isolator Functional Test

- (1) Record the serial numbers of the installed cards on the data sheet (Attachment 6).
- (2) Connect the output of the  $\pm 15\text{-V}$  power supply to the test connector per Figure 4.
- (3) Turn on the  $\pm 15\text{-V}$  power supply to the isolator frame and allow 10 minutes for warmup.
- (4) Connect the test connectors to appropriate J1- and J0- connectors on the isolator frame.
- (5) Turn on the system calibrator and adjust the output for "INPUT LOW" as specified on the data sheet  $\pm 0.1\%$ .
- (6) Adjust the "zero" potentiometers on cards 1 and 2 for "OUTPUT LOW" as specified on the data sheet  $\pm 0.1\%$  on channels 1 through 4 of each card.
- (7) Adjust the system calibrator output for "INPUT HIGH" as specified on the data sheet  $\pm 0.1\%$ .

REVISION NO. 0	PROCEDURE NO. <u>EIP-24</u> JOB CODE - S/N	PAGE 12 OF 33
-------------------	---	---------------

- (8) Adjust the "GAIN" potentiometers on cards 1 and 2 for output as specified on the data sheet  $\pm 0.1\%$  on channels 1 through 4 of each card.
- (9) Repeat steps (5) through (8) as required, to verify that both adjustments will reach their final desired values.
- (10) Record the output data on the data sheet.
- (11) Turn off the dual power supply.

### 8.3 Hi-Potential Test (DC)

CAUTION: Lethal voltage will be present during the performance of the following steps:

- (1) Record the serial numbers of the installed cards on the data sheet (Attachment 7).
- (2) Connect the Hipot Tester to all channels of both cards per Figure 3 (for digital isolators) or Figure 5 (for analog isolators.)
- (3) Turn on the Hipot Tester and set the "Raise Voltage" control to 0.
- (4) Set up the Hipot Tester per the characteristics specified in 5.1.1.
- (5) Gradually increase the voltage applied to the isolator.
- (6) Stop increasing the voltage when 3 KV is reached or the isolator breaks down.
- (7) Record the leakage current on the data sheet.

REVISION NO. 0	PROCEDURE NO. <u>EIP-24</u> JOB CODE - S/N	PAGE 13 OF 33
-------------------	---	---------------

- (8) Turn off the Hipot Tester.
- (9) Repeat (1) through (8) for the remaining cards connecting the test connectors to J12 and J02, J13 and J03, etc., as required.

#### 8.4 Hi-Potential Test (AC)

CAUTION: Lethal voltage will be present during the performance of the following steps:

- (1) Record the serial numbers of the installed cards on the data sheet (Attachment 8).
- (2) Connect the Hipot Tester to all channels of one of the cards per Figure 3 (for digital cards) or Figure 5 (for analog cards).
- (3) Turn on the Hipot Tester and set the "Raise Voltage" control to 0.
- (4) Set up the Hipot Tester per the characteristics specified in 5.1.2.
- (5) Gradually increase the voltage applied to the isolator.
- (6) Stop increasing the voltage when 1.5 KVAC is reached or the isolator breaks down.
- (7) Let the test run for one minute.
- (8) Record the leakage current on the data sheet.
- (9) Turn off the Hipot Tester.
- (10) Repeat (1) through (9) for the remaining cards by connecting the test connectors to J12 and J02, J13 and J03, etc., as required.

## 8.5 Surge Withstand Capability Test

### 8.5.1 Pretest Setup

- (1) Plug the Surge Transient Generator and Oscilloscope into a 115-V, 60-Hz source. Activate the power switch on each.
- (2) Configure the scope for external trigger.
- (3) Connect the SCOPE TRIGGER output of the Velonex 510 to the external trigger input of the oscilloscope per Figure 6.
- (4) Connect the OUTPUT MONITOR of the Velonex 510 to the scope channel 1 input.
- (5) Monitor the voltage on the 1 volt/div. scale.

NOTE: The MONITOR OUTPUT of the Velonex 510 presents a 1000:1 attenuated output for scope monitoring.

- (6) With no output leads attached, configure the Velonex 510 as follows:

BURST MODE - Line freq.

OUTPUT TIMER MODE - Continuous (for voltage adjustment only)

OUTPUT AMPLITUDE - min.

SOURCE IMPEDANCE - 150  $\Omega$

Caution: The following steps will produce lethal voltages on the outputs of the Velonex 510.

- (7) With no load connected to the output, simultaneously depress both HV-ON buttons.
- (8) Adjust the AMPLITUDE of the Velonex 510 until 2.5-V peak (2.5-KV output) is displayed on the oscilloscope.
- (9) Verify that the waveshape displayed has the following characteristics. Record verification on the data sheet (Attachment 9):

Peak Amplitude - 2.5 KV peak

Frequency - 1.0 to 1.5 MHz

Fall Time -  $\geq 6 \mu$  sec to fall to 50% of peak.

- (10) Press either HV-ON push button to place the Velonex 510 in standby.
- (11) Reconfigure the Velonex 510 as follows:

OUTPUT TIMER MODE - TIMED OUTPUT

OUTPUT TIMER DURATION - 2 sec.

- (12) Reconfigure the scope as follows:

INPUT - Alternate (alt)

CHANNEL 1 - 1 Volt/Division

CHANNEL 2 - 2 Volt/Division

SWEEP -  $2 \mu$ s/Division

TRIGGER - External, Positive Level and Slope

- (13) Connect the isolator power supply to the test connector in accordance with Figure 1.

REVISION NO.

0

PROCEDURE NO. EIP-24

JOB CODE - S/N

PAGE 16 OF 33



- (14) Record the serial numbers of the cards on the data sheet.
- (15) Insert the card to be tested into the test connector.
- (16) Perform a functional test on the selected cards per the appropriate section of this procedure.
- (17) Connect the Velonex 510 output leads (Caution: verify the unit is in standby) to the test connector in accordance with Figure 6.
- (18) Connect Channel 2 of the oscilloscope to the test connector in accordance with Figure 6.
- (19) QC Representative verify all test connections and initial appropriate column on data sheet.

#### 8.5.2 Test Performance

- (20) Turn on the isolator power supply.
- (21) Visually monitor the oscilloscope. Channel 1 will display the applied surge waveform. Channel 2 will verify the application of the surge waveform to the channel being tested.
- (22) Depress both HV-ON push buttons of the Velonex 510 simultaneously.
- (23) Depress the START button of the Velonex 510.
- (24) Document the application of the SWC Transverse Mode voltage to the test specimen by initialing the appropriate column.
- (25) Press either of the HV-ON push buttons to place the Velonex 510 in standby.

REVISION NO.

0

PROCEDURE NO. FIP-24

JOB CODE - S/N

PAGE 17 OF 33

- (26) Connect the Velonex output leads and Channel 2 of the oscilloscope to the test connector in accordance with Figure 7.
- (27) Repeat steps (19) through (23).
- (28) Document the application of the SWC Common Mode voltage to the test specimen by initialing the appropriate column on the data sheet.
- (29) Press either of the HV-ON push buttons to place the Velonex 510 in standby.
- (30) Perform a functional test on the channel per the appropriate section of this procedure. Attach a completed copy of the functional test data sheet with pre- and post-SWC test data.
- (31) Repeat (17) through (30) for all channels on the card.

#### 8.6 Analog Isolator Thermal Drift

- (1) Record the serial number of the card on the data sheet (Attachment 10).
- (2) Calibrate the card according to the appropriate functional test of Section 8.2.
- (3) Set the Environmental Chamber temperature to ambient. Allow card to operate for a period of 20 minutes at the set temperature.
- (4) Take input and output data for high and low inputs.
- (5) Repeat steps (3) and (4) for temperatures 5°C, 10°C, 15°C, and 20°C below ambient.
- (6) Return the chamber to ambient and repeat step (3).

- (7) Repeat steps (3) through (5) for temperatures 5°C, 10°C, 15°C, and 20°C above ambient.

#### 8.7 Analog Isolator Linearity

- (1) Record the serial number of the card on the data sheet (Attachment 11).
- (2) Calibrate the card according to the appropriate functional test of Section 8.2.
- (3) Allow card to operate at ambient temperature for 20 minutes.
- (4) Take readings across the input span in increments of 25% of the span starting at the low end.

#### 8.8 Analog Isolator Power Supply Drift

- (1) Record the serial number of the card on the data sheet (Attachment 12).
- (2) Calibrate the card according to the appropriate functional test of Section 8.2.
- (3) Allow card to operate at ambient temperature for 20 minutes.
- (4) Adjust the  $\pm 15$ -V power supplies to  $\pm 15$  VDC  $\pm 0.001$  VDC.
- (5) Apply a 50% full scale input to the card using the system calibrator.
- (6) Record the outputs of each channel.
- (7) Adjust the +15-VDC power supply to  $+15.025 \pm 0.001$  VDC.

REVISION NO.

0

PROCEDURE NO. FIP-24

JOB CODE - S/N

PAGE 19 OF 33

- (8) Record the outputs of each channel.
- (9) Repeat steps (7) and (8) adjusting the + 15 VDC to + 15.050 VDC.
- (10) Repeat steps (7) and (8) using +14.975 VDC.
- (11) Repeat steps (7) and (8) using +14.950 VDC.
- (12) Return the +15-VDC supply to 15 VDC  $\pm$  .001.
- (13) Repeat steps (7) to (11) adjusting the -15-VDC supply to the negative values.

#### 8.9 Analog Isolator Interchannel Effects at Saturation

- (1) Record the serial number of the card on the data sheet (Attachment 13).
- (2) Calibrate the card according to the appropriate functional test of Section 8.2.
- (3) Apply a 50% of full scale input to all the channels. Record the outputs.
- (4) Continue to apply a 50% of full scale input to three channels and apply a 125% of full scale input to the fourth. Record the outputs of all channels.

#### 8.10 Analog Isolator Failure Mode Isolation

- (1) Record the serial number of the card on the data sheet (Attachment 14).
- (2) Connect a 4.7K  $\Omega$  resistor across each of the outputs.

- (3) Calibrate the card according to the appropriate functional test of Section 8.2.
- (4) Connect a 1K resistor and DMM across the input terminals.  $\pm 15$  volt power is applied for all tests.
- (5) Short across the 4.7K resistor.
- (6) Measure the DC voltage at the inputs and record on the data sheet.
- (7) Remove the resistor, measure the DC voltage at the inputs and record on the data sheet.
- (8) Connect 15 VDC across the output terminals with the polarity the same as the output. Measure the DC voltage on the inputs and record on the data sheet.
- (9) Connect 15 VDC across the output terminals with the polarity opposite the output. Measure the DC voltage on the input and record on the data sheet.
- (10) Connect 120 VAC through a 10K  $\Omega$ , 2-watt resistor to the output terminals. Measure the AC voltage on the inputs and record on the data sheet.

#### 8.11 Analog Isolator Bandwidth

- (1) Record the serial number of the card on the data sheet (Attachment 15).
- (2) Calibrate the card according to the appropriate functional test of Section 8.2.

- (3) Apply a square wave from the function generator with a magnitude of 100% of full scale input and a duration (T) calculated from the equation below to the inputs of the card.

$T = 10 RC$  where R and C are taken from EI DWG No. 00796.

Channel	R	C
1	$R_4 + 1/2 R_5$	$C_1$
2	$R_{13} + 1/2 R_{14}$	$C_4$
3	$R_{22} + 1/2 R_{23}$	$C_7$
4	$R_{31} + 1/2 R_{32}$	$C_{10}$

- (4) Record the value of RC for the channel on the data sheet.
- (5) Connect the oscilloscope and the waveform generator as shown on Figure 8.
- (6) Adjust the oscilloscope to display the output of the isolator exactly between the 0% and 100% graticle lines.
- (7) Adjust the sweep to display approximately 5 RC.
- (8) Enter on the data sheet the time taken for the output to rise from zero to the 63% line on the graticle.
- (9) Repeat steps (4) through (8) for all channels on the card.

#### 9.0 POSTTEST

- (1) Remove all test equipment and test leads and fixtures.
- (2) Return all isolator cards to controlled storage for proper storage.



- (3) Submit all data sheets and data acceptance sheets to the responsible engineer for review and acceptance or rejection of the tested cards.

## 10.0 ACCEPTANCE CRITERIA

### 10.1 Digital Isolator Functional Test

- (1) Output less than 1 volt for an input less than 6 volts (DC for -1 assembly, AC RMS for -2 assembly).
- (2) Output greater than or equal to 3.8 volts for input voltage greater than 45 volts.

### 10.2 Analog Isolator Functional Test

- (1) Outputs within 0.1% of output span for inputs at high and low limits of input span.

### 10.3 HI-Potential Isolation Tests (DC and AC)

- (1) Leakage current less than 1  $\mu$ ADC at 3 KVDC.
- (2) Leakage current less than 200  $\mu$ AAC rms at 1.5 KVAC.

### 10.4 Surge Withstand Capability Test

- (1) The channel fails if "zero" and/or "gain" adjustments cannot be made to bring amplifier output to within tolerances after SWC test.
- (2) The channel fails if after the SWC test the output fails to return to within 0.1% of the output span of the pre-SWC test value.

REVISION NO.

0

PROCEDURE NO. EIP-24

JOB CODE - S/N

PAGE 23 OF 33

#### 10.5 Thermal Drift

- (1) Output change of less than 0.015% of output span per °C for the range of 10°C to 40°C.

#### 10.6 Linearity

- (1) Output variance from tracking the input is less than 0.1% of the output span.

#### 10.7 Power Supply Drift

- (1) Output change less than 0.1% of the output span.

#### 10.8 Interchannel Effect at Saturation

- (1) Output change less than 0.05% of the output span.

#### 10.9 Failure Mode Isolation

- (1) Voltage at the input of less than 0.01% of input span.

#### 10.10 Bandwidth

- (1) Rise time measured (t) within 20% of calculated (RC).

#### 11.0 RETEST

- (1) Any card failing the acceptance criteria shall be returned to the card vendor for repair.
- (2) The repaired card shall be retested according to the appropriate section of this procedure and the retest data recorded on the appropriate data sheet.

12.0 FINAL REVIEW

All applicable steps of this procedure have been performed as written and all signatures and other verifications are complete.

Test Engineer Signature \_\_\_\_\_ Date \_\_\_\_\_

QC Representative Signature \_\_\_\_\_ Date \_\_\_\_\_

Qualification level of test engineer verified to level II or III per QAP 10-2.

Functional Manager Signature \_\_\_\_\_ Date \_\_\_\_\_

Test procedure approved for use.

Project Manager Signature \_\_\_\_\_ Date \_\_\_\_\_

REVISION NO.

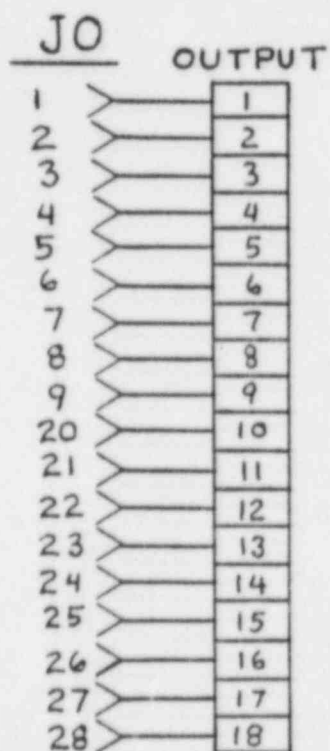
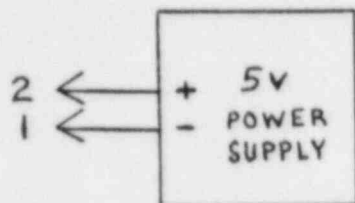
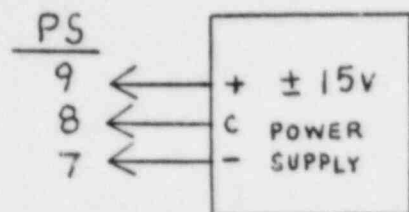
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PROCEDURE NO.

EIP-24

JOB CODE - S/N

PAGE 25 OF 33



#### AMP CONNECTOR PARTS NEEDED

PLUG	PART	AMP No.
PS	Plug Cable Clamp (5) Socket	206708-1 206966-1 205090-1 or 66602-1
JO	Plug Cable Clamp (18) Socket	205839-3 206070-1 205090-1 or 66602-1
JI	Plug Cable Clamp (32) Pin	206437-1 206512-1 205089-1

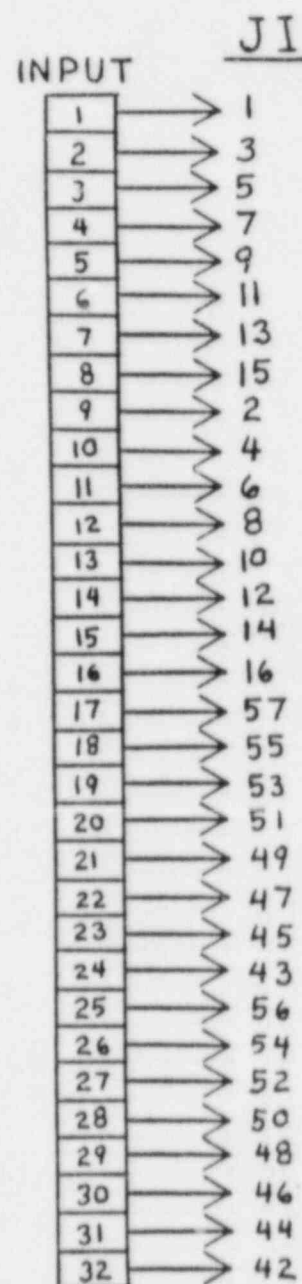
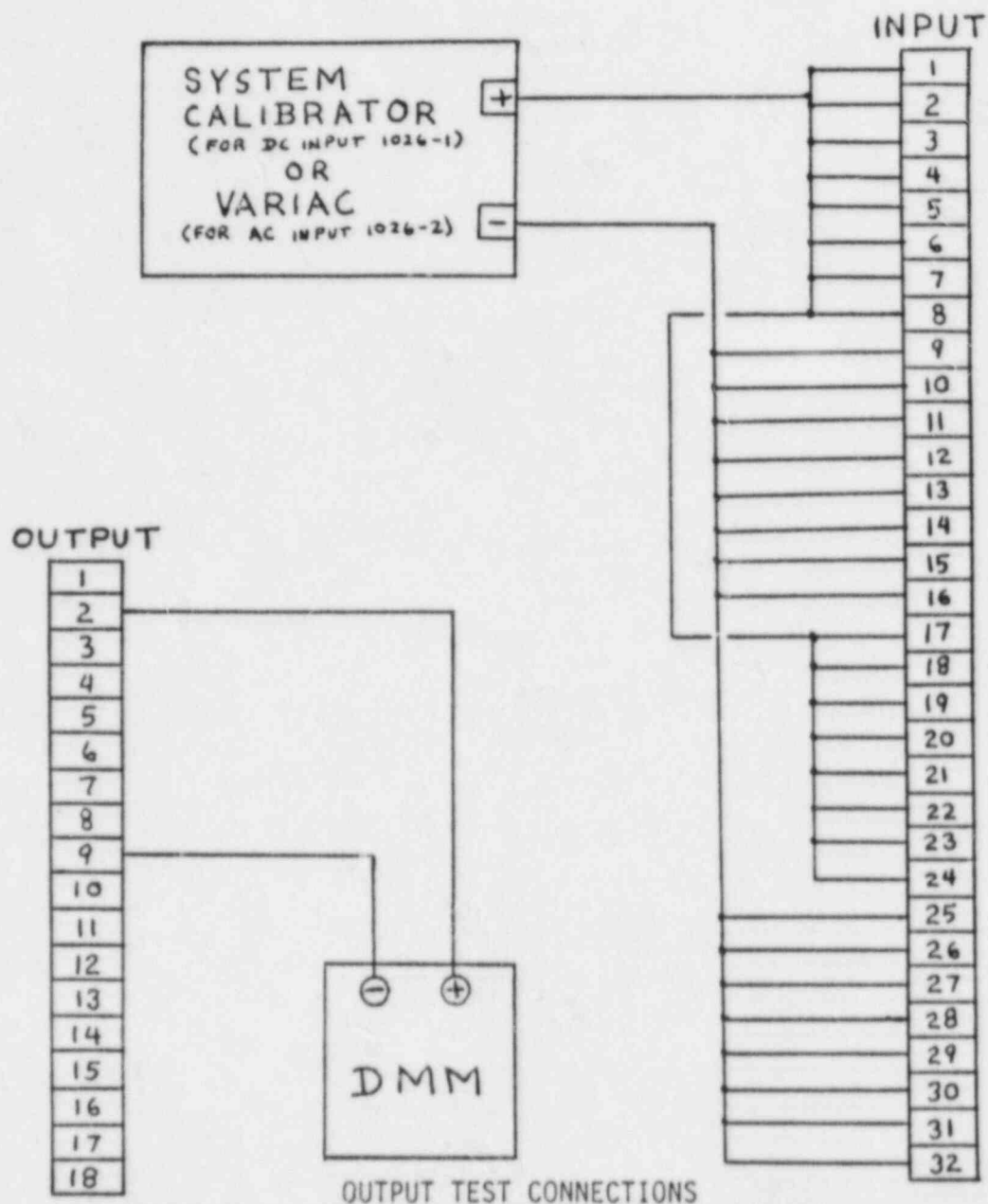


FIGURE 1  
Test Connector  
EIP-24



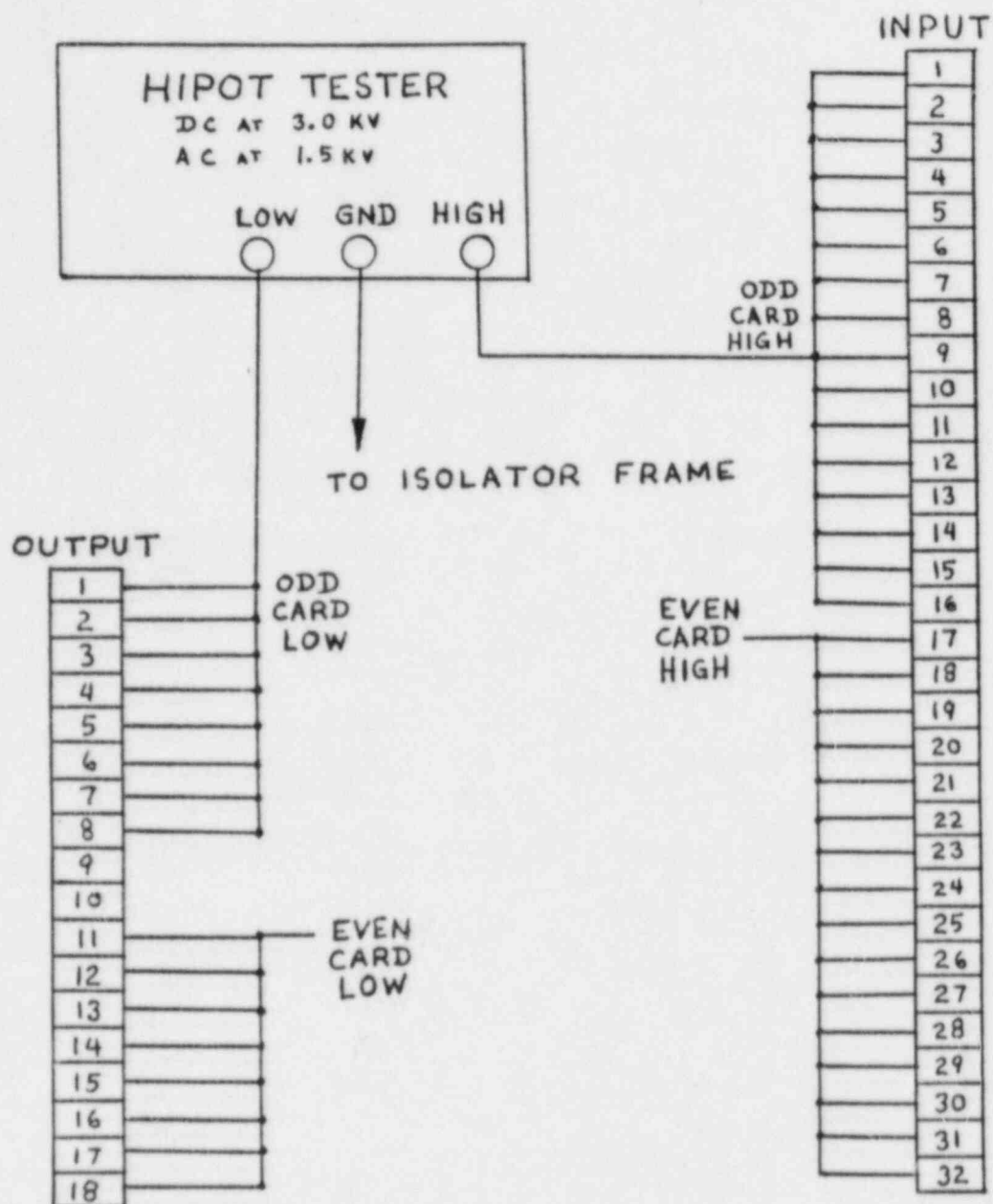
OUTPUT TEST CONNECTIONS

CHANNEL	ODD CARD	EVEN CARD
1	2	17
2	4	15
3	6	13
4	8	11
5	1	18
6	3	16
7	5	14
8	7	12
Com	9	10

FIGURE 2

Digital Isolator Functional Test Configuration

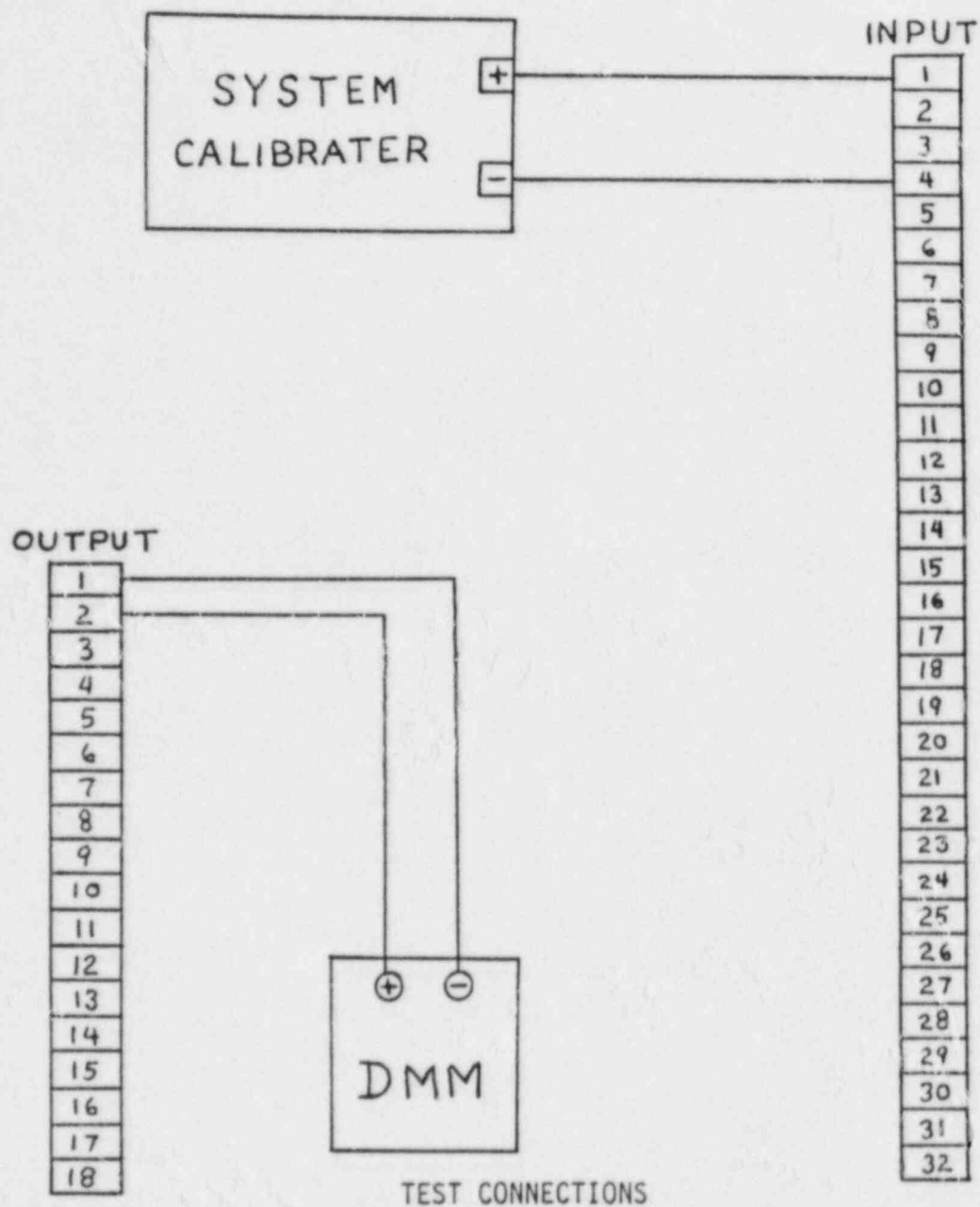
EIP-24



DC Test may be conducted on both cards simultaneously.  
 AC Test to be run on one card at a time.

FIGURE 3  
 Digital Isolator Isolation Test Configuration  
 EIP-24





TEST CONNECTIONS

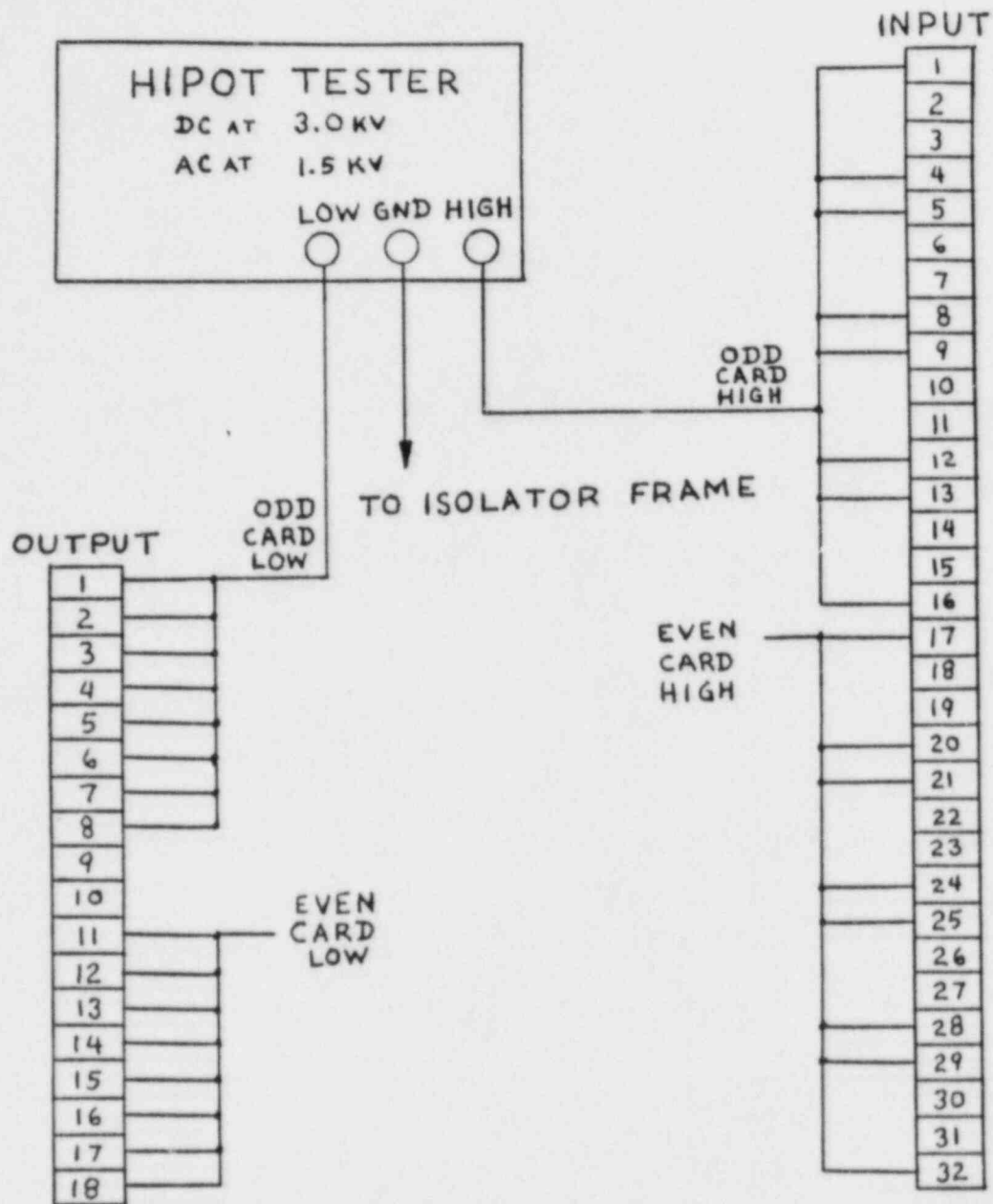
CHANNEL	ODD CARD				EVEN CARD			
	INPUT (+) (-)		OUTPUT (+) (-)		INPUT (+) (-)		OUTPUT (+) (-)	
1	13	16	8	7	29	32	11	12
2	5	8	6	5	21	24	13	14
3	9	12	4	3	25	28	15	16
4	1	4	2	1	17	20	17	18

\*Current loop inputs may be connected in series for simultaneous adjustment while voltage inputs may be connected in parallel.

FIGURE 4

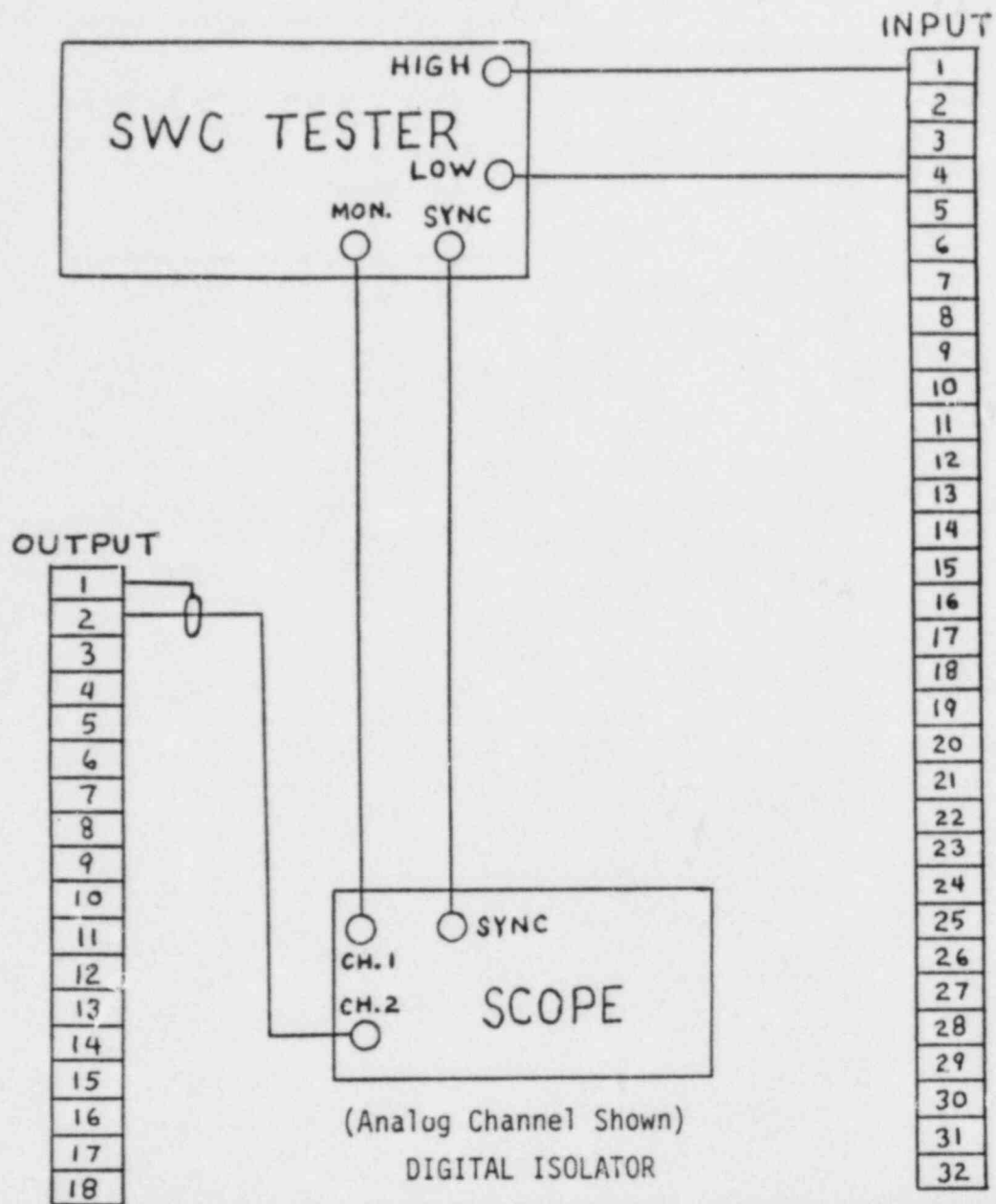
Analog Isolator Functional Test Configuration

EIP-24



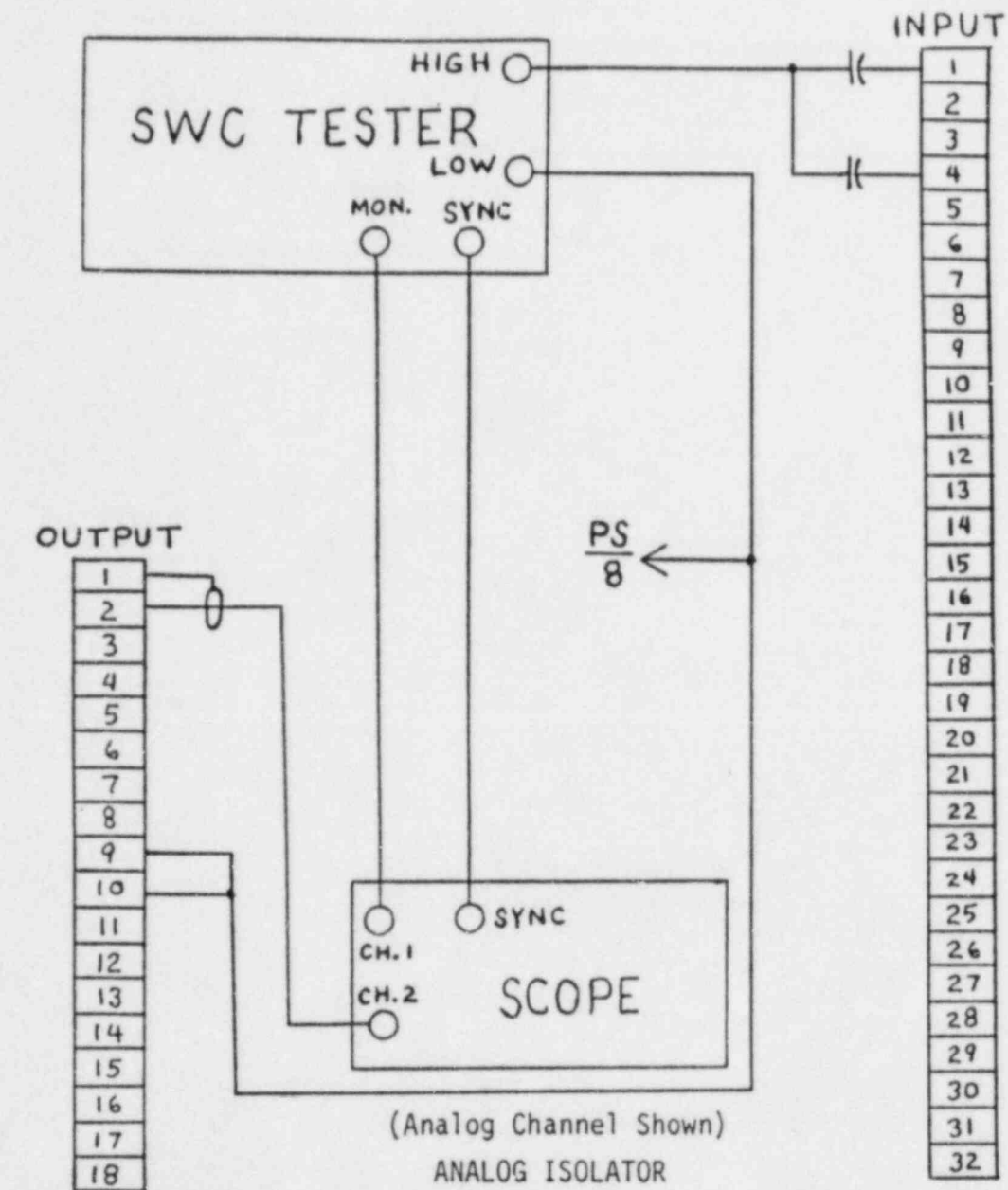
DC Test may be conducted on both cards simultaneously.  
 AC Test to be run on one card at a time.

FIGURE 5  
 Analog Isolator Isolation Test Configuration  
 EIP-24



Analog Isolator  
Inputs and Outputs  
listed on Figure 7.

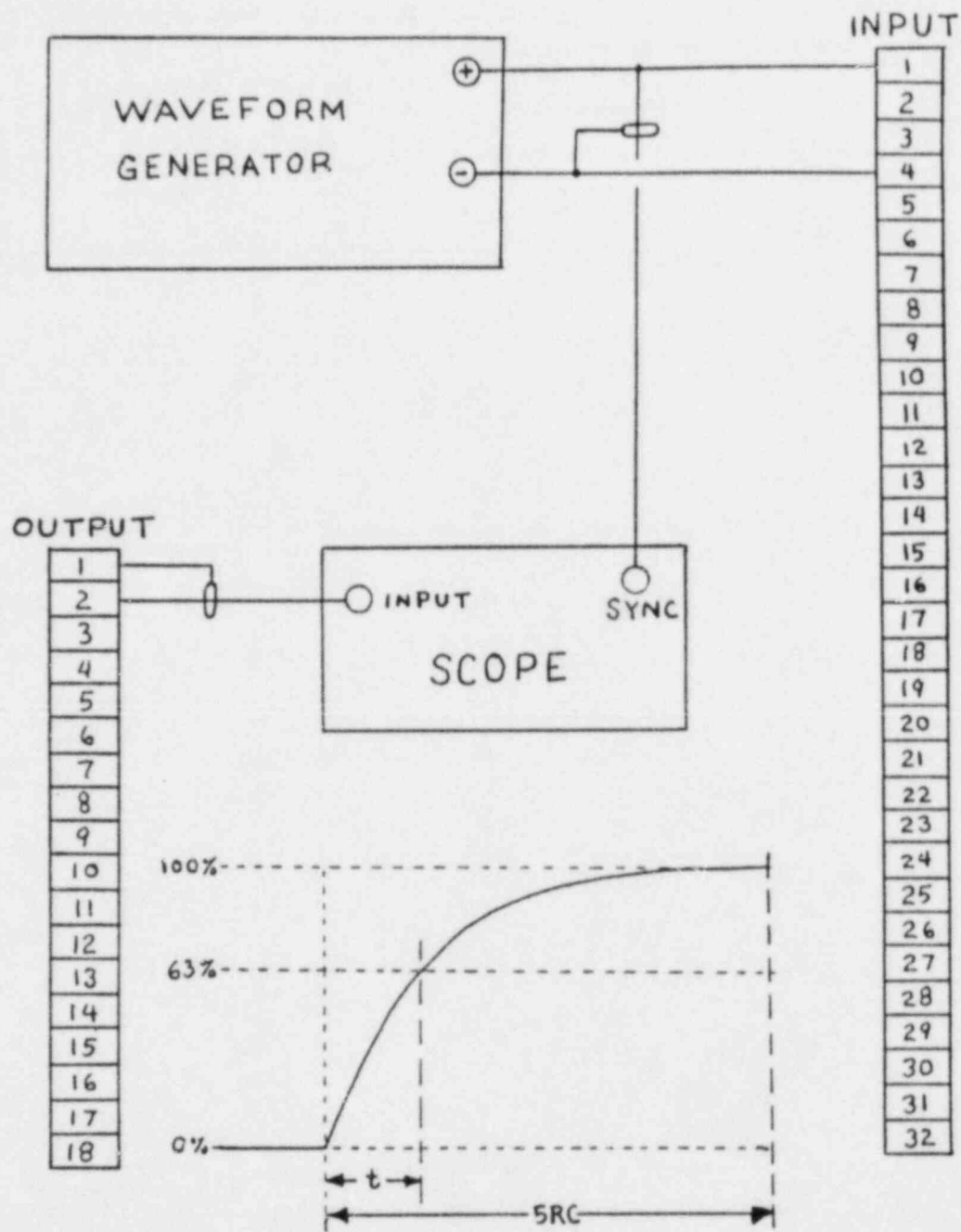
FIGURE 6  
Surge Withstand Capability Transverse Mode Test Configuration  
EIP-24



CHANNEL	ODD CARD				EVEN CARD			
	(+ ) IN (- )		(+ ) OUT (- )		(+ ) IN (- )		(+ ) OUT (- )	
1	13	16	8	7	29	32	11	12
2	5	8	6	5	21	24	13	14
3	9	12	4	3	25	28	15	16
4	1	4	2	1	17	20	17	18

Digital Isolator  
Inputs and  
Outputs listed  
on Figure 6.

FIGURE 7  
Surge Withstand Capability Common Mode Test Configuration  
EIP-24



See Figure 4 for Test Connections Table

FIGURE 8

Analog Isolator Bandwidth Test Configuration

TEST PROCEDURES TO BE USED

Test Section Number	Attachment Number	Quantity

Program Manager \_\_\_\_\_

Date \_\_\_\_\_

TEST EQUIPMENT USE LOG

Date \_\_\_\_\_  
Test Engineer \_\_\_\_\_  
QCR \_\_\_\_\_

Calibration

Item/Model	Serial No.	Date	Used For Tests



BURN-IN

Date \_\_\_\_\_  
Test Engineer \_\_\_\_\_  
QCR \_\_\_\_\_

±15-Volt DC Power Supply Used: MODEL \_\_\_\_\_

S/N \_\_\_\_\_

+5-Volt DC Power Supply Used: MODEL \_\_\_\_\_

S/N \_\_\_\_\_

Isolator Frame Used: MODEL \_\_\_\_\_

S/N \_\_\_\_\_

Isolation Amplifier Printed Circuit Boards Installed

Slot	Model	Serial Number
1	_____	_____
2	_____	_____
3	_____	_____
4	_____	_____
5	_____	_____
6	_____	_____
7	_____	_____
8	_____	_____
9	_____	_____
10	_____	_____
11	_____	_____
12	_____	_____
13	_____	_____
14	_____	_____
15	_____	_____
16	_____	_____
17	_____	_____
18	_____	_____
19	_____	_____
20	_____	_____
21	_____	_____
22	_____	_____
23	_____	_____
24	_____	_____

Burn-in time Specified \_\_\_\_\_

Actual \_\_\_\_\_

# FUNCTIONAL TEST

DATE: \_\_\_\_\_  
 TEST ENGINEER: \_\_\_\_\_  
 QCR \_\_\_\_\_

## DIGITAL ISOLATOR DATA SHEET 01026-X

Sht \_\_\_\_ of \_\_\_\_

Card Slot	Card S/N	Channel	Output	Input to Get		Output	
			0 V in	1 V out	3.8 V out	48 V in	QCR
Accepted Rejected		1					
		2					
		3					
		4					
		5					
		6					
		7					
		8					
Accepted Rejected		1					
		2					
		3					
		4					
		5					
		6					
		7					
		8					
Accepted Rejected		1					
		2					
		3					
		4					
		5					
		6					
		7					
		8					
Accepted Rejected		1					
		2					
		3					
		4					
		5					
		6					
		7					
		8					

# FUNCTIONAL TEST

DATE: \_\_\_\_\_  
 TEST ENGINEER: \_\_\_\_\_  
 QCR \_\_\_\_\_

## 00798 ANALOG ISOLATOR DATA SHEET

Assembly No. -1, -51, -60	Specifications		Sht ____ of ____
		Input      Output	
	Low      0 V      0 V		
	High 51 mVDC      51 mVDC		

Card Slot	Card S/N	Channel	Output Voltage		QCR
			Low	High	
Accepted Rejected		1			
		2			
		3			
		4			
Accepted Rejected		1			
		2			
		3			
		4			
Accepted Rejected		1			
		2			
		3			
		4			
Accepted Rejected		1			
		2			
		3			
		4			
Accepted Rejected		1			
		2			
		3			
		4			
Accepted Rejected		1			
		2			
		3			
		4			
Accepted Rejected		1			
		2			
		3			
		4			
Accepted Rejected		1			
		2			
		3			
		4			

# FUNCTIONAL TEST

DATE: \_\_\_\_\_  
 TEST ENGINEER: \_\_\_\_\_  
 QCR \_\_\_\_\_

## 00798 ANALOG ISOLATOR DATA SHEET

Assembly No. -2, -52	Specifications		Sht ____ of ____
		Input      Output	
	Low      0 V      0 V		
	High      1 VDC      51 mVDC		

Card Slot	Card S/N	Channel	Output Voltage		QCR
			Low	High	
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____

# FUNCTIONAL TEST

DATE: \_\_\_\_\_  
 TEST ENGINEER: \_\_\_\_\_  
 QCR \_\_\_\_\_

## 00798 ANALOG ISOLATOR DATA SHEET

<u>Assembly No.</u>	Specifications	
-3, -58	<div style="display: flex; justify-content: space-around;"> <div>           Input            Low 0 V            High 10 VDC         </div> <div>           Output            0 V            10 VDC         </div> </div>	Sht ____ of ____

Card Slot	Card S/N	Channel	Output Voltage		QCR
			Low	High	
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____

# FUNCTIONAL TEST

DATE: \_\_\_\_\_  
 TEST ENGINEER: \_\_\_\_\_  
 QCR \_\_\_\_\_

## 00798 ANALOG ISOLATOR DATA SHEET

Assembly No. -4, -56	Specifications		Sht ____ of ____
		Input      Output	
	Low    4 mADC      0 V		
	High 20 mADC      10 VDC		

Card Slot	Card S/N	Channel	Output Voltage		QCR
			Low	High	
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____

# FUNCTIONAL TEST

DATE: \_\_\_\_\_  
 TEST ENGINEER: \_\_\_\_\_  
 QCR \_\_\_\_\_

## 00798 ANALOG ISOLATOR DATA SHEET

Assembly No. -5	Specifications		Sht ____ of ____
		Input      Output	
	Low    0 mAAC      0 VAC		
	High 50 mAAC      1.3 VAC		

Card Slot	Card S/N	Channel	Output Voltage		QCR
			Low	High	
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____



# FUNCTIONAL TEST

DATE: \_\_\_\_\_  
 TEST ENGINEER: \_\_\_\_\_  
 QCR \_\_\_\_\_

## 00798 ANALOG ISOLATOR DATA SHEET

Assembly No. -6	Specifications		Sht ____ of ____
		Input      Output	
	Low      0 VAC      0 VAC		
	High 150 VAC      3.5 VAC		

Card Slot	Card S/N	Channel	Output Voltage		QCR
			Low	High	
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____

# FUNCTIONAL TEST

DATE: \_\_\_\_\_  
 TEST ENGINEER: \_\_\_\_\_  
 QCR \_\_\_\_\_

## 00798 ANALOG ISOLATOR DATA SHEET

Assembly No. <u>-7</u>	Specifications		Sht ____ of ____
		Input      Output	
	Low	0 VDC      0 VDC	
	High	150 VDC      10 VDC	

Card Slot	Card S/N	Channel	Output Voltage		QCR
			Low	High	
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____

# FUNCTIONAL TEST

DATE: \_\_\_\_\_  
 TEST ENGINEER: \_\_\_\_\_  
 QCR \_\_\_\_\_

## 00798 ANALOG ISOLATOR DATA SHEET

Assembly No. -8	Specifications				Sht ____ of ____
		Input		Output	
		0 V	0 V		
	Low High	10 V PULSE	10 V PULSE		

Card Slot	Card S/N	Channel	Output Voltage		QCR
			Low	High	
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____

# FUNCTIONAL TEST

DATE: \_\_\_\_\_  
 TEST ENGINEER: \_\_\_\_\_  
 QCR \_\_\_\_\_

## 00798 ANALOG ISOLATOR DATA SHEET

Assembly No. -9	Specifications		Sht ____ of ____
		Input      Output	
	Low    4 mADC      0 VDC		
	High 20 mADC      1 VDC		

Card Slot	Card S/N	Channel	Output Voltage		QCR
			Low	High	
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____

# FUNCTIONAL TEST

DATE: \_\_\_\_\_  
 TEST ENGINEER: \_\_\_\_\_  
 QCR \_\_\_\_\_

## 00798 ANALOG ISOLATOR DATA SHEET

<u>Assembly No.</u>	<u>Specifications</u>							
-10	<table border="0" style="width: 100%;"> <tr> <td style="width: 50%; text-align: center;"><u>Input</u></td> <td style="width: 50%; text-align: center;"><u>Output</u></td> </tr> <tr> <td>Low 0 V</td> <td>0 V</td> </tr> <tr> <td>High 51 mVDC</td> <td>1 VDC</td> </tr> </table>	<u>Input</u>	<u>Output</u>	Low 0 V	0 V	High 51 mVDC	1 VDC	Sht ____ of ____
<u>Input</u>	<u>Output</u>							
Low 0 V	0 V							
High 51 mVDC	1 VDC							

Card Slot	Card S/N	Channel	Output Voltage		QCR
			Low	High	
Accepted Rejected		1			
		2			
		3			
		4			
Accepted Rejected		1			
		2			
		3			
		4			
Accepted Rejected		1			
		2			
		3			
		4			
Accepted Rejected		1			
		2			
		3			
		4			
Accepted Rejected		1			
		2			
		3			
		4			
Accepted Rejected		1			
		2			
		3			
		4			
Accepted Rejected		1			
		2			
		3			
		4			

# FUNCTIONAL TEST

DATE: \_\_\_\_\_  
 TEST ENGINEER: \_\_\_\_\_  
 QCR \_\_\_\_\_

## 00798 ANALOG ISOLATOR DATA SHEET

Assembly No. -53	Specifications		Sht ____ of ____
		Input      Output	
	Low    0 V	0 V	
	High 100 mVDC	1 VDC	

Card Slot	Card S/N	Channel	Output Voltage		QCR
			Low	High	
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____
_____	_____	1	_____	_____	_____
_____	_____	2	_____	_____	_____
Accepted	_____	3	_____	_____	_____
Rejected	_____	4	_____	_____	_____

HI-POTENTIAL TEST (DC)

DATE: \_\_\_\_\_  
TEST ENGINEER: \_\_\_\_\_  
QCR \_\_\_\_\_

DIGITAL ISOLATOR DATA SHEET  
01026-1 or 01026-2

Sht \_\_\_\_ of \_\_\_\_

Card Slot	Card S/N	Channel	Leakage Current	
			3 KV	QCR
Accepted Rejected		1		
		2		
		3		
		4		
		5		
		6		
		7		
		8		
Accepted Rejected		1		
		2		
		3		
		4		
		5		
		6		
		7		
		8		
Accepted Rejected		1		
		2		
		3		
		4		
		5		
		6		
		7		
		8		
Accepted Rejected		1		
		2		
		3		
		4		
		5		
		6		
		7		
		8		



# HI-POTENTIAL TEST (DC)

PROCEDURE NO. \_\_\_\_\_  
 REV. \_\_\_\_\_  
 EI JOB NO. \_\_\_\_\_

DATE: \_\_\_\_\_  
 TEST ENGINEER: \_\_\_\_\_  
 QCR \_\_\_\_\_

## ANALOG ISOLATOR 00798-X DATA SHEET

Sht \_\_\_\_ of \_\_\_\_

Card Slot	Card S/N	Channel	Leakage Current	
			3 KV	QCR
_____	_____	1	_____	_____
_____	_____	2	_____	_____
Accepted	_____	3	_____	_____
Rejected	_____	4	_____	_____
_____	_____	1	_____	_____
_____	_____	2	_____	_____
Accepted	_____	3	_____	_____
Rejected	_____	4	_____	_____
_____	_____	1	_____	_____
_____	_____	2	_____	_____
Accepted	_____	3	_____	_____
Rejected	_____	4	_____	_____
_____	_____	1	_____	_____
_____	_____	2	_____	_____
Accepted	_____	3	_____	_____
Rejected	_____	4	_____	_____
_____	_____	1	_____	_____
_____	_____	2	_____	_____
Accepted	_____	3	_____	_____
Rejected	_____	4	_____	_____
_____	_____	1	_____	_____
_____	_____	2	_____	_____
Accepted	_____	3	_____	_____
Rejected	_____	4	_____	_____

# HI-POTENTIAL TEST (AC)

DATE: \_\_\_\_\_  
TEST ENGINEER: \_\_\_\_\_  
QCR \_\_\_\_\_

## DIGITAL ISOLATOR DATA SHEET 01026-1 or 01026-2

Sht \_\_\_\_ of \_\_\_\_

Card Slot	Card S/N	Channel	Leakage Current	
			1.5 KVAC	QCR
_____	_____	1	_____	_____
		2	_____	_____
		3	_____	_____
Accepted	_____	4	_____	_____
Rejected	_____	5	_____	_____
		6	_____	_____
		7	_____	_____
		8	_____	_____
_____	_____	1	_____	_____
		2	_____	_____
		3	_____	_____
Accepted	_____	4	_____	_____
Rejected	_____	5	_____	_____
		6	_____	_____
		7	_____	_____
		8	_____	_____
_____	_____	1	_____	_____
		2	_____	_____
		3	_____	_____
Accepted	_____	4	_____	_____
Rejected	_____	5	_____	_____
		6	_____	_____
		7	_____	_____
		8	_____	_____

# HI-POTENTIAL TEST (AC)

DATE: \_\_\_\_\_  
TEST ENGINEER: \_\_\_\_\_  
QCR \_\_\_\_\_

ANALOG ISOLATOR 00798-X DATA SHEET

Sht \_\_\_\_ of \_\_\_\_

Card Slot	Card S/N	Channel	Leakage Current	
			1.5 KVAC	QCR
_____	_____	1	_____	_____
Accepted	_____	2	_____	_____
Rejected	_____	3	_____	_____
	_____	4	_____	_____
_____	_____	1	_____	_____
Accepted	_____	2	_____	_____
Rejected	_____	3	_____	_____
	_____	4	_____	_____
_____	_____	1	_____	_____
Accepted	_____	2	_____	_____
Rejected	_____	3	_____	_____
	_____	4	_____	_____
_____	_____	1	_____	_____
Accepted	_____	2	_____	_____
Rejected	_____	3	_____	_____
	_____	4	_____	_____
_____	_____	1	_____	_____
Accepted	_____	2	_____	_____
Rejected	_____	3	_____	_____
	_____	4	_____	_____
_____	_____	1	_____	_____
Accepted	_____	2	_____	_____
Rejected	_____	3	_____	_____
	_____	4	_____	_____

SURGE WITHSTAND CAPABILITY TEST

CARD TYPE \_\_\_\_\_ DATE: \_\_\_\_\_  
TEST ENGINEER: \_\_\_\_\_  
QCR: \_\_\_\_\_  
WAVESHAPE VERIFICATION QCR \_\_\_\_\_ Sht \_\_\_\_ of \_\_\_\_

TRANSVERSE MODE S.W.C. TEST

<u>CARD S/N</u>	<u>CHANNEL</u>	<u>QCR CONNECTIONS OK</u>	<u>QCR TEST RUN</u>	<u>PRE-SWC TEST FUNCTIONAL OK</u>
_____	_____	_____	_____	_____
_____	_____	_____	_____	_____
_____	_____	_____	_____	_____
_____	_____	_____	_____	_____
_____	_____	_____	_____	_____
_____	_____	_____	_____	_____
_____	_____	_____	_____	_____

COMMON MODE S.W.C. TEST

<u>CARD S/N</u>	<u>CHANNEL</u>	<u>QCR CONNECTIONS OK</u>	<u>QCR TEST RUN</u>	<u>POST-SWC TEST FUNCTIONAL OK</u>
_____	_____	_____	_____	_____
_____	_____	_____	_____	_____
_____	_____	_____	_____	_____
_____	_____	_____	_____	_____
_____	_____	_____	_____	_____
_____	_____	_____	_____	_____
_____	_____	_____	_____	_____

THERMAL DRIFT

CARD TYPE \_\_\_\_\_  
CARD S/N \_\_\_\_\_

DATE: \_\_\_\_\_  
TEST ENGINEER: \_\_\_\_\_  
QCR: \_\_\_\_\_

Sht \_\_\_\_ of \_\_\_\_

Temp ( ) \_\_\_\_\_ °C (Ambient)

	<u>Input Low</u>	<u>Output</u>	<u>Input High</u>	<u>Output</u>	<u>QCR</u>
CH1	_____	_____	_____	_____	_____
CH2	_____	_____	_____	_____	_____
CH3	_____	_____	_____	_____	_____
CH4	_____	_____	_____	_____	_____

Temp ( ) \_\_\_\_\_ °C for a period of \_\_\_\_\_

CH1	_____	_____	_____	_____	_____
CH2	_____	_____	_____	_____	_____
CH3	_____	_____	_____	_____	_____
CH4	_____	_____	_____	_____	_____

Temp ( ) \_\_\_\_\_ °C for a period of \_\_\_\_\_

CH1	_____	_____	_____	_____	_____
CH2	_____	_____	_____	_____	_____
CH3	_____	_____	_____	_____	_____
CH4	_____	_____	_____	_____	_____

Temp ( ) \_\_\_\_\_ °C for a period of \_\_\_\_\_

CH1	_____	_____	_____	_____	_____
CH2	_____	_____	_____	_____	_____
CH3	_____	_____	_____	_____	_____
CH4	_____	_____	_____	_____	_____

Temp ( ) \_\_\_\_\_ °C for a period of \_\_\_\_\_

CH1	_____	_____	_____	_____	_____
CH2	_____	_____	_____	_____	_____
CH3	_____	_____	_____	_____	_____
CH4	_____	_____	_____	_____	_____

THERMAL DRIFT

CARD S/N \_\_\_\_\_

Sht \_\_\_\_ of \_\_\_\_

Temp ( ) \_\_\_\_\_ °C (Ambient)

	<u>Input Low</u>	<u>Output</u>	<u>Input High</u>	<u>Output</u>	<u>QCR</u>
CH1	_____	_____	_____	_____	_____
CH2	_____	_____	_____	_____	_____
CH3	_____	_____	_____	_____	_____
CH4	_____	_____	_____	_____	_____

Temp ( ) \_\_\_\_\_ °C for a period of \_\_\_\_\_

CH1	_____	_____	_____	_____	_____
CH2	_____	_____	_____	_____	_____
CH3	_____	_____	_____	_____	_____
CH4	_____	_____	_____	_____	_____

Temp ( ) \_\_\_\_\_ °C for a period of \_\_\_\_\_

CH1	_____	_____	_____	_____	_____
CH2	_____	_____	_____	_____	_____
CH3	_____	_____	_____	_____	_____
CH4	_____	_____	_____	_____	_____

Temp ( ) \_\_\_\_\_ °C for a period of \_\_\_\_\_

CH1	_____	_____	_____	_____	_____
CH2	_____	_____	_____	_____	_____
CH3	_____	_____	_____	_____	_____
CH4	_____	_____	_____	_____	_____

Temp ( ) \_\_\_\_\_ °C for a period of \_\_\_\_\_

CH1	_____	_____	_____	_____	_____
CH2	_____	_____	_____	_____	_____
CH3	_____	_____	_____	_____	_____
CH4	_____	_____	_____	_____	_____

THERMAL DRIFT

CARD S/N \_\_\_\_\_

Sht \_\_\_\_ of \_\_\_\_

Temp ( ) \_\_\_\_\_ °C (Ambient)

	<u>Input Low</u>	<u>Output</u>	<u>Input High</u>	<u>Output</u>	<u>QCR</u>
CH1	_____	_____	_____	_____	_____
CH2	_____	_____	_____	_____	_____
CH3	_____	_____	_____	_____	_____
CH4	_____	_____	_____	_____	_____



LINEARITY

DATE: \_\_\_\_\_  
TEST ENGINEER: \_\_\_\_\_  
QCR: \_\_\_\_\_

CARD TYPE \_\_\_\_\_

CARD S/N \_\_\_\_\_

Sht \_\_\_\_ of \_\_\_\_

Minimum Input \_\_\_\_\_

	<u>Input</u>	<u>Output</u>	<u>QCR</u>
CH1	_____	_____	_____
CH2	_____	_____	_____
CH3	_____	_____	_____
CH4	_____	_____	_____

25% of Maximum Input \_\_\_\_\_

	<u>Input</u>	<u>Output</u>	<u>QCR</u>
CH1	_____	_____	_____
CH2	_____	_____	_____
CH3	_____	_____	_____
CH4	_____	_____	_____

50% of Maximum Input \_\_\_\_\_

	<u>Input</u>	<u>Output</u>	<u>QCR</u>
CH1	_____	_____	_____
CH2	_____	_____	_____
CH3	_____	_____	_____
CH4	_____	_____	_____

75% of Maximum Input \_\_\_\_\_

	<u>Input</u>	<u>Output</u>	<u>QCR</u>
CH1	_____	_____	_____
CH2	_____	_____	_____
CH3	_____	_____	_____
CH4	_____	_____	_____

100% of Maximum Input \_\_\_\_\_

	<u>Input</u>	<u>Output</u>	<u>QCR</u>
CH1	_____	_____	_____
CH2	_____	_____	_____
CH3	_____	_____	_____
CH4	_____	_____	_____

POWER SUPPLY DRIFT

DATE: \_\_\_\_\_  
TEST ENGINEER: \_\_\_\_\_  
QCR: \_\_\_\_\_

CARD TYPE \_\_\_\_\_

CARD S/N \_\_\_\_\_

Sht \_\_\_\_ of \_\_\_\_

(Normal)  $\pm 15.0 \pm .001$  VDC

	<u>Input</u>	<u>Output</u>	<u>QCR</u>
CH1	_____	_____	_____
CH2	_____	_____	_____
CH3	_____	_____	_____
CH4	_____	_____	_____

+15.025 VDC

	<u>Input</u>	<u>Output</u>	<u>QCR</u>
CH1	_____	_____	_____
CH2	_____	_____	_____
CH3	_____	_____	_____
CH4	_____	_____	_____

+15.050 VDC

	<u>Input</u>	<u>Output</u>	<u>QCR</u>
CH1	_____	_____	_____
CH2	_____	_____	_____
CH3	_____	_____	_____
CH4	_____	_____	_____

+14.975 VDC

	<u>Input</u>	<u>Output</u>	<u>QCR</u>
CH1	_____	_____	_____
CH2	_____	_____	_____
CH3	_____	_____	_____
CH4	_____	_____	_____

+14.950 VDC

	<u>Input</u>	<u>Output</u>	<u>QCR</u>
CH1	_____	_____	_____
CH2	_____	_____	_____
CH3	_____	_____	_____
CH4	_____	_____	_____

POWER SUPPLY DRIFT

CARD S/N \_\_\_\_\_

Sht \_\_\_\_ of \_\_\_\_

-15.025 VDC

	<u>Input</u>	<u>Output</u>	<u>QCR</u>
CH1	_____	_____	_____
CH2	_____	_____	_____
CH3	_____	_____	_____
CH4	_____	_____	_____

-15.050 VDC

	<u>Input</u>	<u>Output</u>	<u>QCR</u>
CH1	_____	_____	_____
CH2	_____	_____	_____
CH3	_____	_____	_____
CH4	_____	_____	_____

-14.975 VDC

	<u>Input</u>	<u>Output</u>	<u>QCR</u>
CH1	_____	_____	_____
CH2	_____	_____	_____
CH3	_____	_____	_____
CH4	_____	_____	_____

-14.950 VDC

	<u>Input</u>	<u>Output</u>	<u>QCR</u>
CH1	_____	_____	_____
CH2	_____	_____	_____
CH3	_____	_____	_____
CH4	_____	_____	_____

INTERCHANNEL EFFECTS AT SATURATION

DATE: \_\_\_\_\_  
TEST ENGINEER: \_\_\_\_\_  
QCR: \_\_\_\_\_

CARD TYPE \_\_\_\_\_

CARD S/N \_\_\_\_\_

Sht \_\_\_\_ of \_\_\_\_

50% of Full Scale \_\_\_\_\_

	<u>Input</u>	<u>Output</u>	<u>QCR</u>
CH1	_____	_____	_____
CH2	_____	_____	_____
CH3	_____	_____	_____
CH4	_____	_____	_____

125% of Full Scale \_\_\_\_\_

	<u>Input</u>	<u>Output</u>	<u>QCR</u>
CH1	_____	_____	_____
CH2	_____	_____	_____
CH3	_____	_____	_____
CH4	_____	_____	_____

BANDWIDTH

DATE: \_\_\_\_\_

TEST ENGINEER: \_\_\_\_\_

QCR: \_\_\_\_\_

CARD TYPE \_\_\_\_\_

CARD S/N \_\_\_\_\_

Sht \_\_\_\_ of \_\_\_\_

	<u>RC</u>	<u>t</u>	<u>QCR</u>
CH1	_____	_____	_____
CH2	_____	_____	_____
CH3	_____	_____	_____
CH4	_____	_____	_____

BANDWIDTH

DATE: \_\_\_\_\_

TEST ENGINEER: \_\_\_\_\_

QCR: \_\_\_\_\_

CARD TYPE \_\_\_\_\_

CARD S/N \_\_\_\_\_

Sht \_\_\_\_ of \_\_\_\_

	<u>RC</u>	<u>t</u>	<u>QCR</u>
CH1	_____	_____	_____
CH2	_____	_____	_____
CH3	_____	_____	_____
CH4	_____	_____	_____