

## Enclosure 2

### Non-Proprietary Documents for RadICS Topical Report

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## RadICS Topical Report

*Revision 2*

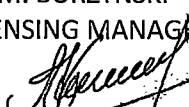
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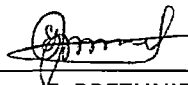
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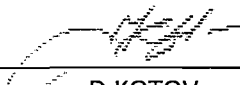
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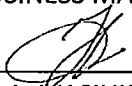
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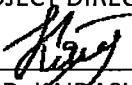
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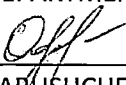
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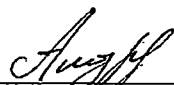
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## Abstract

The RadICS Topical Report presents design, performance, and qualification information for the RadICS digital safety instrumentation and control (I&C) platform developed by Research and Production Corporation (RPC) Radiy. The RadICS Platform is a generic digital safety I&C platform dedicated to the implementation of Class 1E safety I&C functions in U.S. nuclear power plants (NPPs). The RadICS Platform builds on the digital safety I&C systems developed by RPC Radiy since 1998.

The RadICS Topical Report is the summary licensing document for the RadICS Platform digital safety I&C platform and is organized as follows:

- Chapter 1, Introduction
- Chapter 2, RadICS Development and Operational History
- Chapter 3, Quality Assurance
- Chapter 4, RadICS Commercial Grade Dedication Plan
- Chapter 5, Regulations, Codes, and Standards
- Chapter 6, RadICS Platform
- Chapter 7, RadICS Platform Development Process
- Chapter 8, Electronic Design Development
- Chapter 9, Equipment Qualification and Analysis
- Chapter 10, Diversity and Defense-In-Depth
- Chapter 11, Secure Development and Operational Environment
- Chapter 12, Compliance Summary for Key Regulations, Codes, and Standards
- Appendix A, RadICS Platform Application Guide
- Appendix B, DI&C-ISG-04 Compliance Matrix
- Appendix C, RadICS Electronic Design Documents
- Appendix D, Evaluation of Diversity in an Application Using the RadICS Platform
- Appendix E, Request for Additional Information Cross Reference

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### Revision History

Revision information for the RadICS Topical Report is listed below. This table will contain a listing and description of changed paragraphs for each succeeding revision.

Revision	Date	Paragraph	Description of Change
0	September 19, 2016	All	Initial Release
1	June 30, 2019	As noted by revision bars	Reflect results of NRC review activities and responses to NRC requests for additional information. The results of the equipment qualification testing and commercial grade dedication assessments were incorporated.
2	April 14, 2020	As noted by revision bars	Reflects addition of three new input modules: Wide Range Analog Inputs Module, Resistance Temperature Detector Inputs Module, and Thermocouple Inputs Module



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# 1 Introduction

## 1.1 Background

The continued safe and economical operation of nuclear power plants (NPPs) requires the modernization of its control and safety systems to cope with obsolescence and age-related degradation. Changes and upgrades made in these systems also affect their digital instrumentation and control (I&C) systems, human-system interface (HSI) systems in the control rooms, and the full-scope simulators.

Nuclear utilities may choose to perform a large-scale modernization of their I&C systems in a single maintenance outage, or they may take several modernization steps spread over several outages. The design, manufacturing, and installation tasks to replace existing I&C systems are usually done by external companies and contractors with project supervision by the NPPs technical departments.

Research and Production Corporation (RPC) Radiy has a long history of working with operating NPPs and installing new I&C systems in turn-key projects. RPC Radiy provides a wide variety of I&C solutions ranging from full-scope turn-key modernization projects to reverse engineering and printed circuit board-level, like-for-like replacement as well as solutions to ageing and obsolescence problems, both for safety and non-safety applications. RPC Radiy uses Field Programmable Gate Array (FPGA) technology in its digital platform to implement customized solutions to NPPs I&C systems. RPC Radiy's proven technological expertise has been demonstrated in over 90 systems installed to-date.

RPC Radiy I&C systems have been installed in safety related systems of all operating NPP sites in the Ukraine and Bulgaria. The installed systems include Reactor Trip System (RTS), Reactor Power Control and Limitation System (RPCLS), Engineered Safety Features Actuation System (ESFAS), and Rod Control System, Switchgear and Electrical Distribution Systems, Nuclear Island Control System, and Turbine Island Control System. In addition, RPC Radiy is supporting Candu Energy Inc. in Canada and the Embalse NPP in Argentina in joint projects to improve and modernize safety systems. A detailed listing of RPC Radiy safety I&C installations is provided in Chapter 2.

RPC Radiy has successfully completed the final independent Functional Safety Assessment performed by **exida**. The certification company confirmed that the RPC Radiy processes and product complied with Safety Integrity Level (SIL) 3 requirements in single or multiple-channel configurations. The SIL 3 certification was performed using International Electrotechnical Commission (IEC) 61508:2010 (Parts 1 - 7) (Reference 1-1).<sup>1</sup>

In addition, RPC Radiy has been an ardent supporter of industry efforts to promote the use of reliable, diverse, and cost-effective FPGA-based I&C solutions for safety and control systems in NPPs. RPC Radiy has twice hosted the International Workshop on the Application of Field Programmable Gate Arrays in Nuclear Power Plants, in cooperation with the International Atomic Energy Agency (IAEA) and SunPort SA.

<sup>1</sup> The IEC 61508 Safety Integrity Level rating is different than the Software Integrity Level classification scheme described in IEEE Std 1012-2004.



## 1.2 Objectives of the Report

RPC Radiy established Radics LLC as a wholly owned Limited Liability Company (LLC) in July 2012. The Radics LLC business focus is the design and delivery of I&C systems for NPPs using the RadICS Platform equipment. Radics LLC is submitting this RadICS Topical Report to the Nuclear Regulatory Commission (NRC) for review and approval of the RadICS Platform design. The RadICS Platform is intended to be used as a digital control system platform solution for safety-related applications in NPPs. It is designed to replace existing analog and computer-based I&C systems currently used in U.S. NPP applications and to be installed as original equipment for new NPP facilities.

Radics LLC is seeking NRC generic approval for use of the RadICS Platform in nuclear safety I&C systems in any U.S. NPP. The RadICS Platform was originally designed, qualified, and manufactured to meet European nuclear safety and quality standards. In addition, RadICS Platform has been demonstrated to comply with the IEC 61508 SIL 3 certification requirements (Reference 1-2). Radics LLC is now managed under a quality assurance (QA) program that complies with 10 CFR Part 50 Appendix B (Reference 1-3). The purpose of the RadICS Topical Report is to demonstrate that the RadICS Platform and the associated quality and programmable logic life cycle process comply with NRC requirements. Compliance is demonstrated via the following licensing approach:

- Dedicate the generic RadICS Platform, which was not originally developed under a 10 CFR Part 50 Appendix B QA program, in accordance with the basic requirements for commercial dedication as defined in 10 CFR Part 21 (Reference 1-4). Radics LLC has employed the commercial dedication processes described in Electric Power Research Institute (EPRI) Topical Report (TR)- 106439 (Reference 1-5) and TR-107330 (Reference 1-6) and approved by the NRC (References 1-7 and 1-8).
- Qualify RadICS Platform hardware to meet U.S. standards. The RadICS Platform hardware has been qualified and maintained under the Radics LLC 10 CFR Part 50 Appendix B Quality Assurance Program Document (QAPD) (Reference 1-9). If new boards are developed or existing boards modified for obsolescence or other reasons, the new or modified hardware will be appropriately tested and/or analyzed to maintain equipment qualification to U.S. standards.
- Develop project-specific programmable logic in accordance with software life cycle plans that are compliant with NRC Branch Technical Position (BTP) 7-14 (Reference 1-10).
- The RadICS Platform toolset, which is provided as a design aid and not as a replacement for verification and validation (V&V), are not dedicated but continue to be subject to a configuration management (CM) program.

Radics LLC has concluded that the RadICS Platform can meet the needs of U.S. nuclear safety I&C applications in NPPs. Radics LLC will use the RadICS Platform defined in this Topical Report as a basis to provide project-specific systems to utilities and other users. Project-specific systems will be documented and submitted to the NRC by the appropriate licensees, using the appropriate processes, for review and approval for installation.

## 1.3 Scope of the Report

The RadICS Topical Report focuses on the following topics:

- RadICS Platform hardware design, qualification and analysis

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- RadICS Platform generic programmable logic and associated development life cycle processes (which includes application-oriented library of re-usable programmable logic components)
- RadICS Platform toolset used to design and implement the system architecture, configure the units and networks, and develop the project-specific programmable logic
- RadICS Platform project-specific development life cycle processes

The RadICS Topical Report also addresses the following interfaces with the RadICS Platform:

- Input connections to field devices but not the field devices
- Output connections to field devices but not the field devices
- Communication independence features of the RadICS Platform that support communication interfaces for export of data to a Monitoring and Tuning System (MATS) or a customer's plant computer system but not the MATS hardware or software or the plant computer system
- Communication independence and data transfer protocol features of the RadICS Platform that support communication with a customer's maintenance laptop computer to adjust setpoints and other predefined calibration factors but not the laptop computer
- Keyswitch interfaces for keyswitch inputs that support RadICS Platform access control features used to support system maintenance activities but not the keyswitch design or location
- Module connections and data protocols for loading electronic design configuration files but not the download station

The RadICS Platform is designed to be functionally and physically like currently installed I&C systems. Its platform capabilities include input processing, customizable logic solving, and output processing. The RadICS Platform continuously monitors system status through signals that are received from field sensors. It performs logic computations to create control commands. It also converts control commands to output signals that are applied to field actuators. The RadICS Platform has a modular and scalable design that can be configured to meet the needs of safety I&C applications in NPPs.

The RadICS Platform is a state-of-the-art digital control system platform specifically designed for safety-related control and protection systems in NPP applications. The RadICS Platform features a modular and distributed FPGA-based architecture. The RadICS Platform components are functionally like legacy analog measurement and trip modules; however, the RadICS Platform equipment takes advantage of the benefits of digital technology. The FPGA-based architecture supports effective implementation of key nuclear safety design principles: redundancy; independence; predictability and repeatability; and diversity and defense-in-depth (D3). The FPGA-based architecture allows simple programmable logic that avoids the unfavorable aspects of software-based systems

## ***1.4 Structure of the RadICS Topical Report***

The RadICS Topical Report has been divided into 12 chapters and 3 appendices:

Chapter 1 - Introduction: This chapter provides an overview of the RadICS Topical Report and identifies the supporting documents that were submitted for NRC review.

Chapter 2 - RadICS Development and Operational History: This chapter provides an overview of RadICS Platform development and operational use in international NPPs where it is currently deployed in a

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variety of digital safety I&C applications. This information is provided to illustrate the safety I&C developments that led to the RadICS Platform.

**Chapter 3 - Quality Assurance:** This chapter provides an overview of the quality program and the quality process employed to dedicate the generic RadICS Platform hardware and associated programmable logic used to develop systems for delivery to U.S. customers.

**Chapter 4 – RadICS Commercial Grade Dedication Plan:** This chapter provides an overview of the commercial grade dedication program used to dedicate the generic RadICS Platform hardware and associated platform programmable logic.

**Chapter 5 - Regulations, Codes, and Standards:** This chapter identifies the regulatory requirements, design criteria, and guidelines applicable to the RadICS Platform. Compliance with the key guidance documents is summarized in Chapter 12.

**Chapter 6 - RadICS Platform:** This chapter provides a description of the RadICS Platform operation and how it can be applied in NPP safety-related applications. This chapter also provides descriptions of the hardware and associated generic programmable logic that comprise the RadICS Platform. In addition, details are provided on how digital communications and testability are implemented in the RadICS Platform.

**Chapter 7 - RadICS Platform Development Process:** This chapter provides a description of the hardware development process, associated planning documents, and component testing process.

**Chapter 8 - Electronic Design Development:** This chapter provides a description of the RadICS Platform generic programmable logic development life cycle, planning documents, and the verification and validation process. The RadICS Platform programmable logic life cycle processes were examined in more detail as part of the SIL certification. This chapter also describes the separate programmable logic life cycle processes for the implementation of project-specific functionality.

**Chapter 9 - Equipment Qualification and Analysis:** This chapter provides an overview of the generic equipment qualification program for the RadICS Platform. The RadICS Platform qualification “envelope” is designed to meet or exceed the environmental qualification requirements for NPPs in the U.S. using the EPRI TR-107330 criteria. This chapter also provides a summary of the board-level reliability analysis results and an overview of the response time and setpoint analysis support information.

**Chapter 10 - Diversity and Defense in Depth:** This chapter provides an overview of the RadICS Platform approach to equipment and functional diversity to provide reasonable assurance that common cause failures (CCF) associated with FPGA technology are mitigated.

**Chapter 11 - Secure Development and Operational Environment:** This chapter provides a summary of a RadICS Platform vulnerability analysis and the secure development and operational environment controls provided by RPC Radiy.

**Chapter 12 - Compliance Summary for Key Regulations, Codes, and Standards:** This chapter provides a conformance summary of the RadICS Platform design and development processes for the key regulatory guidance documents.

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**Appendix A - RadICS Platform Application Guide:** This appendix provides the project-specific system design guidance for use of the RadICS Platform, including recommended practices and any restrictions.

**Appendix B - DI&C-ISG-04 Compliance Matrix:** This appendix provides a Digital I&C Interim Staff Guidance (DI&C-ISG)-04 (Reference 1-11) compliance matrix, with the requirement listed, RadICS Platform compliance to each criterion defined.

**Appendix C - RadICS Electronic Design Documents:** This appendix contains a listing of the RadICS Platform design documents associated with the Electronic Designs for the RadICS Modules and identifies the set of documents submitted to NRC to support the review of the RadICS Topical Report.

**Appendix D - Evaluation of Diversity in an Application Using the RadICS Platform:** This appendix contains an evaluation of the diversity in a typical application using the RadICS Platform technology based on the methodology outlined in NUREG/CR-7007 (Reference 1-12).

In this document, brackets (“[[ ]]”) denote proprietary information. In the proprietary document, the two brackets denoting the end of a proprietary segment of this report may appear one or more pages following the bracket indicating the start of the proprietary segment. In the nonproprietary edition of this document, the material within the brackets is removed.

## **1.5 Special Definitions**

RPC Radiy	RPC Radiy is a leading Ukrainian designer and supplier of advanced I&C systems for nuclear power plants. RPC Radiy is the designer and manufacturer of the RadICS Platform equipment. RPC Radiy is the parent company of Radics LLC. RPC Radiy is the company discussed in the context of the development and manufacture of the RadICS Platform, the RadICS Modules and associated generic Platform Electronic Design (EDs), and the RadICS Platform Functions Block Library.
Radics LLC	Radics LLC is a wholly owned LLC established in July 2012. The company's business focus is the design and delivery of I&C systems for NPPs using the RadICS Platform equipment. Radics LLC is the company discussed in the context of I&C system development using RadICS Platform equipment and the development of the Application ED using the Application Functions Block Library.
RPC Radiy Quality Management System	The RPC Radiy Quality Management System (QMS) governs the design and manufacture of the RadICS Platform equipment. The RPC Radiy QMS is based on International Organization for Standardization (ISO) 9001:2015 (Reference 1-13).



#### Radics LLC Quality Assurance Program

The Radics LLC Quality Assurance Program (QAP) governs the system design, integration, and delivery of I&C systems for NPPs using the RadICS Platform equipment. The Radics LLC QAP is based on 10 CFR Part 50 Appendix B and American Society of Mechanical Engineers (ASME) Nuclear Quality Assurance (NQA)-1-2008 (Reference 1-14) and the NQA-1a-2009 Addenda (Reference 1-15), as endorsed by Regulatory Guide (RG) 1.28 (Reference 1-16) and implemented through the Radics LLC QAPD.

#### RadICS Platform

RadICS Platform is used to describe the collective set of equipment that is used to develop I&C systems. The set of equipment includes the RadICS Chassis, the RadICS Modules, the generic Platform ED for the RadICS Modules, the RadICS Platform Functions Block Library, and the associated Radiy Product Configuration Toolset.

#### RadICS Chassis

Chassis is used to describe the frame and backplane supporting the RadICS Modules, the inter-module connections on the backplane, and the input/output (I/O) module external connections via rear connectors.

#### RadICS Module

RadICS Module (or just Module) is used to describe the seven types of hardware modules that perform logic processing, input/output functions, and network communications. Discussion of a RadICS Module includes the associated ED on the FPGA. The RadICS Module is the highest-level component within the RadICS Platform.

#### Unit

Unit is used to describe lower level components that are used to build Modules. Units are standardized to maximize the reuse of proven components and simplify the development of Modules. Units can consist of just hardware or ED or a combination of both.

#### Electronic Design

ED is used to describe the logic and functionality programmed on the FPGA or Complex Programmable Logic Device on a RadICS Module. There are two levels of logic in the RadICS Logic Module (i.e., Platform ED and Application ED) and only the Platform ED in the I/O Modules.

#### Platform ED

Platform ED is used to describe the Platform Logic that manages the basic operation of the RadICS Platform. It performs the management of I/O using a defined Work Cycle, interface communication with the Application ED, and the platform self-testing and communication error checking functions. Platform ED is used to refer to the ED as a configuration item and Platform Logic is used to describe what the Platform ED does.

#### Application ED

Application ED is used to incorporate the end user functional requirements for the I&C system functionality. The Application ED is used to execute the user defined functional requirements (e.g., reactor trip and engineered safety feature actuation functions). Application ED is used to refer to the ED as a configuration item and Application Logic is used to describe what the Application ED does.



Function Block Library	Function Block Library (FBL) is used to describe pre-developed functional blocks used in the implementation of RadICS Platform functions. Functional Blocks are written in Very High Speed Integrated Circuits Hardware Description Language (VHDL). The FBL consists of two parts: Platform FBL (PFBL) and Application FBL (AFBL).
Platform FBL	PFBL refers to the subset of functional blocks used for the development of the Platform ED for the RadICS Modules.
Application FBL	AFBL refers to the subset of functional blocks used for the development of the Application ED for the RadICS Logic Module.
Platform ED Development Life Cycle	Platform ED Development Life Cycle refers to the ED activities performed by RPC Radiy under their QMS to implement the Platform Logic on the RadICS Modules.
Application ED Development Life Cycle	Application ED Development Life Cycle refers to the ED activities performed by Radics LLC under their QAPD to implement the Application Logic on the RadICS Logic Modules in accordance with the end user functional requirements specification.
Form A	Form A means a normally open contact supporting a de-energize to trip function. The contact will open when energizing force is not present.

## 1.6 Acronyms and Abbreviations

Term	Definition
A	Ampère
A/D	Analog/Digital
AC	Alternating Current
AD	Architecture Description
ADC	Analog-to-Digital Conversion
AECL	Atomic Energy of Canada Limited
AFBL	Application Function Block Library
AFBL SD	Application Logic Functional Block Library Self-Diagnostics
AIM	Analog Inputs Module
AOM	Analog Outputs Module
ASME	American Society of Mechanical Engineers
ASPI	Advanced SCSI Programming Interface
BTP	Branch Technical Position
C	Celsius



Term	Definition
CCB	Change Control Board
CCF	Common Cause Failure
CDR	Critical Digital Review
CFR	Code of Federal Regulations
CGD	Commercial Grade Dedication
CM	Configuration Management
CMB	Configuration Management Board
CPLD	Complex Programmable Logic Device
CRAM	Configuration RAM
CRC	Cyclic Redundancy Check
CRR	Code Review Report
CSA	Canadian Standards Association
D/A	Digital/Analog
DAC	Digital-to-Analog Conversion
DAS	Data Acquisition System
dB	Decibel
dBuV	Signal Level
DC	Direct Current
DD	Detailed Description
DI&C-ISG	Digital Instrumentation and Controls Interim Staff Guidance
DIM	Discrete Inputs Module
DIU	Digital Input Unit
DLS	DownLoad Station
DOM	Discrete Outputs Module
DOU	Discrete Output Unit
DTP ID	Data Transfer Protocol Identification
DTP SD	Data Transmission Protocol Self-Diagnostics
D3	Diversity and Defense-In-Depth
ED	Electronic Design
ED SD	Electronic Design Self-Diagnostics



Term	Definition
EEPROM	Electrically Erasable Programmable Read-Only Memory
EPROM	Erasable Programmable Read-Only Memory
EFT	Electrical Fast Transient
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EPRI	Electric Power Research Institute
EQ	Equipment Qualification
ESD	Electrostatic Discharge
ESFAS	Engineered Safety Feature Actuation System
F	Fahrenheit
FBL	Function Block Library
FIT	Fault Insertion Test
FMEA	Failure Mode and Effects Analysis
FMEDA	Failure Modes and Effects Diagnostic Analysis
FOIP	Fiber Optic Inter-Chassis Interface
FOMP	Fiber Optic Monitoring Interface
FOTP	Fiber Optic Tuning Interface
FPGA	Field Programmable Gate Array
FSA	Functional Safety Audit
FSMP	Functional Safety Management Plan
FT	Functional Test
g	Acceleration Due to Gravity
GDC	General Design Criteria
GHz	Gigahertz
GQA	Global Quality Assurance, Inc.
HBC	Heartbeat Control
HDL	Hardware Description Language
HPD	HDL-Programmed Devices
HSI	Human-System Interface
HW	Hardware



Term	Definition
HW SD	Hardware Self-Diagnostics
HWM SD	Hardware Modules Self-Diagnostics
HWU SD	Hardware Unit Self-Diagnostics
Hz	Hertz
I&C	Instrumentation and Control
I/O	Input/Output
IAEA	International Atomic Energy Agency
ID	Identification
IDR	Input Data Receive
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronic Engineers
IERICS	Independent Engineering Review of I&C Systems in Nuclear Power Plants
IF SD	Interface and Data Transmission Self-Diagnostics
IOPM	Interface Protection Module
IP	Internet Protocol
IPC	Institute for Printed Circuits
ISA	Instrument Society of Automation
ISO	International Organization for Standardization
IT	Integration Test
JTAG	Joint Test Action Group
kA	Kiloampère
kHz	Kilohertz
kSPS	kilo samples per second
kV	Kilovolt
kΩ	Kiloohm
LAN	Local Area Network
LED	Light Emitting Diode
LLC	Limited Liability Company
LLS&TS	Logic Level Simulation and Timing Simulation
LM	Logic Module



Term	Definition
LSB	Least Significant Bit
LVDS	Low-Voltage Differential Signaling
m	Meter
ma	Milliampère
MATS	Monitoring and Tuning System
MC	Monotony Control
MED SD	Module ED Self-Diagnostics
MHz	Megahertz
MIL-STD	Military Standard
ms	Millisecond
mV	Millivolt
MΩ	Megaohm
NPP	Nuclear Power Plant
NQA	Nuclear Quality Assurance
NRC	Nuclear Regulatory Commission
OBE	Operating Basis Earthquake
OCM	Optical Communication Module
ODT	Output Data Transmission
PAD	Product Architecture Document
PC	Personal Computer
PCB	Printed Circuit Board
PCD	Product Concept Document
PD SD	Packet Data Self-Diagnostics
PLC	Programmable Logic Controllers
PS	Protection System
PSWD	Power Supply and Watchdog
QA	Quality Assurance
QAP	Quality Assurance Program
QAPD	Quality Assurance Program Document (i.e., Radics LLC QAPD-001)
QMS	Quality Management System



Term	Definition
QTS	Qualification Test Specimen
R&D	Research and Development
Rad	Radiation Absorbed Dose
RAD SD	Random-Access Data Self-Diagnostics
RAM	Random-Access Memory
RFI	Radio Frequency Interference
RG	Regulatory Guide
RIM	Resistance Temperature Detector Inputs Module
RMS	Root Mean Square
RPC	Research and Production Corporation
RPCLS	Reactor Power Control and Limitation System
RPCT	Radiy Product Configuration Toolset
RPP	Radiy Proprietary Protocol
RR	Review Report
RSCP	RS-232 Interface
RTD	Resistance Temperature Detector
RTL	Register Transfer Level
RTS	Reactor Trip System
RUP	Radiy UDP Based Protocol
RWSP	Radiy Watchdog Interface
SCA	Static Code Analysis
SD	Self-Diagnostics
SER	Safety Evaluation Report
SIL	Safety Integrity Level (from IEC 61508)
SIS	Safety Instrumented System
SOR	Safety Override
SQTS	Supplemental Qualification Test Specimen
SPI	Serial Peripheral Interface
SPIP	SPI Interface
SRP	Standard Review Plan





Term	Definition
SRS	Safety Requirements Specification
SSE	Safe Shutdown Earthquake
SSRAM	Synchronous Static Random-Access Memory
ST	Switch Time
STA	Static Timing Analysis
STC	Scientific and Technical Center
TDC	Thermocouple-to-Digital Converter
TIM	Thermocouple Inputs Module
TR	Topical Report
TSAP	Test Specimen Application Program
TÜV	Technischer Überwachungsverein (Technical Inspection Association)
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
UICP	UART Interface
UKTS	Unified Hardware System Equipment (UKTS in Russian)
U.S.	United States of America
V&V	Verification and Validation
V	Volts
VAC	Volts Alternating Current
VDC	Volts Direct Current
VHDL	<b>Very High Speed Integrated Circuits Hardware Description Language</b>
VM	Ventilation Module
VVER	Russian: Voda-Vodyanoi Energetichesky Reaktor (Pressurized Water Reactor)
WADC	Wide Range Analog-to-Digital Conversion Unit
WAIM	Wide Range Analog Inputs Module
ZPA	Zero Period Acceleration
$\Omega$	Ohm

## 1.7 Chapter 1 References

- 1 IEC 61508:2010, "Functional Safety of Electrical / Electronic / Programmable Electronic Safety-Related Systems"

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- 2 **exida** Report No. RAD 14-06-037 R002, "Results of the IEC 61508 Functional Safety Assessment for FPGA-Based Safety Controller RadICS," September 15, 2015
- 3 10 CFR Part 50 Appendix B, "Quality Assurances Requirements for Nuclear Power Plants and Fuel Reprocessing Plants"
- 4 10 CFR Part 21, "Reporting of Defects and Noncompliance"
- 5 EPRI TR-106439, "Guideline on Evaluation and Acceptance of Commercial Grade Digital Equipment for Nuclear Safety Applications", Electric Power Research Institute, October 1996
- 6 EPRI TR-107330, "Generic Requirements Specification for Qualifying a Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants," Electric Power Research Institute, December 1996
- 7 NRC Letter to EPRI dated July 17, 1997, "Review of EPRI Topical Report TR-106439, "Guideline on Evaluation and Acceptance of Commercial Grade Digital Equipment for Nuclear Safety Applications (TAC No. M94127)"
- 8 NRC Letter to EPRI dated July 30, 1998, "Safety Evaluation by the Office of Nuclear Reactor Regulation Electric Power Research Institute Topical Report, TR-107330, Final Report, Generic Requirements Specification for Qualifying a Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants."
- 9 QAPD-001, "Radics LLC Quality Assurance Program Description"
- 10 Branch Technical Position 7-14, Revision, 5, "Guidance on Software Reviews for Digital Computer Based Instrumentation and Control Systems," U.S. Nuclear Regulatory Commission, March 2007
- 11 DI&C-ISG-04, Revision 1, "Highly Integrated Control Rooms - Digital Communication Systems"
- 12 NUREG/CR-7007, "Diversity Strategies for Nuclear Power Plant Instrumentation and Control Systems."
- 13 ISO 9001:2015, "Quality management systems – Requirements"
- 14 ASME NQA-1-2008, "Quality Assurance Program Requirements for Nuclear Facilities"
- 15 ASME NQA-1a-2009, "Quality Assurance Program Requirements for Nuclear Facilities"
- 16 Regulatory Guide 1.28, Revision 4, "Quality Assurance Program Criteria (Design and Construction)"



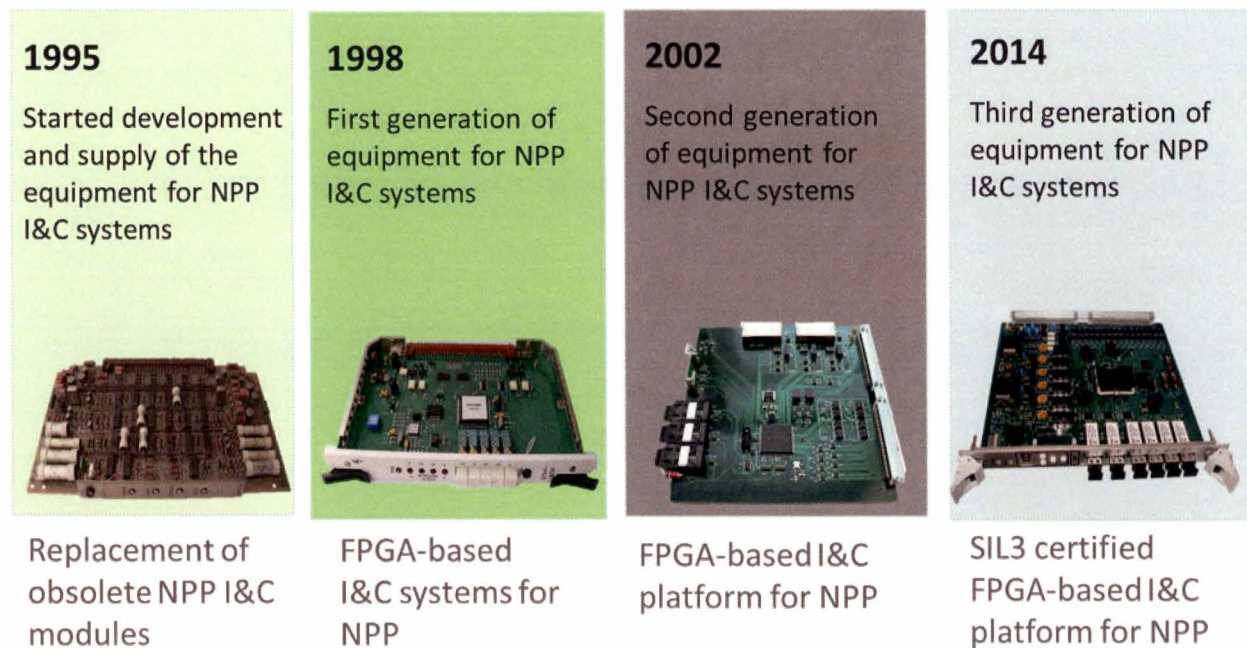
## 2 RadICS Development and Operational History

### 2.1 Evolution of RPC Radiy Products

The first generation of RPC Radiy products, called Unified Hardware System equipment (UKTS in Russian), was introduced in 1995. The main purpose of using UKTS was to replace obsolete NPP equipment that was no longer available in the market. Within the next six years, about 10,000 UKTS modules housed in approximately 700 UKTS cabinets, were manufactured and supplied and installed at to Ukrainian nuclear power plants.

In 1998 RPC Radiy developed a new generation of UKTS-DPI modules and cabinets with digital signal processing, noise-elimination and built-in diagnostics functions. FPGA technology was used for the first time in these modules to implement control logic. More than 50,000 of such modules were installed in NPPs in subsequent years.

The evolution of RPC Radiy products is shown in Figure 2-1.



**Figure 2-1: Evolution of RPC Radiy Products**

The development of a new concept of an FPGA-based I&C platform was initiated in 2002 concurrent with the manufacturing and installation of the UKTS-DPI modules. This new platform, called RADIY Platform, eventually replaced the UKTS-DPI platform, whose main disadvantage was that it was designed for single-purpose applications.





The RADIY Platform is of a modular type and it includes modules such as logic modules, diagnostic modules, and digital and analog I/O modules. RPC Radiy has installed over 70 RADIY Platform-based safety and control systems in operating NPPs. Examples applications include RTS, RPCLS, and ESFAS.

The RPC Radiy latest development is the FPGA-based RadICS Platform. This is a new generation product, designed in 2011 based on an earlier RADIY platform. The RadICS Platform consists of an IEC 61508:2010 (Reference 2-1) SIL 3 chassis level certifiable architecture with a typical response time of less than 10 milliseconds and a comprehensive set of constituent modules.

The Functional Safety Assessments performed by *exida* (Reference 2-2) demonstrated that the RadICS Platform complies with the IEC 61508 SIL 3 certification requirements.

## 2.2 Overview of RadICS Platform

The RadICS Platform (see Figure 2-2) consists mostly of a set of general-purpose building blocks that can be configured and used to implement project-specific functions and systems. The RadICS Platform is composed of various standardized modules, each based on the use of FPGA chips as computational engines.

The basic architecture of the RadICS Platform consists of an instrument chassis containing a logic module, as well as up to 14 other I/O and fiber-optic communication modules. Logic modules gather input data from input modules, execute user-specific logic, and update the value driving the output modules. They are also responsible for gathering diagnostic and general health information from all I/O modules. The I/O modules provide interfaces with field devices (e.g., sensors, transmitters, and actuators). The functionality of each module is defined by the logic implemented in the FPGA(s) that are part of the above modules.

In addition to the above described general purpose I/O modules, there is a fiber-optic communication module that can be used to expand the I&C system to multiple chassis. It is also possible to provide inter-channel communications via fiber-optic based connections between logic modules.

The backplane of the RadICS Platform provides interfaces to power supplies, process I/Os from the field, communication links, key switch inputs, and indicators. The internal backplane provides interfaces to the various modules installed within each chassis by means of a dedicated, isolated, point-to-point low-voltage differential signaling (LVDS) interface.

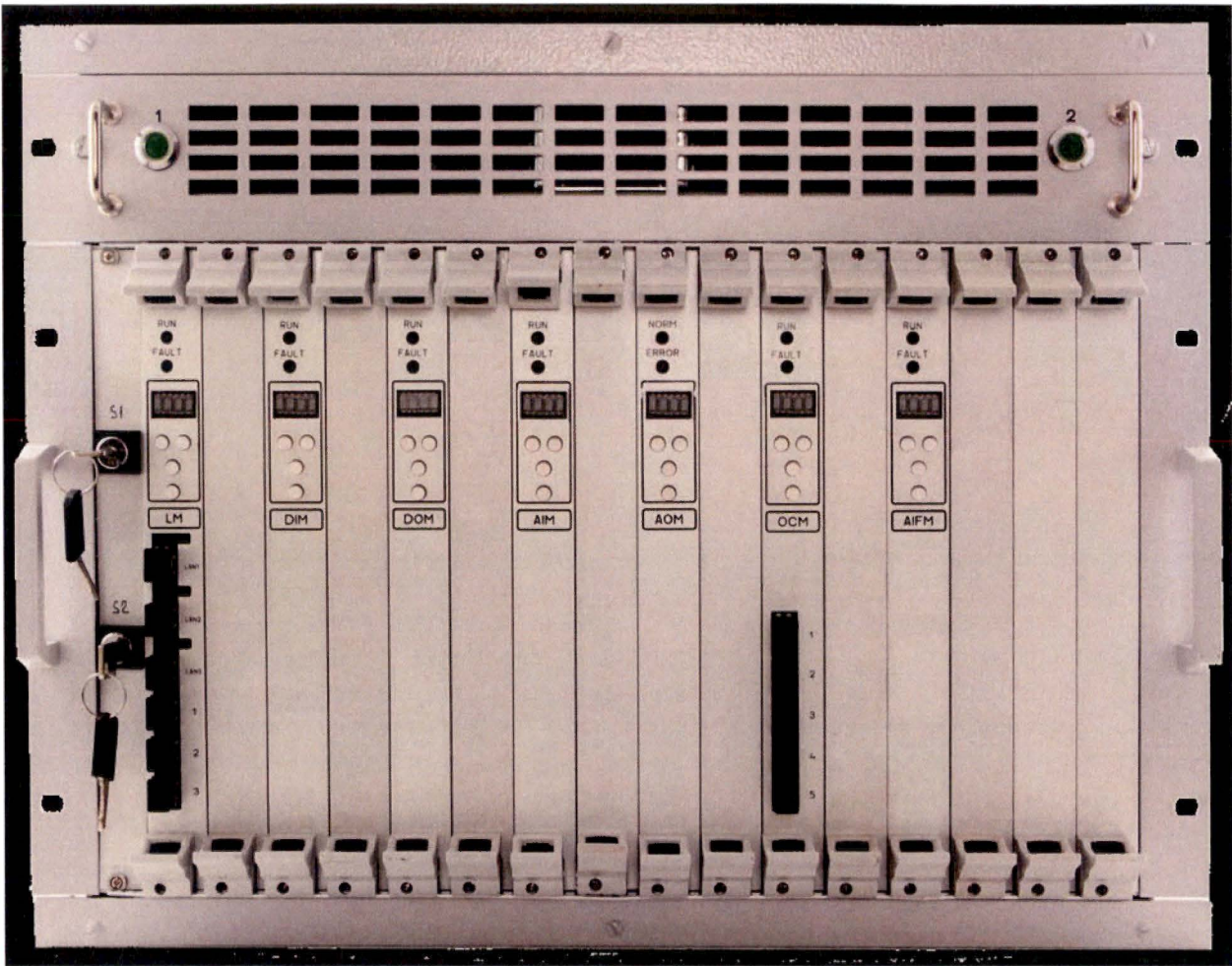


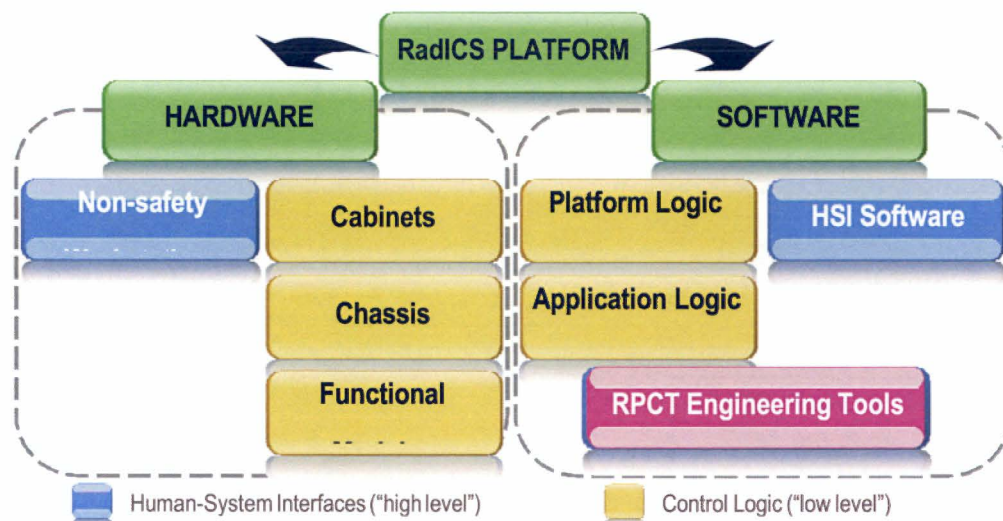
Figure 2-2: RadICS Platform

For application development, RPC Radiy provides a tool called Radiy Product Configuration Toolset (RPCT). This tool can be used to configure logic for various applications using the AFBL.

In addition, the RadICS Platform includes extensive on-line self-surveillance and diagnostics at various levels, including control of FPGA power, watchdog heartbeat monitoring, cyclical redundancy check (CRC) calculations, and monitoring of the performance of FPGA support circuits, I/O modules, communications units, and power supplies.

The RadICS Platform can also be represented as a hierarchy with several levels, which could be arranged into two main groups: software (i.e., VHDL to configure the FPGA) and hardware blocks. The RadICS Platform high-level representation is shown in Figure 2-3. The non-safety workstations and the HSI software associated with the MATS are not within the scope of the RadICS Platform Topical Report.





**Figure 2-3: RadICS Platform High Level Representation**

The diagnostic functions are separated from the logic functions and both are executed concurrently. In case of fault detection, the system is placed in a safe state as predefined for each application during configuration.

## **2.3 RadICS-Based Applications**

FPGA based platforms produced by RPC Radiy are used in the most critical and high-reliability demanding NPP applications such as RTS, ESFAS, and Rod Control System. The following sub-sections provide a description of these systems to provide examples of how the RadICS Platform can be used for specific projects; however, no NRC approval is sought for any specific system architecture or design as part of the RadICS Topical Report review.

### **2.3.1 Reactor Trip System**

RPC Radiy has developed RTSs that have been used to continuously monitor various process variables and generates reactor shutdown signals in case these variables reach their setpoints. These systems have been designed to transmit all the information necessary for surveillance and monitoring of the plant (e.g., the status of command execution, plant conditions, and diagnostic data) to the control room, and on customer's request, to other safety and non-safety systems. An example four channel RTS configuration is shown in Figure 2-4.

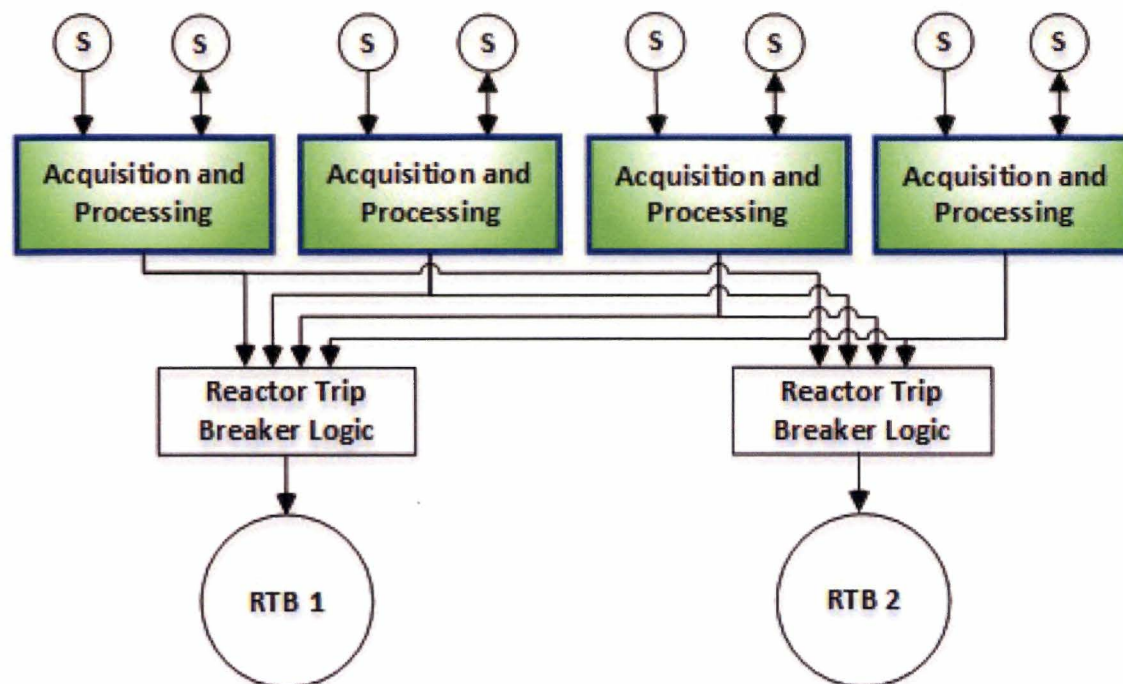


Figure 2-4: Example Reactor Trip System Configuration

Systems designed with RadICS Platform technology can be designed to correct voting logic when faults are detected, so that system availability is optimized without compromising safety. The RadICS self-diagnostic subsystem includes troubleshooting assistance functions that can be used to support maintenance work for easy localization of faults. In case of failure detection (i.e., failure in a RadICS Module), a system designed with RadICS Platform technology can put itself in the safe state by generating a reactor shutdown signal and the corresponding annunciation signals. RadICS Platform technology has been used to design systems that included manual actuation of shutdown logic from the Main Control Room or Remote Shutdown Station. The RadICS Platform can be adapted to perform equivalent functions in all the major reactor types. A typical set of RadICS Platform equipment is shown in Figure 2-5.



*To date there are 30 RPC Radiy designed RTSS in operation at Zaporizhzhе NPP, Rivne NPP, Khmelnytsky NPP, and South Ukraine NPP.*

**Figure 2-5: Typical RadICS Reactor Trip System Equipment**

### **2.3.2 Engineered Safety Features Actuation System**

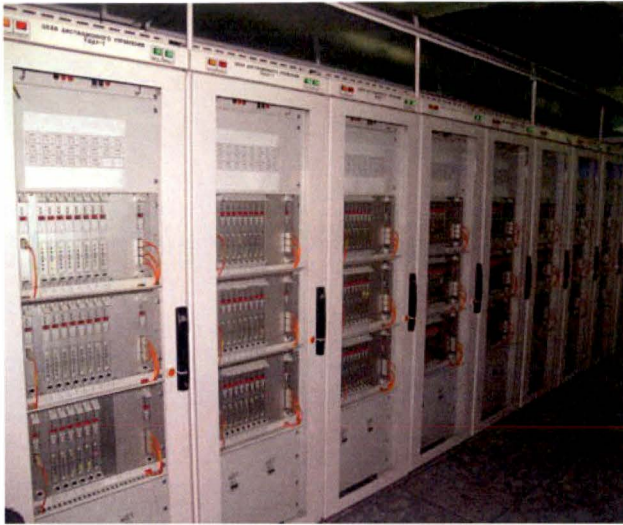
The RadICS Platform technology can be used to design and manufacture ESFAS applications (see Figure 2-6) that have the following main functions:

- Protection, interlocking, and monitoring of actuators
- Manual remote control of actuators
- Acquisition of signal data and other related information
- Signal conditioning and monitoring of safety signals, detectors, and sensor
- Full-scope system self-diagnostics

The following design principles can be applied in the ESFAS using RadICS Platform technology:

- Variety of input signals (e.g., current, voltage, resistance, “dry contact”)
- System expandability to accommodate the need for an increased number of inputs and outputs
- A simple and controlled process for the modification of system logic and control algorithms
- Interfacing capability with other plant control and monitoring systems





*Twenty Four ESFASs are presently in operation at Rivne, South Ukraine, and Kozloduy (Bulgaria) NPPs.*

**Figure 2-6: RadICS Engineered Safety Features Actuation System Cabinets**

A RadICS Platform-based ESFAS can be supplied in two, three, or four channels configurations. In these configurations, a RadICS Platform-based system can meet U.S. Class 1E requirements. An example of a four-channel ESFAS configuration is shown in Figure 2-7.

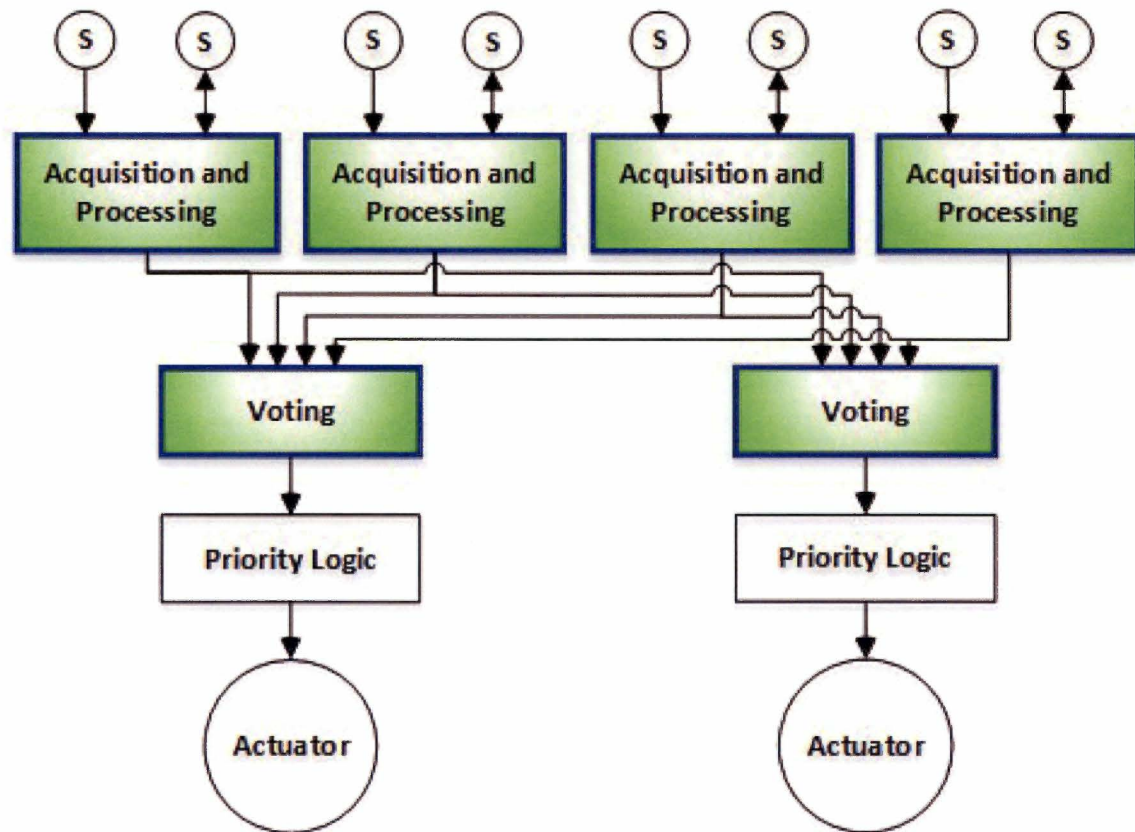


Figure 2-7: Example Engineered Safety Features Actuation System Configuration

## 2.4 RPC Radiy Safety I&C Installations

RPC Radiy FPGA-based I&C systems have been installed in operating NPPs since 1998. A summary of RPC Radiy nuclear I&C references collectively implemented with all technologies is provided in Table 2-1.

**Table 2-1: RPC Radiy Designed and Manufactured Equipment and Systems Installed in NPPs**

<b>Systems Supplied</b>	<b>Nuclear Power Plant</b>	<b>Number of Installed Systems</b>	<b>Installation Years</b>
Reactor Trip System	Zaporozhye NPP, South-Ukraine NPP, Rivne NPP, and Khmelnytskyi NPP	30	2004-2015
Reactor Power Control and Limitation System	Zaporozhye NPP, South-Ukraine NPP, Rivne NPP, and Khmelnytskyi NPP	14	2004-2019
Engineered Safety Feature Actuation System	South-Ukraine NPP, Rivne NPP, and Kozloduy NPP (Bulgaria)	24	2005-2020
Rod Control System	South-Ukraine NPP	1	2013
Fire Alarm System	Zaporozhye NPP, South-Ukraine NPP, and Rivne NPP	17	2008-2019
Reactor Trip Breakers	South-Ukraine NPP and Kozloduy NPP (Bulgaria)	9	2007-2015
UKTS-Based Reactor and Turbine Control System	Rivne NPP and Zaporozhye NPP	15	1998-2004
Switchgear Cabinets	Khmelnytskyi NPP, Zaporozhye NPP, Rivne NPP, Nuclear Research Institute, Kozloduy NPP, and South-Ukraine NPP	3,282	2006-2019
Seismic Sensors	Khmelnytskyi NPP, Zaporozhye NPP, Rivne NPP, and South-Ukraine NPP	83	2010-2019
Pressure Heat Transportation Pump Motor Speed Measuring Devices	Embalse NPP (Argentina)	12	Delivered to Candu Energy, April 2014
Main Control Room and Secondary Control Area Window Annunciators	Embalse NPP (Argentina)	1	Delivered to Candu Energy, April 2014



Radics LLC has a problem reporting and tracking system as described in the Radics LLC Quality Assurance Manual (Reference 2-3). The RPC Radiy nuclear operating experience has provided ample opportunities to identify latent errors and to validate equipment performance.

In addition, operating experience with RPC Radiy digital safety I&C systems has shown no instances where the capability of the safety I&C system to perform its intended safety function(s) was compromised during an anticipated operational occurrence. Specifically, the RPC Radiy systems have not experienced any system failures or common cause failures in more than 692 reactor-years of operation as of January 2020.

## **2.5 Chapter 2 References**

- 1 IEC 61508-2010, "Functional Safety of Electrical/Electronic/Programmable Electronic Safety-related Systems," International Electrotechnical Commission
- 2 "*exida* Report No. RAD 14-06-037 R002, "Results of the IEC 61508 Functional Safety Assessment for FPGA-Based Safety Controller RadICS," September 15, 2015
- 3 QAPD-001, "Radics LLC Quality Assurance Program Description"





### 3 Quality Assurance

#### 3.1 Introduction

RPC Radiy is a leading Ukrainian designer and supplier of advanced I&C systems for NPPs. RPC Radiy offers a full development cycle including design, manufacturing, testing, and equipment installation. RPC Radiy is the designer and manufacturer of the RadICS Platform equipment.

The RPC Radiy QMS governs the design and manufacture of the RadICS Platform equipment. The RPC Radiy QMS is based on ISO 9001:2015 (Reference 3-1). The RPC Radiy QMS is described in Section 3.2.

Radics LLC is a wholly owned LLC established in July 2012. The company's business focus is the design and delivery of I&C systems for NPPs using the RadICS Platform equipment.

The Radics LLC QAP governs the system design, integration, and delivery of I&C systems for NPPs using the RadICS Platform equipment. Radics LLC QAP is based on 10 CFR Part 50 Appendix B (Reference 3-2) and ASME NQA-1-2008 (Reference 3-3) and the NQA-1a-2009 Addenda (Reference 3-4), as endorsed by RG 1.28 (Reference 3-5). The Radics LLC QAP is described in Section 3.3.

#### 3.2 RPC Radiy Quality Assurance Program

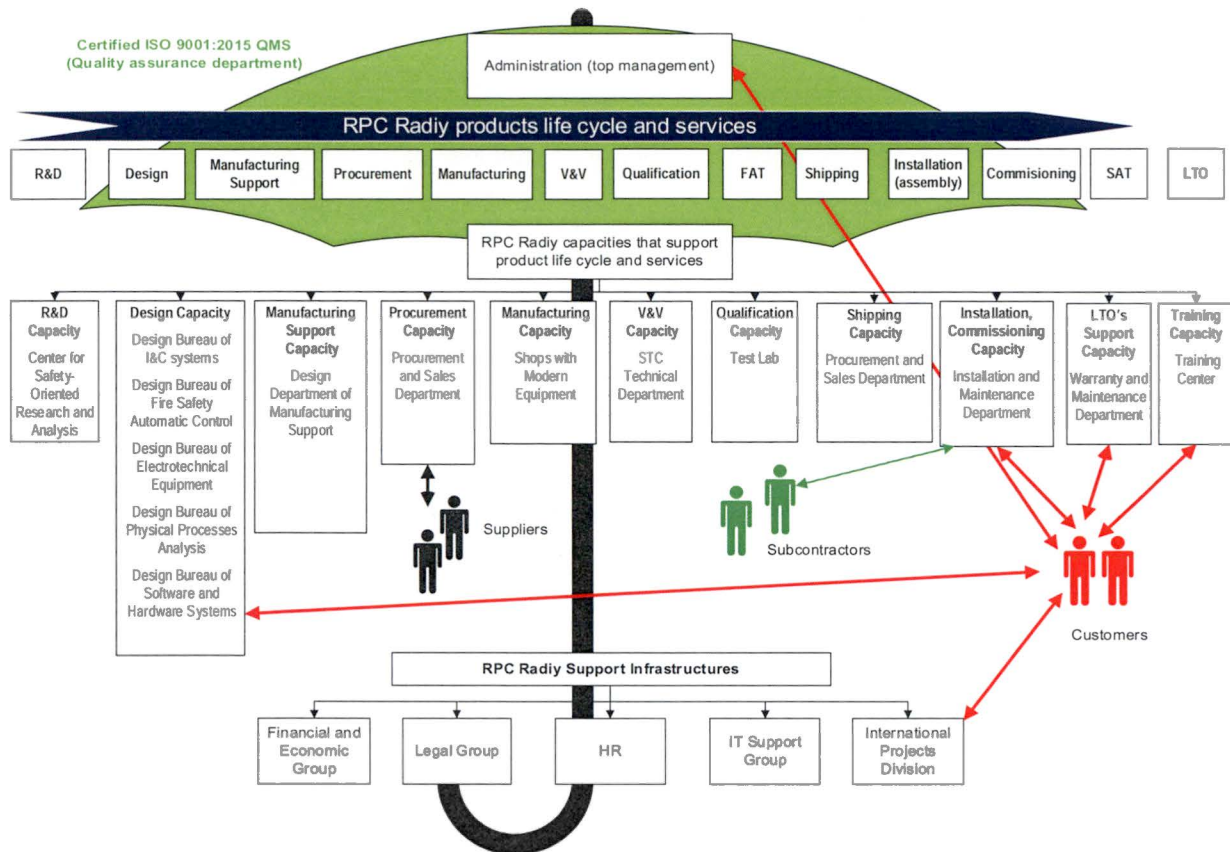
##### 3.2.1 RPC Radiy Organization

RPC Radiy is headquartered in Kropyvnytskyi, Ukraine. RPC Radiy provides a full range of design activities. In addition to the RadICS Platform equipment, RPC Radiy designs other hardware components, such as electrical distribution and switchgear cabinets and non-FPGA-based I&C systems. RPC Radiy has a broad range of technical capabilities and high degree of vertical integration: design, procurement, manufacturing, testing, and installation. The RPC Radiy organization structure is shown in Figure 3-1.

##### 3.2.1.1 RPC Radiy Design Bureaus

The RPC Radiy Design Bureaus include the following:

- Design Bureau of I&C Systems performs design of instrumentation and control and electrical systems for NPPs and other industrial facilities,
- Design Bureau of Fire Safety Automatic Control performs design of fire detection and video surveillance systems for NPPs and other industrial facilities,
- Design Bureau of Electrotechnical Equipment designs RTS, ESFAS, RPCLS, and electrical distribution control systems,
- Design Bureau of Physical Processes Analysis develops industrial seismic sensors and seismic detection systems, and
- Design Bureau of Software and Hardware Systems develops new platforms and systems, performs reverse engineering, and supports Radiy activities during international projects.



**Figure 3-1: RPC Radiy Organization Structure**

RPC Radiy has adopted design processes and QMS practices that comply with industry wide safety requirements for I&C systems as described in IEC 61508 (Reference 3-6), as well as specific requirements for nuclear I&C systems as described in the IAEA and IEC standards for nuclear facilities.

RPC Radiy designers have been involved in the development of I&C systems for the nuclear industry since 1995 and with FPGA-based applications since 1998. The RPC Radiy methods are based on the company's experience, continuous improvement processes, and the best international FPGA design practices. RPC Radiy also collaborates with the international NPP community, including the EPRI, to shares FPGA-related experience.

RPC Radiy technical departments and top management support the designers' professional development. Training of designers is performed on a regular basis to achieve the appropriate staff qualification levels. All training activities are performed in accordance with the RPC Radiy QMS.

### **3.2.1.2 Research and Development (R&D)**

RPC Radiy is one of the leading companies in the world providing FPGA-based I&C solutions to the nuclear industry and seeking new applications where FPGA technology can be utilized. The ongoing

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investment in Research and Development (R&D) activities leads to continuous improvement of its products.

The Scientific and Technical Center for Safety Infrastructure-Oriented Research and Analysis (STC) is the R&D Department. Some of the STC's main activities are as follows:

- Safety assessment of FPGA based I&C systems and applications,
- Design assessment: evaluating attributes, such as reliability, security, and maintainability of FPGA-based systems hardware and electronic design,
- Development of techniques and tools for multi-version system assessment of safety and diversity,
- Development of V&V techniques for the FPGA-based I&C systems,
- Participation in the development of standards and other normative documents associated with FPGA based I&C systems, support to the development of the RPC Radiy QMS, and
- Certification and licensing support of FPGA based and other I&C systems.

### **3.2.1.3 Manufacturing Support**

The Manufacturing Support department is responsible for the preparation of documentation to be used in the manufacturing of components and assembly units and their interconnecting parts, as well as manufacturing processes such as metal plating, polymeric coating, mounting, handling, rinsing, marking, testing, packing, and associated manufacturing control operations. All manufacturing support activities are performed in compliance with Company Standards, Guides, and Working Instructions/Procedures that are part of RPC Radiy QMS.

### **3.2.1.4 Procurement**

RPC Radiy performs all manufacturing activities in its own production facilities. Certain components, such as printed circuit boards (PCBs) and electronic components, as well as materials, such as metal plates, mounting hardware, and chemical are purchased parts. The selection of these components is performed by RPC Radiy technologists, procurement department personnel, QA staff (quality inspectors and auditors) and using Test Laboratory capabilities (if needed) in accordance with the requirements of generally accepted standards and specifications, which meet the requirements of the ASME NQA-1b-2007 (Reference 3-7) and the guidance in EPRI NP-5652 (Reference 3-8) and EPRI TR-102260 (Reference 3-9).

According to requirements of ISO 9001, ASME NQA-1b-2007, and other related standards, it is necessary to establish a supplier evaluation process to provide reasonable assurance that a commercial grade item will successfully perform its intended safety function. Information required for the evaluation of the RPC Radiy suppliers is obtained via the following methods:

- Testing (Special Tests and Inspections);
- Suppliers' assessment (Commercial Grade Survey),
- Suppliers' inspection (Source Verification), and
- Statistical estimation (Acceptable Supplier/Item Performance Record).

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The supplier evaluation and selection process is implemented by the Procurement Department in accordance with established procedures. The capability of a supplier to provide products that conform to the specified technical requirements is evaluated. Suppliers are required to identify all regulatory documents used for products manufacturing and provide them to RPC Radiy, as requested. Product delivery terms are evaluated to the ability of the supplier to deliver products timely in accordance with a plan of delivery. The Procurement Department Head can decide to audit a supplier to confirm the quality of supplied products. Audits are performed in accordance with established procedures by authorized Procurement Department employees. An audit report is provided to the Director of Marketing, Logistics, and Procurement. Based on audit report, the Director of Marketing, Logistics and Procurement makes the decision on further cooperation with subsequent execution of a contract with this supplier and including of this supplier into the List of Approved Suppliers.

The following criteria are used for supplier selection:

1. quality of delivered items:
  - reliability data of supplier items
  - quantity of unaccepted materials due to noncompliance with requirements
  - acceptability of deviations from requirements at various stages throughout the entire scope of delivery
  - quality and completeness of the documentation
  - parts traceability
  - availability of a certified QMS
2. observance of delivery terms:
  - timely delivery of order items
  - compliance with commercial and legal conditions of the contract
  - in case of justified delays, the suppliers' ability and willingness to implement a successful schedule recovery plan
3. price policy and terms of payment:
  - compatibility of terms of payment with the RPC Radiy financial strategy
  - competitive pricing
  - production capability
  - financial health of the company
  - ability and willingness to support their clients during challenging times
4. other requirements:
  - Ability of the suppliers' staff to communicate in a clear and open fashion

All above mentioned activities are performed by the RPC Radiy Procurement and Sales Department on a regular basis, allowing us to maintain an up-to-date list of qualified suppliers.

RPC Radiy has implemented procedures for performing incoming inspection to prevent the usage of counterfeit materials in digital I&C systems. The inspection is used to check the availability of documentation for products that certify the quality, completeness, control, and conformity of product quality to specified regulatory documents. The inspection also checks product packaging and marking. Sampling is used to check product attributes using various test methods (e.g., titrimetric, photometric,

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spectroscopic, and gravimetric testing methods) or analysis based on functional testing to controlled parameters.

### **3.2.1.5 Manufacturing**

RPC Radiy has the following manufacturing capabilities and facilities:

- Metal working shop equipped with automated sheet shearing machines, sheet bending presses, turret punch presses, table spot welding machines, and automated welding machines for assembling components and complete cabinets,
- Formed-in-place foam gasket line for polyurethane foam or silicone sealing contours gasket on the doors and different panels of the chassis/racks/cabinets, equipped with automated mixing and dispensing machines,
- Galvanic coating lines,
- Polymeric powder and seal coating lines,
- Automated line for PCB surface mounting (including soldering) equipped with an automatic solder pastes screen printer, inspection conveyor, automatic surface-mount device pick and place machine, inspection conveyor, automatic convection soldering system, and automated X-ray tomography system for soldering quality control,
- Facilities for manual heavy components, as well as production lines for surface mounting of connectors on the PCBs with quality inspection workstations,
- PCB washing and protective coating (including protection against tropical conditions) facilities using Silicone Conformal Coating (Electrolube DCA SSC 3 type),
- Fiber-optical patch cables manufacturing facility equipped with a video fiber microscope, polishing machine, fiber optic curing oven, and universal optical fiber test platform/ reflectometer,
- Facilities equipped with special measurement, monitoring, and simulation equipment for calibration of electronic and electric assemblies and systems,
- Facilities for the repair of PCBs, modules, assemblies, and other parts associated with I&C systems. These are equipped with disassembling, demounting, coating, soldering, measurement, monitoring, and simulation equipment, and
- Facilities for the inspection of soldering in PCBs, electronic, and electrical assemblies.

The RPC Radiy manufacturing and inspection facilities comply with the QMS, which complies with applicable ISO, IEC, and Institute for Printed Circuits (IPC) standards.

### **3.2.1.6 Verification and Validation**

RPC Radiy has established a V&V program in full compliance with processes defined in international standards. The following V&V methods are in use:

- Documents review,
- Failure and mode effect analysis (FMEA),
- Static code analysis and code review,
- HDL code functional testing,
- Logic level simulation, timing simulation and static timing analysis (for FPGA ED),

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- Reports review of synthesis, place and route, bitstream generation (for FPGA ED),
- Fault insertion testing (FIT), and
- Integration testing, validation testing.

RPC Radiy prefers the use of proven V&V tools over manual methods to eliminate human error. The above tools are purchased only from well-established vendors, with a good track record of configuration management, V&V, problem notification and resolution, and support and training materials.

The company QMS prescribes that all commercial software-based tools used for V&V should be tested and evaluated with the issuance of relevant evaluation reports. In addition to commercial software-based tools, RPC Radiy developed custom software-based and hardware-based tools in-house for V&V activities that have been tested and validated.

RPC Radiy V&V capabilities are supported by the STC, a department that is technically, administratively, and financially independent from the Design departments. Personnel performing V&V activities have a strong theoretical background and practical experience on design and testing of software and FPGA ED. RPC Radiy practices are in line with those followed by other organizations involved in the design of FPGA-based safety and non-safety I&C solutions for NPPs and in compliance with international standards. STC took an active part in the SIL 3 certification of RadICS Platform.

The V&V process for the RadICS Platform is described in further details in Section 7.4.

### **3.2.1.7 Qualification Test Laboratory**

Equipment qualification (EQ) testing for RPC Radiy I&C systems is performed in the RPC Radiy testing laboratory, which is certified by the National Accreditation Agency of Ukraine<sup>2</sup> to be in conformance with ISO/IEC 17025:2005 (Reference 3-10). The testing laboratory is equipped with all the necessary certified test equipment. The above test equipment is calibrated in compliance with ISO 10012:2003 (Reference 3-11). The testing laboratory is operated by trained and experienced staff.

The facilities include test benches for seismic qualification and environmental qualification; equipment aging chambers; and I&C systems simulation/modeling facilities. Qualification test capabilities include: radiation exposure and dust resistance (via approved service supplier); pressure, temperature, and humidity resistance; seismic qualification, vibration and other mechanical shock resistance; and electrical insulation, electrical safety, and electromagnetic compatibility. RPC Radiy EQ processes comply with EPRI qualification methods.

### **3.2.1.8 Storage and Shipping**

RPC Radiy storage, packing, and shipment procedures ensure the following:

- Protection against equipment physical and functional damage resulting from mechanical or environmental damage,
- Labeling of parts in compliance with customer requirements,

<sup>2</sup> Affiliated member of the International Laboratory Accreditation Cooperation





- Packing in containers in compliance with customer requirements and adequate packaging in accordance with the type of equipment and transportation mode, and
- Provision of a complete and detailed packing list.

RPC Radiy procedures prescribe methods and assign responsibilities for the handling of defective products. Where required to store or ship products that do not meet requirements, these will be properly identified and controlled to avoid unintended use.

### 3.2.2 Quality Management System

Between 1994 and 2003 the Company has developed, implemented, and put into action the QMS that conformed to the requirements of ISO 9000 series standards. In February 2004, RPC Radiy passed the certification audit by the Ukrainian State Agency "State Regulatory Center of Delivery and Service Quality" of quality certification system "SERTATOM." This certified RPC Radiy compliance with requirements of the national standard DSTU ISO 9001-2015 (Reference 3-12).

In 2008, after analyzing a set of documents, including QMS, the State Committee of the Nuclear Regulations in Ukraine expanded the previously granted the Activity License to authorize RPC Radiy to perform the design and manufacturing activities of certain nuclear products.

In 2009 RPC Radiy introduced an updated QMS that it believes satisfies the requirements of 10 CFR Part 50 Appendix B and ASME NQA-1-2008 to prepare for a broader international presence; however, the QMS was organized and aligned to ISO 9001:2008.

#### 3.2.2.1 International Certification Activities

Information on the international certification activities is provided to give the NRC some context regarding the effectiveness of the RPC Radiy QMS design and implementation, since it may not be familiar with RPC Radiy and its business operation.

In January 2005, the RPC Radiy QMS was certified in the International Certification System by the TÜV<sup>3</sup> Rheinland InterCert for compliance with requirements of international standard ISO 9001:2008. Based on the successful audit, TÜV Rheinland InterCert issued a certificate confirming that the required production quality controls were established at RPC Radiy. Based on an additional audit performed by the International Certification Agency TÜV Rheinland InterCert in October 2011, RPC Radiy obtained a new certificate for compliance with standard requirements of ISO 9001:2008. The certificate's scope included design, manufacturing, installation, and maintenance of instrumentation and control systems and the fire alarm system, including systems and equipment important to safety for nuclear power plants. The certificate was updated by TÜV Rheinland InterCert in 2013. In 2016, the QMS was certified by Quality Austria for compliance with requirements of ISO 9001:2015.

Inputs from other design and manufacturing companies, performing audits to assess RPC Radiy as a potential supplier, also helped improve the RPC Radiy QMS. In 2010, the RPC Radiy QMS was assessed by the former Atomic Energy of Canada Limited (AECL) (now CANDU Energy) Procurement Department to confirm the implementation and effectiveness of the QMS. AECL's Supplier's QMS Audit was

<sup>3</sup> Technischer Überwachungsverein

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conducted to evaluate the ability of RPC Radiy to supply products that can meet the AECL requirements. RPC Radiy standards were modified and implemented to successfully pass the AECL audit. Based on the audit's results, AECL concluded that the RPC Radiy QMS complies with the Canadian Standards Association (CSA) CAN3-Z299 series and subsequently RPC Radiy was included in the official AECL suppliers' list. To renew the approved vendor qualification status, CANDU Energy audited RPC Radiy in April 2013 against Canadian Standard CSA N Z299.1 (Reference 3-13) and ISO 9001:2008.

In 2014, the RPC Radiy QMS was assessed by Hungarian nuclear utility MVM Paks Nuclear Power Plant. The audit resulted in a conclusion that RPC Radiy is in full compliance with requirements to perform work such as design, manufacturing, repair, maintenance, expert activities, main contractor activities, and contributions in installation activities related to operation, maintenance, modification, and repair of I&C systems and components classified into the safety categories 2 and 3.

In 2015, RPC Radiy started work with ISO Ingenierie to align the RPC Radiy platform and applications against regulatory requirements in France. The activities include a review of RadICS Platform, as well as a review RadICS Platform, applications, and processes for compliance with IEC standards. The effort is designed to identify an approach for requirements gap analysis and safety case implementation to develop a road map for qualification of RadICS Platform technology in France.

### **3.2.2.2 International Atomic Energy Agency Mission at RPC Radiy Facilities**

The IAEA review mission titled, *Independent Engineering Review of I&C Systems in Nuclear Power Plants (IERICS)*, was established by the Nuclear Power Engineering Section of IAEA to conduct peer reviews of NPP I&C design documents, prototype systems, and systems in actual operation in NPPs. The IERICS review team consists of a group of invited subject matter experts from various IAEA Member States.

The IERICS Mission is based on appropriate IAEA documents, such as Safety Guides and Nuclear Energy Series Reports. The IERICS Mission took place at the RPC Radiy facilities in Kirovograd, Ukraine, in December 2010 and closed-out in March 2011 in the IAEA offices in Vienna, Austria. The subject matter of the above review mission was the RPC Radiy FPGA-based safety I&C RadICS Platform. The IERICS review was based on the IAEA Safety Guide NS-G-1.3 (Reference 3-14) and IAEA Nuclear Energy Series Reports NP-T-1.4 (Reference 3-15), NP-T-1.5 (Reference 3-16), and NP-T-3.12 (Reference 3-17).

The findings of the IERICS Mission were given in the Mission Report IERICS-UKR-2010, *Independent engineering review of instrumentation and control systems (IERICS) in nuclear power plants: IAEA review of the Radiy FPGA-based safety I&C platform and systems for NPPs*. The conclusions of the IERICS Mission included recommendations, suggestions, and an acknowledgement of good practices at RPC Radiy. The following items were identified as good practices:

- The use of FPGA technology and advanced approaches to the development of an FPGA based platform and systems,
- The design includes extensive on-line self-diagnostics at different system levels,
- Full implementation of the IAEA QMS requirements in the RPC Radiy Quality Management System, and
- Defect reporting program from which other organizations may benefit.





The IAEA review team confirmed that extensive, high quality engineering work, in compliance with the relevant sections of the IAEA Safety Guide NS-G-1.3, had been performed by RPC Radiy in the development of FPGA-based I&C systems.

### 3.2.2.3 IEC Safety Integrity Level Certification

[[ ]]<sup>a,c,e</sup> to a critical design review (CDR) based on EPRI TR-1011710 (Reference 3-18). IEC 61508 defines the requirements for suppliers to follow during product development to ensure that their products have a robust level of resistance to random hardware and “systematic” design failures. Compliance is evaluated by qualified third-party certification agencies that assess and certify that a product has been designed and developed in accordance with the standard.

The IEC 61508 SIL 3 certification process is shown pictorially in Figure 3-2.

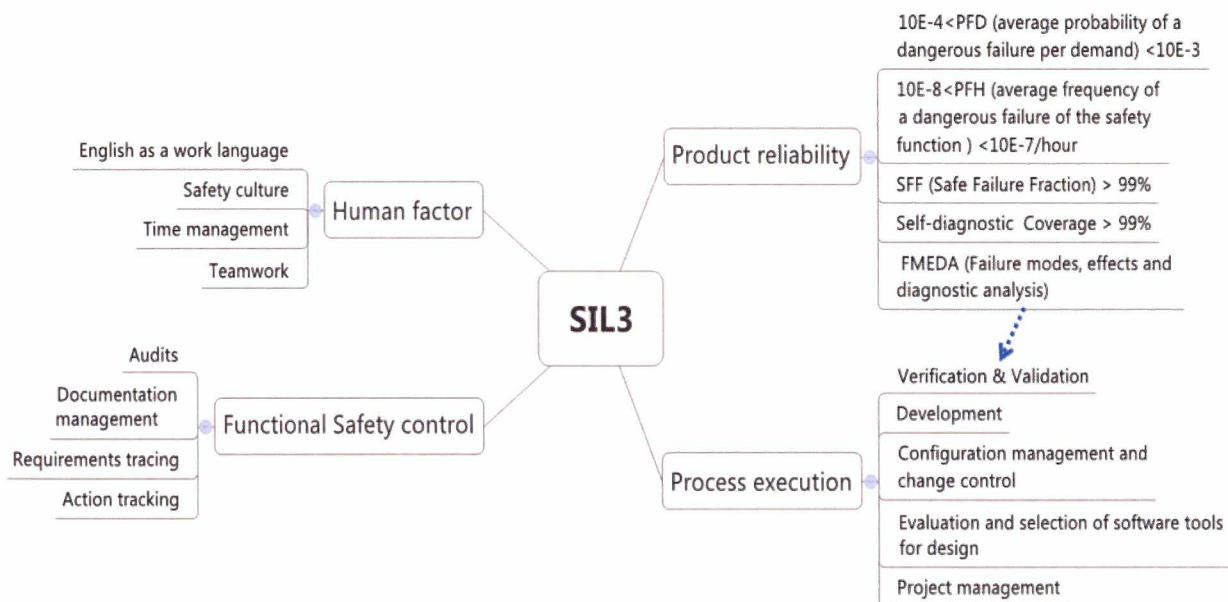


Figure 3-2: SIL 3 Certification Process

*exida* followed a rigorous process that verified the SIL of the RadICS Platform Hardware and associated ED, as well as its manufacturing and quality control procedures. [[

]]<sup>a,c,e</sup>

The IEC 61508 standard provides means of certifying systems based on four predefined SILs, where SIL 4 would be the most demanding level. SILs are order of magnitude levels of risk reduction. The IEC 61508 establishes three modes of operation:

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- Low Demand Mode: where the safety function is only performed on demand, and where the frequency of demands is no greater than one per year;
- High Demand Mode: where the safety function is only performed on demand, and where the frequency of demands is greater than one per year;
- Continuous Demand Mode: where the safety function is a part of normal operation.

The SIL table for appropriate measures for a NPP protection system is shown in Table 3-1.

**Table 3-1: IEC 61508 SIL Table for Demand Mode**

Safety Integrity Level	Average Probability of a Dangerous Failure on Demand of the Safety Function (Low Demand Mode of Operation)	Average Frequency of a Dangerous Failure of the Safety Function, 1/hour (High Demand and Continuous Modes of Operation)	Risk Reduction Factor
SIL 4	$\geq 10^{-5}$ to $< 10^{-4}$	$\geq 10^{-9}$ to $< 10^{-8}$	100,000 to 10,000
SIL 3	$\geq 10^{-4}$ to $< 10^{-3}$	$\geq 10^{-8}$ to $< 10^{-7}$	10,000 to 1,000
SIL 2	$\geq 10^{-3}$ to $< 10^{-2}$	$\geq 10^{-7}$ to $< 10^{-6}$	1,000 to 100
SIL 1	$\geq 10^{-2}$ to $< 10^{-1}$	$\geq 10^{-6}$ to $< 10^{-5}$	100 to 10

The SIL certification process requires that products developed under a Functional Safety Management Plan (FSMP) to be audited in stages by the independent certification agency. The FSMP describes the process and procedures used to design; verify and validate; and maintain the RadICS Platform. The FSMP defines the specific management responsibilities for the RadICS Platform development project. The FSMP takes all IEC 61508 requirements into consideration and mandates that they be applied throughout the product life cycle.

The SIL certification process outlined in IEC 61508 requires the preparation of a set of documents specific to each of the phases of the product life cycle. These documents must be subject of an independent auditing process and assessment by a Certification Body.

The auditing process starts early in the product development process with an independent Functional Safety Assessment of the readiness of the processes and product(s). Internal Functional Safety Audits (FSAs) are conducted after successful completion of the development process at specific milestones, as described below.

The first internal FSA usually takes place early within the development process, after the functional and safety requirements definition, when V&V plans and product architecture design are available. Other activities that need to be completed before the commencement of this first internal FSA are the safety concept definition, the section dealing with suppliers and the implementation of a configuration control process.





The objectives of this internal FSA are to verify that:

- The required documents have been approved for use and are under proper configuration
- Control,
- Project QA manual is in place and in line with corporate and project objectives and quality requirements,
- The QA programs of suppliers of materials and services are in line with the project quality requirements as defined in the project QA manual,
- Whether all verification activities associated with this phase of the development process were correctly executed,
- An effective action tracking process was instituted and followed by all members of the team,
- An effective requirement tracing process was instituted and followed by all members of the team,
- The Safety Concept for the product is clearly defined,
- The required competences and accountabilities for the project are clearly identified and the organization is staffed accordingly, and
- An effective Change Management process was instituted and followed by all members of the verification team.

All the above is consistent with activities as described in the RadICS Platform FSMP.

The objectives of subsequent internal FSAs are:

- To address observations from the previous FSAs,
- To ensure continued compliance with all applicable objectives, as defined for the first internal FSA,
- To ensure that the development process continues to follow the FSMP,
- To verify that only qualified tools are used in the development process,
- To determine whether conditions are met for the commencement of the independent Functional Safety Assessment by the corresponding Certification Body,
- To ensure compliance with the FSMP at each audited project phase,
- Verify that the product release baseline audit has been successfully performed, and
- Verify that fault insertion tests cover the appropriate measures.

The independent Functional Safety Assessment is performed by an external certification agency and documented in a report in accordance with the FSA plan.

The following information is required as input to the independent Functional Safety Assessment:

- IEC 61508,
- The final product functional, safety and performance requirements, and
- The final product safety integrity requirements (requirements for probability rates and reliability indexes).

On completion of the independent Functional Safety Assessment, the certification agency publishes the following documents: Functional Safety Assessment Plan, Functional Safety Assessment Report and the certificate of product's compliance.

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In 2010, RPC Radiy senior management set as one of the company's goal, to use our RadICS Platform for Safety Instrumented System (SIS) applications under IEC 61508. Because of the above, the following decisions were made:

- To move from being a turnkey only supplier (supplier of entire systems) to different contractual arrangements where the RadICS Platform could be used for implementation of different safety and non-safety applications and in which RPC Radiy or the client could play the role of the integrator,
- To pursue certification of the RadICS Platform to SIL 3 based on IEC 61508, and
- To contract **exida** Inc. as the independent assessor and certification agency.

In 2011, **exida** performed a preliminary assessment to assist RPC Radiy management in determining the level of effort required to reach SIL 3 certification for the RadICS Platform, assuming a 2-out-of-3 voting logic architecture. The assessment included:

- IEC 61508 Process Gap Analysis (product development and support processes evaluation) and
- System Failure Mode and Effect Analysis (high-level design assessment).

The results of the **exida** assessment formed the basis of a new comprehensive project aimed at enhancing the life cycle processes of the RadICS Platform to the level required for SIL 3 certification.

Changes to the platform development process and detailed planning of associated activities for the upgrading of the RadICS Platform to comply with SIL 3 requirements were implemented during the first phase of the project. Personnel, Document, Functional Safety Management, Configuration Management and Overall V&V plans, along with Safety Requirements Specification and other documents covering all aspects of the life cycle were developed during this phase of the project.

Results of subsequent phases of the certification project showed that all the **exida** recommendations were considered and successfully implemented.

The subsequent assessments performed by **exida**, as well as final independent Functional Safety Assessment in August 2014, confirmed that RPC Radiy processes comply with SIL 3 requirements and the RadICS Platform meets SIL 3 requirements in both multiple and single channel configurations.

### **3.3 RadICS Quality Assurance Program**

#### **3.3.1 Radics LLC Organization**

The Radics LLC organization is designed to provide for safety-related I&C systems to NPPs using the RadICS Platform equipment. Radics LLC, based in Kirovograd, Ukraine is responsible for all RadICS Platform-based application project activities except the manufacturing of the RadICS Platform equipment. The RadICS Platform equipment is manufactured by RPC Radiy, as described in Section 3.2.

The main departments within Radics LLC that are involved in a RadICS Platform-based application project include:

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- Supply and Sales Department – Provides customer technical and QA requirements from procurement documents. Provides storage, packaging, and shipping for completed RadICS Platform-based systems designed and integrated by Radics LLC. Packaging and shipment are performed by Radiy under the Radiy QMS. All these requirements are included into the purchase order and controlled by Radics LLC.
- Application Design Bureau – Develops project-specific I&C system designs based on RadICS Platform technology. The systems design work includes the system architecture, the Application EDs, and hardware that implement customer function requirements. The design work is based on using the RadICS Platform Development Tools and AFBL.
- Verification Department – Performs verification activities on the hardware and electronic design documents prepared by the Application Design Bureau, as specified in the Project Overall V&V Plan. The Verification Department is technically, administratively, and financially independent from the Application Design Bureau.
- Validation and Commercial Grade Dedication Department – Performs commercial grade dedication of RadICS Platform equipment provided by RPC Radiy. RPC Radiy designs and manufactures the RadICS Platform equipment, including the generic Platform EDs and the Platform and Application Function Block Libraries. Performs validation testing of RadICS Platform-based systems developed by Radics LLC. RPC Radiy performs validation testing of the generic RadICS Platform and FBL. The Validation and Commercial Grade Dedication Department is technically, administratively, and financially independent from the Application Design Bureau.
- Equipment Qualification and Calibration Department – Performs required EQ testing or analysis of equipment used for RadICS Platform-based systems.
- QA Department – Controls the Radics LLC QAPD and Radics LLC development standards and audits implementation of programs and processes. Responsible for independently planning and performing activities to verify the development and effective implementation of the Radics LLC QA Program. Supports commercial grade dedication activities for commercial grade surveys and source inspections, as specified by the commercial grade dedication plan.
- Technical Support and Maintenance - Performs commissioning, warranty support, customer technical support, spare parts availability control, consideration of claims, and customer complaints.

Figure 3-3 shows the Radics LLC organization and workflow interfaces for RadICS Platform-based I&C projects.

Figure 3-4 shows the Radics LLC product lifecycle and organizational responsibilities.

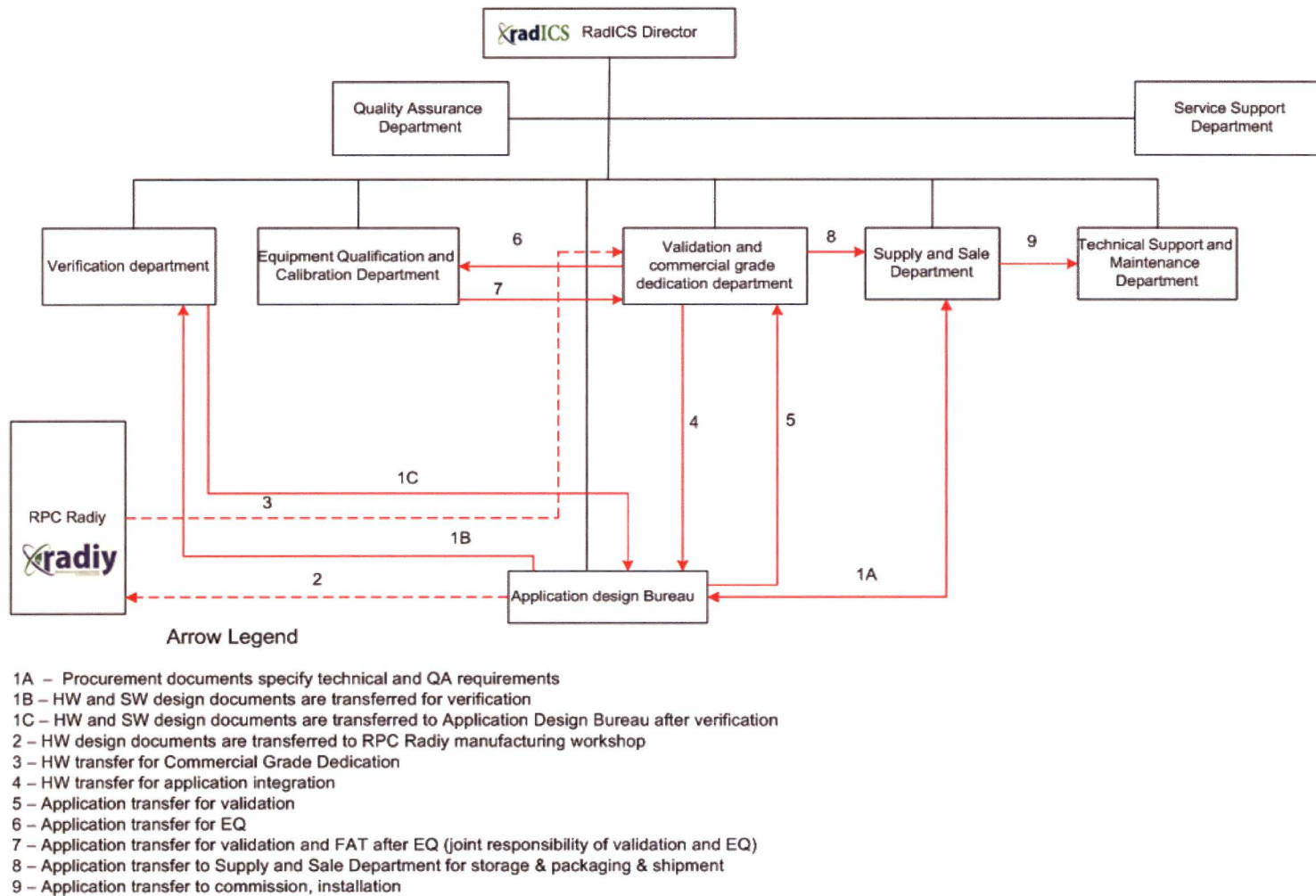
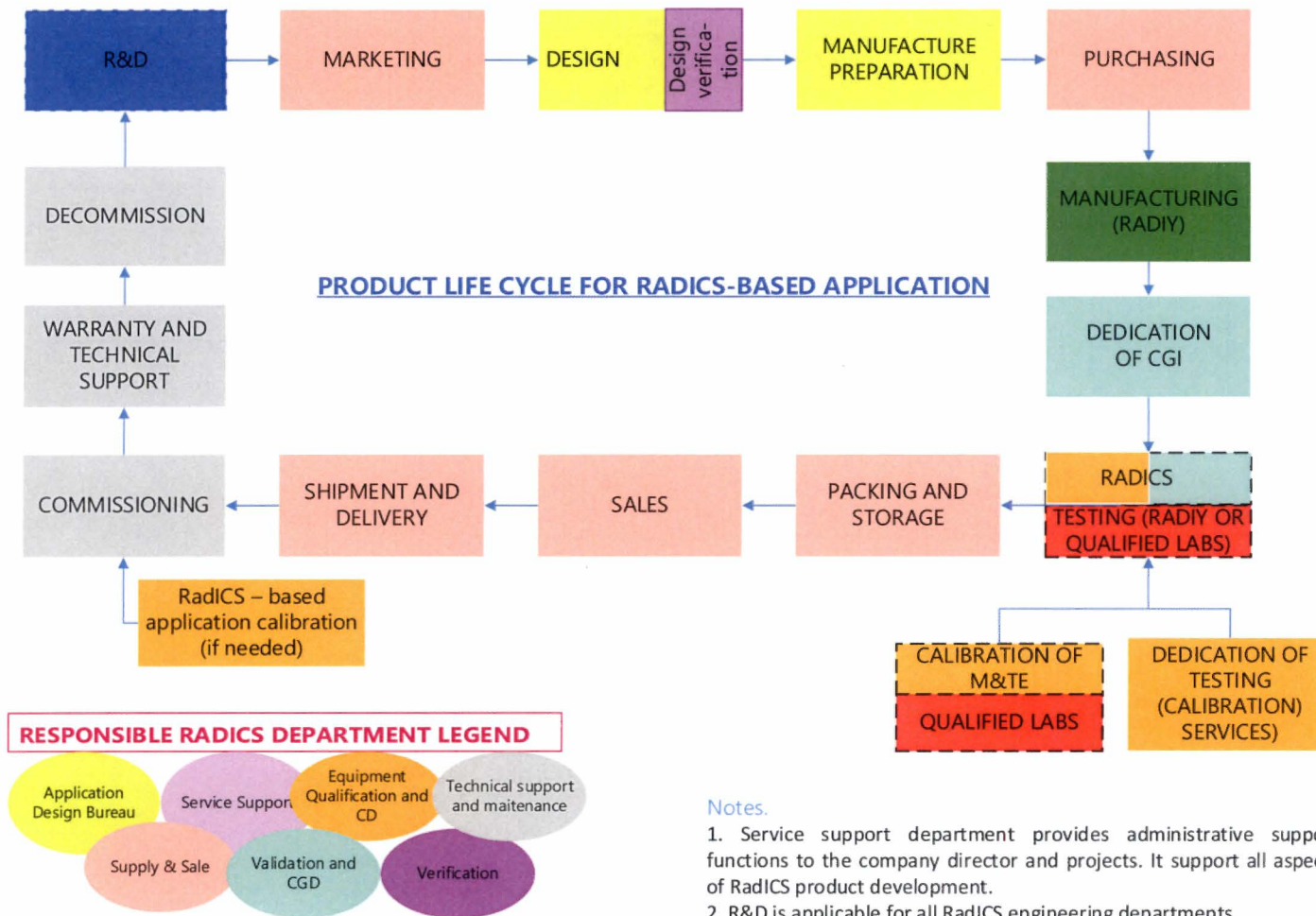


Figure 3-3: Radics LLC Organization and Workflow Interfaces



**Figure 3-4: Radics LLC Product Lifecycle and Organizational Responsibilities**

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### 3.3.2 Quality Assurance Program

The Radics LLC QAPD (Reference 3-19) is the top-level QA document of the 10 CFR Part 50 Appendix B QA program for the Radics LLC organization. The QAPD includes methods pertaining to managerial and administrative controls that meet the requirements of 10 CFR Part 50 Appendix B, RG 1.28, Revision 4, and NQA-1-2008/ NQA-1a-2009 Addenda. The Radics LLC QAPD is based on NEI 11-04A (Reference 3-20).

The Radics LLC QAPD defines specific responsibilities and authority for control of design, documentation, procurement, processes, inspection, testing, nonconformance, corrective action, and QA records. In addition, the Radics LLC QAPD defines requirements for inspection and audits. The Radics LLC QA Department is responsible for maintaining the Radics LLC QAPD.

The Radics LLC QAPD establishes the quality system document structure, which includes the following:

- Radics LLC QAPD is the upper tier quality requirements document,
- Radics LLC Quality Procedures implement the QAPD requirements for programs and processes,
- Radics LLC Quality Work Instructions provide standardized methods to accomplish quality-related work, and
- Radics LLC Forms and Records are used to create the implementation evident for quality-related work.

All Radics LLC activities for the processes described in the RadICS Topical Report are performed in accordance with the Radics LLC QAPD.

Radics LLC activities for supplier selection and evaluation comply with the applicable NQA-1-2008/2009a requirements for source (supplier) evaluation and selection and periodic re-evaluation. The Radics LLC QAPD is implemented through procedures that control the selection and qualification of suppliers and maintenance of the Qualified Suppliers List. QA evaluators perform supplier evaluations, which include assessment of corrective action history, nonconformance submittals, organization changes, etc. A performance rating is determined based on the evaluation of these criteria and a supplier can be added, retained, or removed from the Qualified Suppliers List. The scope of related activities performed by Radics LLC includes supplier audits and commercial grade surveys for commercial suppliers. The Radics LLC QAPD provides control for the selection and evaluation of suppliers for calibration and testing services.

The Radics LLC QAPD establishes procurement and dedication control programs designed to detect and prevent usage of counterfeit and fraudulently marketed products in its projects according to requirements of NRC Generic Letter 89-02 (Reference 3-21). The following Radics LLC QAPD measures are implemented in procedures:

- Involvement of engineering staff in the procurement and product acceptance process,
- Implementation of comprehensive source inspection, receipt inspection, and testing programs,
- Establishment of engineering based, programs for review, testing, dedication of commercial-grade products for suitability, and
- Appropriate training in the detection of these items to applicable personnel.

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As described in Section 3.2, RPC Radiy works under their ISO 9001:2015 QMS and maintains its own set of procedures for the design and manufacturing of the RadICS Platform equipment. Radics LLC uses its commercial grade dedication process to accept the RPC Radiy components into the Radics LLC QAP. During the product development life cycle phases where RPC Radiy performs work, Radics LLC verifies the RPC Radiy generic Platform ED and FBL activities through commercial grade dedication and project-specific V&V activities, as described in the commercial grade dedication plan. The Radics LLC staff has the capabilities to perform the RPC Radiy work on the RadICS Platform technology and is technically competent to review and approve the RPC Radiy work. Radics LLC performs dedication of commercial grade items procured from RPC Radiy, based on the process described in EPRI NP-5652, EPRI TR-102260, and EPRI TR-106439 (Reference 3-22). The initial commercial grade dedication of the RadICS Platform technology is described in Chapter 4.

The QA controls applied to the development of Platform and Application EDs for the RadICS Modules are described on Chapter 7. The QA controls applied to the development of the Platform and AFBL for use in the EDs for RadICS Modules are described on Chapter 8. The secure development environment controls are described in Chapter 11. Radics LLC has established classification and acquisition process control for software-based development tools, as described in Section 8.3.

### 3.3.3 Radics LLC NQA-1 Implementation Activities

Radics LLC started to work with Global Quality Assurance, Inc. (GQA) in 2015, to develop a QAPD and a complete set of implementing quality procedures and working instructions to fully align Radics LLC QAPD with 10 CFR Part 50 Appendix B. The Radics LLC QAPD has been developed to be fully compliant with ASME NQA-1-2008/NQA-1a-2009, as endorsed by RG 1.28, Revision 4. This work was performed to support the development of the RadICS Topical Report for submittal to NRC for review and approval.

A complete set of procedures was developed to implement quality controls for all 18 criteria from 10 CFR Part 50 Appendix B. The Radics LLC quality procedures are listed in Table 3-2.

**Table 3-2: Radics LLC Quality Procedures**

Requirements from NQA-1-2008 and Appendix B	Quality Procedures	
Criterion I, Organization		
Criterion II, Quality Assurance Program	QP 02-1	Management Review Procedure
	QP 02-3	Qualification of Audit and Survey Personnel
	QP 02-4	Indoctrination, Training and Personnel Qualifications



Requirements from NQA-1-2008 and Appendix B	Quality Procedures	
Criterion III, Design Control (Design, Hardware Design, and V&V)	QP 03-1	Design Analysis
	QP 03-2	Hardware Design
	QP 03-3	Software Design <sup>4</sup>
	QP 03-4	Software Design Verification <sup>4</sup>
	QP 03-5	Hardware Design Verification
	QP 03-6	Integration
	QP 03-7	Configuration Management Procedure
	QP 03-8	Determining Functional Safety Classification and Acquisition Guidance for Design and Analysis
	QP 03-9	Secure Development and Operational Environment Procedure
	QP 03-10	Design Control (General Procedure)
	QP 03-11	Verification and Validation (General Procedure)
Criterion IV, Procurement Document Control	QP 04-1	Procurement Document Control and Purchasing Procedure
Criterion V, Instructions, Procedures, and Drawing	QP 05-1	Document Development Procedure
	QP 05-2	QA Project Plan Development
Criterion VI, Document Control	QP 06-1	Document Control Procedure
	QP 06-2	Electronic Document Control
Criterion VII Control of Purchased Material, Equipment, and Services	QP 07-1	Supplier Evaluation and Approval Procedure
	QP 07-2	Items or Services Acceptance Procedure
	QP 07-3	Commercial Grade Dedication Procedure
	QP 07-4	Commercial Grade Survey Procedure
Criterion VIII, Identification and Control of Materials, Parts, and Components	QP 08-1	Product Identification and Indication of Test and Inspection Status
	QP 08-2	Shelf Life Control
Criterion IX Control of Special Processes	QP 09-1	Control of Special Processes
Criterion X Inspection	QP 10-1	In-Processes and Final Inspection Procedure

<sup>4</sup> Including electronic logic design



Requirements from NQA-1-2008 and Appendix B	Quality Procedures	
Criterion XI Test Control	QP 11-1	Test Control Procedure
	QP 11-2	Test Loop Alignment
Criterion XII Control of Measuring and Test Equipment	QP 12-1	Control of Measuring and Test Equipment Procedure
	QP 12-3	Dedication of Calibration and Testing Services
Criterion XIII Handling, Storage and Shipping	QP 13-1	Handling, Storage, and Preservation Procedure
	QP 13-2	Marking and Labeling
	QP 13-3	Packaging and Shipping Procedure
Criterion XIV Inspection, Test, and Operating Status	(This requirement is covered by QP 08-1)	
Criterion XV Nonconforming Materials, Parts, or Components	QP 15-1	Control of Nonconforming Items
	QP 15 -2	Reporting of Noncompliance in Accordance with 10 CFR Part 21
Criterion XVI Corrective Action	QP 16-1	Corrective Action
	QP 16-2	Software Problem Reporting Procedure <sup>5</sup>
Criterion XVII Quality Assurance Records	QP 17-1	Control of Records Procedure
	QP 17-2	Electronic Records Control Procedure
Criterion XVIII Audits	QP 18-1	Internal and External Audit Procedure
	QP 19-1	Order Entry Contract Review Procedure

A comprehensive training plan was prepared for Radics LLC personnel on the key elements of the QA Program document and implementing procedures. A qualification and training program was implemented for QA lead auditors and survey personnel using the services of GQA. Initial training of personnel was performed by SunPort (Lausanne, Switzerland) at the RPC Radiy site in April 2015. The Radics LLC staff has been certified on the following topics:

- Internal/External Auditing topics and techniques
- Organization safety culture, root cause determination and problem-solving techniques
- Means to identify and deal with Counterfeit, Fraudulent, and Suspect Items
- Commercial Grade Item Dedication

<sup>5</sup> Including electronic logic design





GQA completed a third-party evaluation in August 2016 (Reference 3-23). Evaluation QAP\_EVAL-2016 was performed to assess the adequacy of the Radics LLC Quality Assurance Program documents for meeting 10 CFR Part 50 Appendix B, 10 CFR Part 21, ASME NQA-1-1994, NQA-1-2008, and NQA-1a-2009. The evaluation was performed as a document audit of current policies and quality procedures to assess the Radics LLC QAPD for addressing applicable requirements for control over quality activities for supplying nuclear safety-related digital instrumentation and control equipment. The scope of the evaluation included the latest approved revisions of the Radics LLC QAPD, 42 Quality Procedures, and 3 significant Work Instructions.

The evaluation found that the Radics LLC QAPD was a comprehensive network of policies, procedures, instructions, and forms that address the nuclear quality assurance requirements in detail. The Radics LLC QAPD also reflect recent regulatory developments, provisions and guidance of impact to nuclear licensees and their suppliers. GQA concluded that the Radics LLC QAPD is comprehensively documented and compliant with stated requirements. Three evaluation comments were submitted for corrective action in accordance with the Radics LLC QAPD.

### 3.3.4 Corrective Action Program

The Radics LLC corrective action procedure (Reference 3-24) addresses corrective action for conditions adverse to quality related to the following sources:

- Supplier deficiencies in processes and / or controls identify during a Commercial Grade Survey (as described in QP 07-4),
- Findings from internal audits (as described in QP 18-1),
- Nonconforming items whose apparent causes resulted in dispositioned rework, replacement or repair (as described in QP 15-1) and for which the dispositioning process has resulted in a decision to investigate the cause of the issue further,
- Customer complaints, returns, or audit findings,
- Software (including electronic logic design) that is assigned a Severity 1 (Critical Error) with a Priority Level 1 (as described in QP-16-2), and
- Trend analysis suggests recurring issues regardless of source.

This procedure acknowledges the implementation of related procedures that correct conditions adverse to quality and prescribes a defined process for attending to significant conditions adverse to quality, regardless of source (e.g., item, audit, programmatic, complaint or trend). The defined process for significant conditions adverse to quality includes causal analysis, taking actions to mitigate or prevent recurrence, and verification of completed corrective actions.

Each corrective action report is evaluated for 10 CFR Part 21 (Reference 3-25) reporting applicability.

### 3.3.5 10 CFR Part 21 Problem Reporting

Radics LLC, as the designer and supplier of digital I&C systems to U.S. commercial nuclear licensees, is required to comply with 10 CFR Part 21. The Radics LLC reporting procedure for defects and noncompliance (Reference 3-26) describes the process for ensuring compliance with the requirements of 10 CFR Part 21. This procedure establishes the requirements for evaluation and reporting of defects

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and noncompliance in accordance with 10 CFR Part 21. This procedure applies to all materials, components, subassemblies, services, and finished items that are basic components and that have been delivered to a U.S. nuclear customer. The Radics LLC QA Manager is the Responsible Officer for the effective implementation of this procedure.

### 3.3.6 Maintenance Process of NRC Safety Evaluation Report

RPC Radiy and Radics LLC will periodically update procedures related to the RadICS Platform technology and associated I&C system projects to continuously improve activities after issuance of the NRC Safety Evaluation Report (SER) for the RadICS Digital I&C Platform Topical Report. Additionally, some parts of the RadICS Platform might have to be modified to replace obsolete components or correct identified problems. The overall RadICS Platform and Application Lifecycles might require updates to reflect changes in RPC Radiy or Radics LLC management structures or quality programs.

Radics LLC working instructions define a change management process for future changes to the approved RadICS Platform (Reference 3-27). The change management process specifies the criteria and evaluation process to evaluate future platform changes for use. Radics LLC can use newer Radiy equipment (i.e., RadICS Platform Hardware and ED Modules) and development procedures provided that the specified criteria are met. The change management process is designed to ensure that:

- Changes to the approved RadICS Platform do not modify or eliminate the key design principles, key processing features, or key communication independence features,
- Changes to the RadICS Platform (i.e., Hardware and ED Modules) do not result in more than a minimal increase in the likelihood of occurrence of a malfunction, do not result in more than a minimal increase in the consequences of a malfunction, or do not create a possibility for a malfunction with a different result, and
- Changes to the Radics LLC or Radiy development procedures do not result in a reduction in the NRC-approved quality methods.

To the extent that product or process changes are confirmed to be within the established criteria in the Topical Report and SER, the RadICS Platform will be considered consistent and current with the Topical Report and SER. Changes that satisfy the criteria can be used for a plant retrofit project. Changes that do not satisfy one or more of the criteria cannot be used for a U.S. plant project without specific NRC review and approval. If changes are required to Topical Report or SER, then Radics LLC will provide a revision to the Topical Report to reflect those changes to be reviewed and approved by the NRC before allowing products to be developed or systems designed under the new process for installation in the U.S.

Radics LLC records requirements and periodic reporting obligations are specified for the change evaluations to support a review by independent parties or audits by NRC.

### 3.4 Chapter 3 References

- 1 ISO 9001:2015, "Quality management systems – Requirements"
- 2 10 CFR Part 50 Appendix B, "Quality Assurances Requirements for Nuclear Power Plants and Fuel Reprocessing Plants"
- 3 ASME NQA-1-2008, "Quality Assurance Program Requirements for Nuclear Facilities"

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- 4 ASME NQA-1a-2009, "Quality Assurance Program Requirements for Nuclear Facilities"
- 5 Regulatory Guide 1.28, Revision 4, "Quality Assurance Program Criteria (Design and Construction)"
- 6 IEC 61508:2010, "Functional Safety of Electrical/Electronic/Programmable Electronic Safety-related Systems"
- 7 ASME NQA-1b-2007, "Quality Assurance Program Requirements for Nuclear Facilities"
- 8 EPRI Report NP-5652, "Guideline for the Utilization of Commercial Grade Items in Nuclear Safety-Related Applications (NCIG-07)," dated June 1, 1988
- 9 EPRI TR-102260, "Supplemental Guidance for the Application of EPRI Report NP-5652 on the Utilization of Commercial Grade Items," 1994
- 10 ISO/IEC 17025:2005, "General requirements for the competence of testing and calibration laboratories"
- 11 ISO 10012:2003 "Measurement management systems -- Requirements for measurement processes and measuring equipment"
- 12 DSTU ISO 9001-2015 "Quality management system – Requirements"
- 13 CSA Z299.1, "Quality Assurance Program - Category 1"
- 14 IAEA Safety Guide NS-G-1.3 "Instrumentation and Control Systems Important to Safety in Nuclear Power Plants"
- 15 IAEA Nuclear Energy Series Report No.NP-T-1.4, "Implementing Digital I&C Systems in Modernization of Nuclear Power Plants"
- 16 IAEA Nuclear Energy Series Report No.NP-T-1.5, "Protecting Against Common-Cause Failures in Digital I&C Systems"
- 17 IAEA Nuclear Energy Series Report No.NP-T-3.12, "Core Knowledge on Instrumentation and Control Systems in Nuclear Power Plants"
- 18 EPRI Technical Report 1011710, "Handbook for Evaluating Critical Digital Equipment and Systems," Electric Power Research Institute, November 2005
- 19 QAPD-001, "Radics LLC Quality Assurance Program Description"
- 20 Nuclear Energy Institute Letter to NRC dated June 6, 2013, "Issuance of NEI 11-04A, Revision 0, Nuclear Generation Quality Assurance Program Description"
- 21 NRC Generic Letter 89-02, "Actions to Improve the Detection of Counterfeit and Fraudulently Marketed Products"
- 22 EPRI TR-106439, "Guideline on Evaluation and Acceptance of Commercial Grade Digital Equipment for Nuclear Safety Applications," October 1996
- 23 Global Quality Assurance letter to Radics LLC dated August 26, 2016, "Evaluation of the Radics LLC Quality Assurance Program Description"
- 24 Radics LLC Procedure QP 16-1, "Corrective Action"
- 25 10 CFR Part 21, "Reporting of Defects and Noncompliance"
- 26 Radics LLC Procedure QP 15-2, "Reporting of Noncompliance in accordance with 10 CFR Part 21"
- 27 Radics LLC Work Instruction WI 03-7/2, "RadICS Technology Change Evaluation Process"



## 4 RadICS Commercial Grade Dedication Plan

The RadICS Platform is the third-generation digital safety I&C platform developed by RPC Radiy in accordance with European nuclear safety standards for such systems. The basic U.S. licensing strategy to demonstrate that the generic RadICS Platform and the associated quality and electronic design life cycle processes comply with U.S. nuclear safety requirements is described in Chapter 1.

### 4.1 Commercial Grade Dedication Methodology

Radics LLC has developed a set of Commercial Grade Dedication Plan for the RadICS Platform (References 4-1 through 4-13). This plan outlines the various steps to be followed to dedicate the RadICS Platform. The results of the dedication have been documented in a set of Commercial Grade Dedication Summary Reports for the RadICS Platform after the plan was fully implemented (References 4-14 through 4-26).

#### 4.1.1 Definition of the Generic RadICS Platform

The generic RadICS Platform Electronic Designs is described in Chapter 6. The development of the RadICS Platform is described in Chapters 7 and 8. The EQ plan for the RadICS Platform is described in Chapter 9.

#### 4.1.2 Compliance with Dedication Guidance

EPRI NP-5652 (Reference 4-27) provides the upper tier framework for the technical basis for acceptance and the specific methods used to establish acceptance. NRC conditionally endorsed EPRI NP-5652 in Generic Letter 89-02 (Reference 4-28). EPRI TR-106439 (Reference 4-29) is based on the NRC-endorsed guidance in EPRI NP-5652 and tailors the guidance for the commercial grade dedication (CGD) of digital equipment. NRC approved EPRI TR-106439 (Reference 4-30). NRC also states in RG 1.152 (Reference 4-31) that EPRI TR-106439 contains adequate guidance to meet the requirements in IEEE Std 7-4.3.2-2003, Section 5.4.2 (Reference 4-32).

It is important to understand how this guidance relates to the use of testing in the acceptance review. Testing can be used to support acceptance in four distinct ways, each with its own set of rules.

Method 1 – Special Tests and Inspections - EPRI NP-5652 Section 3.1.2 states that “Method 1 should be used when the purchaser desires to verify critical characteristics after the item is received.” Method 1 testing is performed during the commercial grade dedication process. EPRI NP-5652 Section 2.5 specifies that this work must be performed in accordance with a 10 CFR Part 50, Appendix B program (Reference 4-33).

Method 2 - Commercial Grade Survey - EPRI NP-5652 Section 3.2.2 states that “Method 2 should be used when the purchaser desires to accept commercial grade items based on the merits of a supplier's commercial quality controls. These controls may constitute quality programs, procedures, or practices.” EPRI NP-5652 Section 3.2.3 states that “Two basic criteria must be met when conducting a commercial grade survey. The purchaser must confirm that the

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selected commercial grade item's critical characteristics are controlled under the scope of commercial quality system activities. The purchaser must also be reasonably assured that the commercial supplier's activities adequately control the commercial grade items supplied." EPRI NP-5652 Table 3-1 lists typical supplier controls that can be surveyed using Method 2, which includes testing. Similarly, EPRI TR-106439 Figure 3-2 shows a review of vendor testing as an element of the dedication process. EPRI NP-5652 Section 2.5 specifies that the review for acceptance of vendor testing must be performed in accordance with a 10 CFR Part 50, Appendix B program; however, the vendor testing itself is not performed in accordance with a 10 CFR Part 50, Appendix B program.

Method 3 - Source Verification - EPRI NP-5652 Section 3.3.1 states that "Method 3 involves the verification of critical characteristics by witnessing quality activities before releasing the item for shipment." EPRI NP-5652 Section 2.5 specifies that the verification for acceptance of vendor testing must be performed in accordance with a 10 CFR Part 50, Appendix B program; however, the vendor testing itself is not performed in accordance with a 10 CFR Part 50, Appendix B program.

Method 4 - Item/Supplier Performance Record - EPRI NP-5652 Section 3.4.1 states that "Method 4 allows the purchaser to accept commercial grade items based upon a confidence in the supplied item achieved through proven performance of the item. It also allows the purchaser to take credit for item performance based upon historical verification gained from the successful utilization of Methods 1, 2, or 3 or pertinent industry-wide performance data."

NRC Generic Letter 89-02 places two limitations of the use of EPRI NP-5652:

1. Acceptance Method 2, "Commercial-Grade Survey of Supplier", should not be employed as the basis for accepting items from suppliers with undocumented commercial quality control programs or with programs that do not effectively implement their own necessary controls. Likewise, Method 2 should not be employed as the basis for accepting items from distributors unless the survey includes the part manufacturer(s) and the survey confirms adequate controls by both the distributor and the part manufacturer(s).
2. Acceptance Method 4, "Acceptable Supplier/Item Performance Record," should not be employed alone unless:
  - a. The established historical record is based on industry-wide performance data that is directly applicable to the item's critical characteristics and the intended safety-related application; and
  - b. The manufacturer's measures for the control of design, process, and material changes have been adequately implemented as verified by audit (multi-licensee team audits are acceptable).

Radics LLC performed an initial assessment of the historical development records for the RadICS Platform as part of the CGD planning effort and made two broad conclusions. First, Radics LLC concluded that [[ ]]<sup>a,c,f</sup> would be needed to satisfy the U.S. regulatory requirements for [[ ]]<sup>a,c,f</sup>. These [[ ]]<sup>a,c,f</sup> and are described in Chapter 9. Second, Radics LLC concluded that the RadICS [[ ]]

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]]<sup>a,c,f</sup> were evaluated using Method 2.

Method 3 was used by Radics LLC to evaluate certain vendor processes used during the equipment qualification testing. It was also used to evaluate certain manufacturing processes used by RPC Radiy for the RadICS Platform equipment.

Method 4 was not used to compensate for shortcomings in legacy electronic designs nor was it used as a basis for establishing RadICS Module failure rates. Radics LLC has only used the RadICS Platform operating experience to demonstrate satisfactory performance with the platform technology.

The sources of guidance related to dedicating a commercial grade digital safety I&C platform are EPRI TR-106439 and EPRI TR-107330 (Reference 4-34). Implementation of this guidance for dedication of the generic RadICS Platform is described below.

The Commercial Grade Dedication Plan for RadICS Platform is based on established guidance:

- EPRI TR-106439 for the CGD of the RadICS Platform developed to the RPC Radiy QMS and IEC Requirements
- EPRI TR-107330 for the EQ tests to be performed on the RadICS Platform

RG 1.152 recognizes the acceptability of EPRI TR-106439 for CGD. The RadICS Module EDs were treated as the "legacy software" described in Section 7.6 of EPRI TR-107330.

#### **4.1.2.1 EPRI TR-106439 Guidance**

EPRI TR-106439 was used to structure the CGD effort. Compliance with EPRI TR-106439 process was demonstrated using a checklist, which provides a mapping that shows where the elements of the dedication process are addressed in licensing documentation.

The RadICS Platform Commercial Grade Dedication Plans used a combination of three acceptance methods described in EPRI TR-106439 to verify the adequacy of the generic RadICS Platform:

- Method 1: Special Tests and Inspections of the RadICS Platform equipment

[[

]]<sup>a,c,f</sup>

- Method 2: Commercial Grade Survey of RadICS Modules [[  
]]<sup>a,c,f</sup>

Critical characteristics were based on three sets of U.S. benchmarks:

- The RadICS Module ED development process, which is based on IEC Standards, were evaluated for dependability critical characteristics developed from applicable NRC review guidance for safety system software development defined in NRC BTP 7-14 (Reference 4-35), IEEE Standard 7-4.3.2-2003, and other endorsed IEEE standards.

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- The RadICS Platform design characteristics were evaluated for performance and dependability critical characteristics developed from NUREG/CR-6082 (Reference 4-36, DI&C-ISG-04 (Reference 4-37), and IEEE Std 603-1991 (Reference 4-38).
- The RadICS Platform design characteristics were evaluated for selected physical critical characteristics developed from EPRI TR-107330.

[[

]]<sup>a,c,f</sup>

EPRI TR-106439 envisions the approach of using the historical development records as a basis for acceptance in a commercial grade dedication review. [[

]]<sup>a,c,f</sup>

- Method 3: Source Verification of the RadICS Platform manufacturing process.

The Source Verification was performed by witnessing quality activities of RPC Radiy (e.g., fabrication, assembly, special process and final inspection).

- Method 4: Acceptable Performance Record of the RadICS Platform

The review of the performance record was based on the RPC Radiy operating experience to demonstrate satisfactory performance with the RadICS Platform technology. Operating experience was not be used to compensate for shortcomings in legacy electronic design nor used as a basis for establishing RadICS Module failure rates.

#### **4.1.2.2 EPRI TR-107330 Guidance**

EPRI TR-107330 was used to define the qualification test methods (including the operability and prudence tests) and the critical characteristics to demonstrate acceptable performance during the qualification tests. Testing will demonstrate that the RadICS Platform functioned correctly during and/or after exposure to the series of stress tests outlined in EPRI TR-107330. The operability and prudence test acceptance criteria were important critical characteristics for performance in the CGD evaluation of the RadICS Platform.

#### **4.1.3 RadICS Commercial Grade Dedication Process**

The Radics LLC process for CGD is dedication is defined in a Radics LLC quality procedure (Reference 4-39), which requires the following:

- Writing a Dedication Plan that includes a detailed checklist with the acceptance activities to be performed to demonstrate compliance with EPRI TR-106439.
- Performing these activities and completing the checklist according to the approved Plan.
- Reporting the results in a Dedication Report.

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The RadICS Platform CGD Summary Reports contain the completed checklists and were issued after the completion of the qualification tests for the RadICS Platform equipment.

The RadICS Platform CGD Summary Reports define the qualification boundary of the RadICS Platform. The RadICS Platform can be used to implement safety-related I&C systems within the defined equipment qualification boundary defined in Chapter 9. It is also expected that I&C systems implemented with the RadICS Platform will address the project-specific actions items identified in the NRC safety evaluation report for the RadICS Platform Topical Report. Any safety-related system beyond that included in the baseline dedication will require additional evaluation for the new application boundary.

The RadICS Platform CGD Summary Reports are maintained as an auditable record for the RadICS Platform CGD effort, as required by 10 CFR 21.21(c)(2) (Reference 4-40).

#### **4.1.4 Maintenance of RadICS Platform Commercial Grade Dedication**

The RadICS Platform hardware and associated Module EDs has been qualified and is maintained under the Radics LLC 10 CFR Part 50 Appendix B quality program (Reference 4-41). If new boards are developed or existing boards modified for obsolescence or other reasons, the new or modified hardware will be appropriately tested and/or analyzed to maintain dedication and EQ to U.S. standards. Changes to the RadICS Platform are evaluated in accordance with the same process that formed the basis for the original CGD acceptance, as controlled by Radics LLC procedures.

All future modifications to the RadICS Platform will continue to be performed under the RPC Radiy QMS, as described in Chapter 3. The RadICS Platform dedication assessment will be updated to address future modifications to the platform.

Documentation supporting the commercial grade item dedication is maintained as a configuration item.

The RadICS Platform CGD maintenance controls satisfy the requirements of IEEE Std 7-4.3.2 Section 5.4.2.3.

## **4.2 Chapter 4 References**

- 1 RadICS Platform Commercial Grade Dedication Plan for LM, Radics LLC Document No. 2015-RTS001-CGDP\_LM-101
- 2 RadICS Platform Commercial Grade Dedication Plan for DIM, Radics LLC Document No. 2015-RTS001-CGDP\_DIM-003
- 3 RadICS Platform Commercial Grade Dedication Plan for DOM, Radics LLC Document No. 2015-RTS001-CGDP\_DOM-102
- 4 RadICS Platform Commercial Grade Dedication Plan for AIM, Radics LLC Document No. 2015-RTS001-CGDP\_AIM-103
- 5 RadICS Platform Commercial Grade Dedication Plan for AOM, Radics LLC Document No. 2015-RTS001-CGDP\_AOM-104
- 6 RadICS Platform Commercial Grade Dedication Plan for OCM, Radics LLC Document No. 2015-RTS001-CGDP\_OCM-106

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- 7 RadICS Platform Commercial Grade Dedication Plan for Chassis, Radics LLC Document No. 2015-RTS001-CGDP\_CH-107
- 8 RadICS Platform Commercial Grade Dedication Plan for I/O Connections Protection Module, Radics LLC Document No. 2015-RTS001-CGDP\_IOPM-131
- 9 RadICS Platform Commercial Grade Dedication Plan for Ventilation Module, Radics LLC Document No. 2015-RTS001-CGDP\_VM-132
- 10 RadICS Platform Commercial Grade Dedication Plan for TIM, Radics LLC Document No. 2019-SRTS003-CGDP\_TIM-150
- 11 RadICS Platform Commercial Grade Dedication Plan for RIM, Radics LLC Document No. 2019-SRTS003-CGDP\_RIM-151
- 12 RadICS Platform Commercial Grade Dedication Plan for WAIM, Radics LLC Document No. 2019-SRTS003-CGDP\_WAIM-152
- 13 RadICS Platform Commercial Grade Dedication Plan for Cables, Radics LLC Document No. 2019-SRTS003-CGDP\_Cb-154
- 14 Commercial Grade Dedication Summary Report for LM, Radics LLC Document No. 2017-RTS001-CGDSR\_LM-371
- 15 Commercial Grade Dedication Summary Report for AIM, Radics LLC Document No. 2017-RTS001-CGDSR\_AIM-372
- 16 Commercial Grade Dedication Summary Report for AOM, Radics LLC Document No. 2017-RTS001-CGDSR\_AOM-370
- 17 Commercial Grade Dedication Summary Report for DIM, Radics LLC Document No. 2017-RTS001-CGDSR\_DIM-373
- 18 Commercial Grade Dedication Summary Report for DOM, Radics LLC Document No. 2017-RTS001-CGDSR\_DOM-374
- 19 Commercial Grade Dedication Summary Report for OCM, Radics LLC Document No. 2017-RTS001-CGDSR\_OCM-375
- 20 Commercial Grade Dedication Summary Report for IOPM, Radics LLC Document No. 2017-RTS001-CGDSR\_IOPM-376
- 21 Commercial Grade Dedication Summary Report for Chassis, Radics LLC Document No. 2017-RTS001-CGDSR\_CH-377
- 22 Commercial Grade Dedication Summary Report for VM, Radics LLC Document No. 2017-RTS001-CGDSR\_VM-378
- 23 Commercial Grade Dedication Summary Report for TIM, Radics LLC Document No. 2019-SRTS003-CGDP-TIM-156
- 24 Commercial Grade Dedication Summary Report for RIM, Radics LLC Document No. 2019-SRTS003-CGDP-RIM-157
- 25 Commercial Grade Dedication Summary Report for WAIM, Radics LLC Document No. 2019-SRTS003-CGDP-WAIM-158
- 26 Commercial Grade Dedication Summary Report for Cables, Radics LLC Document No. 2019-SRTS003-CGDP-Cb-159
- 27 EPRI NP-5652, "Guideline for the Utilization of Commercial Grade Items in Nuclear Safety Related Applications (NCIG-07)," July 1988

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- 28 Generic Letter 89-02, "Actions to Improve the Detection of Counterfeit and Fraudulently Marketed Products"
- 29 EPRI TR-106439, "Guideline on Evaluation and Acceptance of Commercial Grade Digital Equipment for Nuclear Safety Applications, Electric Power Research Institute, October 1996
- 30 Letter from NRC to EPRI dated July 17, 1997, "Review of EPRI Topical Report TR-106439, 'Guideline on Evaluation and Acceptance of Commercial Grade Digital Equipment for Nuclear Safety Applications'"
- 31 Regulatory Guide 1.152, Revision 3, "Criteria for Use of Computers in Safety Systems of Nuclear Power Plants"
- 32 IEEE Std 7-4.3.2-2003, "Standard Criteria for Digital Computers in Safety Systems of Nuclear Power Generating Stations"
- 33 10 CFR Part 50 Appendix B, "Quality Assurances Requirements for Nuclear Power Plants and Fuel Reprocessing Plants"
- 34 EPRI TR-107330, "Generic Requirements Specification for Qualifying a Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants," Electric Power Research Institute, December 1996
- 35 NUREG-0800, Chapter 7, NRC Branch Technical Position 7-14, Revision 5, "Guidance on Software Reviews for Digital Computer Based Instrumentation and Control Systems," U.S. Nuclear Regulatory Commission, March 2007
- 36 NUREG/CR 6082, "Data Communications," August 1993
- 37 DI&C-ISG-04, Revision 1, "Highly Integrated Control Rooms - Digital Communication Systems"
- 38 IEEE Std 603-1991, "Criteria for Safety Systems for Nuclear Power Generating Stations"
- 39 Radics LLC Procedure QP 07-3, "Commercial Grade Dedication Procedure"
- 40 10 CFR 21.21, "Notification of failure to comply or existence of a defect and its evaluation"
- 41 QAPD-001, "Radics LLC Quality Assurance Program Description"



## 5 Regulations, Codes, and Standards

### 5.1 Compliance Summary

A summary of NRC regulatory requirements and acceptance criteria for I&C systems important to safety is found in Standard Review Plan (SRP) Table 7-1 (Reference 5-1). Radics LLC reviewed this table and other sources to define the scope of the regulatory requirements and acceptance criteria that applied to the generic RadICS Platform. Several of the items listed in SRP Table 7-1 apply to project-specific safety I&C systems. Compliance with project-specific regulatory requirements cannot be assessed in the context of a generic digital safety I&C platform that does not include the specific applications. The results of the screening performed by Radics LLC are documented in this Chapter.

### 5.2 10 CFR, Code of Federal Regulations

The following regulations were assessed for applicability to the RadICS Platform design.

#### 5.2.1 10 CFR 50.34(f)(2)(v), Bypass and Operable Status Indication

Project-specific applications of the RadICS Platform will comply with the requirement of 10 CFR 50.34(f)(2)(v), *Bypass and Operable Status Indication*, to provide automatic indication of the bypassed and operable status of safety systems. The generic RadICS Platform supports indications in the main control room and hardwired discrete outputs can be provided, as described in Chapter 6. The specific means for complying with 10 CFR 50.34(f)(2)(v) must be assessed on a project-specific basis.

#### 5.2.2 10 CFR 50.49, Environmental Qualification

10 CFR 50.49, *Environmental Qualification of Electric Equipment Important to Safety for Nuclear Power Plants*, identifies specific requirements for qualification of electric equipment important to safety. RG 1.89 describes methods acceptable to the NRC for complying with 10 CFR 50.49. RadICS Platform equipment will not be installed in harsh environments. The qualification of the RadICS Platform for mild environments is described in Chapter 9.

#### 5.2.3 10 CFR 50.55a(h)(2), Protection Systems

As required in 10 CFR 50.55a(h), *Protection Systems*, the RadICS Platform complies with IEEE Std 603-1991. Compliance with applicable portions of IEEE Std 603-1991 for the RadICS Platform is addressed in Chapter 12. The specific means for complying with 10 CFR 50.55a(h)(2) on a system level must be assessed on a project-specific basis.

#### 5.2.4 10 CFR Part 50 Appendix A, General Design Criteria

The applicable General Design Criteria (GDC) from 10 CFR Part 50 Appendix A are discussed below.

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#### **5.2.4.1 General Design Criterion 1, Quality Standards, and Records**

The basic requirement is that structures, systems, and components shall be designed, fabricated, erected, constructed, tested, and inspected to quality standards commensurate with the importance of the safety function to be performed. The generic RadICS Platform is intended for use in Class 1E safety I&C applications.

The Radics LLC quality assurance program that governs all RadICS activities is compliant with 10 CFR Part 50 Appendix B and ASME NQA-1-2008 and the NQA-1a-2009 Addenda, as described in Chapter 3. The alignment of the Radics LLC QAPD to GDC 1 is described in Chapter 12.

#### **5.2.4.2 GDC 2, Design Bases for Protection Against Natural Phenomena**

The basic requirement is that structures, systems, and components important to safety shall be designed to withstand the effects of a range of natural phenomena without loss of capability to perform their safety functions. The RadICS Platform is intended for use in Class 1E safety I&C applications. The generic qualification program for RadICS Platform that would support compliance with GDC 2 for a specific project is described in Chapter 9. The licensee for a project-specific application of the RadICS Platform will address the correspondence of the generic qualification envelope for the RadICS Platform with the site-specific qualification bounding envelopes.

#### **5.2.4.3 GDC 4, Environmental and Dynamic Effects Design Bases**

The basic requirement is that structures, systems, and components important to safety shall be designed to accommodate the effects of and to be compatible with the environmental conditions associated with normal operation, maintenance, testing, and postulated accidents, including loss-of-coolant accidents. The generic qualification program for RadICS Platform that would support compliance with GDC 4 for a specific project is described in Chapter 9. The licensee for a project-specific application of the RadICS Platform will address the correspondence of the generic qualification envelope for the RadICS Platform with the site-specific qualification bounding envelopes.

#### **5.2.4.4 GDC 13, Instrumentation and Control**

The RadICS Platform standard input boards enable the design of systems using the RadICS Platform technology that can monitor a wide range of variables and systems over their anticipated ranges for normal operation, for anticipated operational occurrences, and for accident conditions as appropriate to assure adequate safety. The RadICS Platform features that would support compliance with GDC 13 for a specific project are described in Chapter 6. The specific means for complying with GDC 13 must be assessed on a project-specific basis.

#### **5.2.4.5 GDC 20, Protection System Functions**

The RadICS Platform features that would support compliance with GDC 20 for a specific project are described in Chapter 6. The standard RadICS Platform hardware described in Chapter 6, the hardware development process described in Chapter 7, and the development life cycle processes for RadICS Platform Electronic Designs (EDs) described in Chapters 7 and 8 are the foundations for designing and

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implementing project-specific safety I&C systems that accomplish the GDC 20 safety functions. The specific means for complying with GDC 20 must be assessed on a project-specific basis.

#### **5.2.4.6 GDC 21, Protection Systems Reliability and Testability**

The RadICS Platform features that would support compliance with GDC 21 for a specific project are described in Chapter 6. The RadICS Platform is designed for high functional reliability. A summary of the board/device-level hardware reliability is provided in Chapter 9. The RadICS Platform ED logic is designed to be highly reliable. The RadICS Platform ED life cycle processes are described in Chapters 7 and 8 have been assessed as part of the Functional Safety Assessments performed by *exida* that demonstrated that the RadICS Platform complies with the IEC 61508 SIL 3 certification requirements (Reference 5-2). The RadICS Platform Application ED development life cycle process is described in Chapter 7. The in-service testing and periodic testing features of the RadICS Platform are described in Chapter 6. The standard RadICS Module hardware and associated Platform ED described in Chapter 6 can be readily employed in system architectures with redundant and independent divisions that comply with the single failure criterion. The specific means for complying with GDC 21 must be assessed on a project-specific basis.

#### **5.2.4.7 GDC 22, Protection System Independence**

The RadICS Platform features that would support compliance with GDC 22 for a specific project are described in Chapter 6. RadICS Platform-based systems have the requisite independence of divisions to ensure that a fault in one independent division does not propagate and affect other redundant divisions. Representative RadICS Platform single division and four division architectures are described in Chapter 2. RadICS Platform interdivisional (i.e., coincidence voting) communications also comply with NRC DI&C-ISG-04 recommendations, as described in Appendix B.

The RadICS Platform has the requisite independence to ensure that a postulated fault in a connected non-safety I&C system does not propagate and affect the safety I&C system. As described in Chapter 6, this is accomplished by a one-way (broadcast only) communication link from the safety I&C system to the non-safety I&C system. In addition, RadICS Platform outputs can be connected to non-Class 1E systems. The Class 1E / non-Class 1E isolation capability of these outputs is verified through qualification testing, which is described in Chapter 9.

RadICS Platform hardware is qualified for a mild operating environment, with a generic qualification envelope as described in Chapter 9. Operation within this envelope will not result in loss of the protection function.

The in-service testing and periodic testing features of the RadICS Platform are described in Chapter 6. With appropriate redundancy in an actual system, maintenance and testing activities will not result in loss of the protection function.

D3 should be addressed in the context of a suite of safety and non-safety I&C systems at a NPP. The RadICS Platform can be used to employ signal diversity, as described in Chapter 6.

The design and implementation of RadICS Platform digital communications described in Chapter 6 enables independence to be maintained between redundant divisions and between the safety I&C

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system and non-safety I&C systems. The interdivisional communications provisions that address the guidance in DI&C-ISG-04 are described in Appendix B.

The specific means for complying with GDC 22 must be assessed on a project-specific basis. D3 will be addressed in the context of the project-specific suite of safety and non-safety I&C systems.

#### **5.2.4.8 GDC 23, Protection System Failure Modes**

The RadICS Platform features that would support compliance with GDC 23 for a specific project are described in Chapter 6. Modes of operation of the RadICS Platform are described in Chapter 6, which also explains the behavior of the RadICS Platform when failures are detected. As discussed in Chapter 9, board-level failure mode and effects analyses (FMEAs) are documented in a separate report. The specific means for complying with GDC 23 must be assessed on a project-specific basis.

#### **5.2.4.9 GDC 24, Separation of Protection and Control Systems**

The RadICS Platform features that would support compliance with GDC 24 for a specific project are described in Chapter 6. The design and implementation of RadICS Platform digital communications described in Chapter 6 enables separation to be maintained between the safety I&C system and non-safety I&C systems. These communications provisions that address the guidance in DI&C-ISG-04 are as described in Appendix B. The specific means for complying with GDC 24 must be assessed on a project-specific basis.

#### **5.2.4.10 GDC 25, Protection System Requirements for Reactivity Control Malfunctions**

The RadICS Platform features that would support compliance with GDC 25 for a specific project are described in Chapter 6. The specific means for complying with GDC 25 must be assessed on a project-specific basis.

#### **5.2.4.11 GDC 29, Protection Against Anticipated Operational Occurrences**

The RadICS Platform features that would support compliance with GDC 29 for a specific project are described in Chapter 6. The RadICS Platform is designed for high functional reliability. A summary of the board/device-level hardware reliability is provided in Chapter 9. Operating experience with RPC Radiy systems described in Chapter 2 has shown no instances where the RPC Radiy systems have experienced any system failures or common cause failures that affected the capability of the safety I&C system to perform its intended safety function(s) during an anticipated operational occurrence. The specific means for complying with GDC 29 must be assessed on a project-specific basis. Specifically, the RPC Radiy systems have not experienced any system failures or common cause failures in more than 400 reactor-years of operation as of December 2015.

### **5.2.5 10 CFR Part 50 Appendix B, Quality Assurance Requirements**

The Radics LLC QAPD that governs all Radics LLC activities are compliant with 10 CFR Part 50 Appendix B, Quality Assurance Requirements for Nuclear Power Plants and Fuel Reprocessing Plants, and ASME

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NQA-1-2008 and the NQA-1a-2009 Addenda, as described in Chapter 3. The alignment of the Radics LLC QAPD to 10 CFR Part 50 Appendix B is described in Chapter 12.

### 5.3 NRC Regulatory Guides

The following NRC RGs were assessed for applicability to the RadICS Platform design.

#### 5.3.1 Regulatory Guide 1.22

The RadICS Platform features that would support compliance with RG 1.22, *Periodic Testing of Protection System Actuation Functions*, for a specific project are described in Chapter 6. The specific means for complying with RG 1.22 must be assessed on a project-specific basis.

#### 5.3.2 Regulatory Guide 1.28

RG 1.28, Revision 4, *Quality Assurance Program Criteria (Design and Construction)*, endorses Part I and Part II requirements included in NQA-1-2008 and the NQA-1a-2009 Addenda for the implementation of a quality assurance program during the design and construction phases of NPPs and fuel reprocessing as an acceptable method for complying with the requirements of Appendix B to 10 CFR Part 50, subject to the specified additions and modifications. The Radics LLC QAPD that governs all Radics LLC activities are compliant with 10 CFR Part 50 Appendix B and ASME NQA-1-2008 and the NQA-1a-2009 Addenda, as described in Chapter 3. The alignment of the Radics LLC QAPD to RG 1.28 is described in Chapter 12.

#### 5.3.3 Regulatory Guide 1.47

The RadICS Platform features that would support compliance with RG 1.47, Revision 1, *Bypassed and Inoperable Status Indication for Nuclear Power Plant Safety System*, for a specific project are described in Chapter 6. RG 1.47 provides supplemental guidance for implementing IEEE Std 603-1991 to satisfy the NRC regulatory requirements with respect to the bypassed and inoperable status indication for NPP safety systems. Project-specific applications of the RadICS Platform will comply with the requirement to provide automatic indication of the bypass or inoperable status of portions of the protection system. In project-specific applications, compliance with RG 1.47 requires further determinations that bypass or inoperable status is also provided for the following:

- Systems actuated or controlled by the protection system
- Auxiliary or supporting systems that must be operable for the protection system and the systems it actuates to perform their safety functions.

The specific means for complying with RG 1.47 must be assessed on a project-specific basis.

#### 5.3.4 Regulatory Guide 1.53

RG 1.53, Revision 2, *Application of the Single-Failure Criterion to Safety Systems*, endorses IEEE Std 379-2000 with qualifications. The standard RadICS Platform hardware described in Chapter 6 can be implemented in system architectures with redundant and independent channels, divisions, and trains that comply with the single failure criterion. Representative RadICS Platform system architectures are

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described in Chapter 2. The specific means for complying with RG 1.53 must be assessed on a project-specific basis.

### 5.3.5 Regulatory Guide 1.62

The RadICS Platform features that would support compliance with RG 1.62, Revision 1, *Manual Initiation of Protection Actions*, for a specific project are described in Chapter 6. The specific means for complying with RG 1.62 must be assessed on a project-specific basis.

### 5.3.6 Regulatory Guide 1.75

RG 1.75, Revision 3, *Criteria for Independence of Electrical Safety Systems*, endorses IEEE Std 384-1992 with qualifications. The standard RadICS Platform hardware described in Chapter 6 is designed to establish and maintain the independence of safety-related equipment, circuits, and auxiliary supporting features by physical separation and electrical isolation. In a project-specific application, this is accomplished by physically separating the redundant divisions of the safety system.

Representative RadICS Platform system architectures are described in Chapter 2. These typical architectures include the interdivisional communication interfaces that are needed to support voting logic. As described in Chapter 6, interdivisional communication is accomplished using fiber optic links that maintain the electrical isolation between divisions and RadICS Logic Module features that maintain the required logical data isolation between divisions.

Electrical independence between Class 1E and non-Class 1E digital systems also is established by means of fiber optic links. As described in Chapter 6, data isolation is assured by implementing logical data isolation in the Class 1E systems as well as providing only one-way (broadcast only) communication links from the Class 1E system to the non-Class 1E system.

The alignment of the RadICS Platform to RG 1.75, Revision 3, is described in Chapter 12. The specific means for complying with the system level independence requirements in RG 1.75 must be assessed on a project-specific basis.

### 5.3.7 Regulatory Guide 1.89

RG 1.89, Revision 1, *Environmental Qualification of Certain Electric Equipment Important to Safety for Nuclear Power Plants*, describes methods acceptable to the NRC for complying with 10 CFR 50.49 for qualification of electric equipment important to safety for service in NPPs. These methods ensure the equipment can perform its safety function during and after a design basis accident. This RG endorses IEEE Std 323-1974. Platform equipment will not be installed in harsh environments. The qualification of the RadICS Platform for mild environments is described in Chapter 9.

### 5.3.8 Regulatory Guide 1.100

RG 1.100, Revision 3, *Seismic Qualification of Electric and Mechanical Equipment for Nuclear Power Plants*, endorses IEEE Std 344-2004. Chapter 9 describes the seismic qualification testing of the RadICS Platform and the use of RG 1.100, Revision 3, and EPRI TR-107330 (EPRI website version) in the seismic

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qualification test plan. The alignment of the RadICS Platform to RG 1.100, Revision 3, is described in Chapter 12. The licensee for a project-specific application of the RadICS Platform will address the correspondence of the generic qualification envelope for the RadICS Platform with the site-specific qualification bounding envelopes.

### 5.3.9 Regulatory Guide 1.105

RG 1.105, Revision 3, *Setpoints for Safety-Related Instrumentation*, endorses Instrument Society of America (ISA) Standard ISA-S67.04-1994 with qualifications.

As described in Section 5.2.3, EPRI TR-107330, Section 4.2.4 requires the qualifier to provide information about the qualified hardware to support an application specific setpoint analysis per ISA-S67.04-1994. Chapter 9 describes the approach Radics LLC used for preparing the setpoint analysis support documentation for the RadICS Platform. This documentation provides sufficient design specification data for a setpoint analysis to be performed on a project-specific RadICS Platform-based system. The specific means for complying with RG 1.105 must be assessed on a project-specific basis.

### 5.3.10 Regulatory Guide 1.118

RG 1.118, Revision 3, *Periodic Testing of Electric Power and Protection Systems*, endorses IEEE Std 338-1987 with qualifications. As provided in IEEE Std 338, automatic testing provisions for programmable digital computer-based systems are subject to the testing provisions of this standard and IEEE Std 7-4.3.2-2003. The RadICS Platform features that would support compliance with RG 1.118 for a specific project are described in Chapter 6. The specific means for complying with RG 1.118 must be assessed on a project-specific basis.

### 5.3.11 Regulatory Guide 1.152

RG 1.152, Revision 3, *Criteria for Use of Computers in Safety Systems of Nuclear Power Plants*, endorses IEEE Std 7-4.3.2-2003 with qualifications. Compliance of the RadICS Platform EDs with IEEE Std 7-4.3.2-2003 is described in Chapter 12.

The RadICS Platform ED life cycle processes applied by RPC Radiy and Radics LLC provide protection against unauthorized, unintended, and unsafe modifications to the EDs, thereby promoting integrity and reliability during operation and maintenance.

As described in Chapter 6, the generic RadICS Platform has been designed as the foundation for project-specific digital safety I&C systems that will implement nuclear safety functions. The design of the generic RadICS Modules and associated Platform ED life cycle processes applied through the factory test phase also accomplish computer security functions by: (a) providing inherent protection against unauthorized, unintended, and unsafe modifications to the system, and (b) implementing design requirements that promote integrity and reliability during operation and maintenance in the event of inadvertent operator actions or undesirable behavior of connected equipment.

The secure development and operating environment for the RadICS Platform is described in Chapter 11.

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RG 1.152 Annex C identifies that EPRI TR-106439 contains adequate guidance for the evaluation and acceptance of commercial grade digital equipment for nuclear safety applications. The CGD program for the RadICS Platform is described in Chapter 4.

Compliance with RG 1.152 for the RadICS Platform is described in Chapter 12. The specific means for complying with the application of RG 1.152 on a system level must be assessed on a project-specific basis.

### **5.3.12 Regulatory Guide 1.153**

RG 1.153, Revision 1, *Criteria for Safety Systems*, endorses IEEE Std 603-1991 and the correction sheet of January 30, 1995. The RadICS Platform features that would support compliance with RG 1.153 for a specific project are described in Chapter 12.

### **5.3.13 Regulatory Guide 1.168**

RG 1.168, Revision 2, *Verification, Validation, Reviews and Audits for Digital Computer Software Used in Safety Systems of Nuclear Power Plants*, endorses IEEE Std 1012-2004 and IEEE Std 1028-2008. IEEE Std 828-2005 describes a structured approach to software V&V. IEEE Std 1028-2008 described methods to perform software reviews and audits. The RPC Radiy and Radics LLC approaches to electronic design V&V are described in Chapters 7 and 8. The RPC Radiy and Radics LLC approaches to electronic design V&V is described in Chapters 7 and 8. The Radics LLC approach to electronic design reviews is described in Section 7.4.3. The RPC Radiy and Radics LLC approaches to electronic design audits are described in Sections 7.3.1, 7.5.3.3, and 11.4. The alignment of the RPC Radiy and Radics LLC configuration management programs to RG 1.168, Revision 2, is described in Chapter 12.

### **5.3.14 Regulatory Guide 1.169**

RG 1.169, Revision 1, *Configuration Management Plans for Digital Computer Software Used in Safety Systems of Nuclear Power Plants*, endorses IEEE Std 828-2005. IEEE Std 828-2005 describes a structured approach to software configuration management. The RPC Radiy and Radics LLC approaches to electronic design configuration management are described in Section 7.5. The alignment of the RPC Radiy and Radics LLC configuration management programs to RG 1.169, Revision 1, is described in Chapter 12.

### **5.3.15 Regulatory Guide 1.170**

RG 1.170, Revision 1, *Software Test Documentation for Digital Computer Software Used in Safety Systems of Nuclear Power Plants*, endorses IEEE Std 829-2008. IEEE Std 829-2008 describes a structured approach to software test documentation. Section 7.5.4.2 describes the RPC Radiy and Radics LLC approaches to Platform and Application ED V&V test documentation. The alignment of RPC Radiy and Radics LLC electronic design test documentation to RG 1.170, Revision 1, is described in Chapter 12.



### 5.3.16 Regulatory Guide 1.171

RG 1.171, Revision 1, *Software Unit Testing for Digital Computer Software Used in Safety Systems of Nuclear Power Plants*, endorses IEEE Std 1008-1987. IEEE Std 1008-1987 describes a structured approach for performing software unit testing. RadICS Platform electronic design testing is described in Chapters 7 and 8. The alignment of Radics LLC electronic design testing to RG 1.171, Revision 1, is described in Chapter 12.

### 5.3.17 Regulatory Guide 1.172

RG 1.172, Revision 1, *Software Requirements Specifications for Digital Computer Software Used in Safety Systems of Nuclear Power Plants*, endorses IEEE Std 830-1998. IEEE Std 830-1998 is a recommended practice for writing software requirements specifications; however, as a recommended practice, it does not identify any specific requirements. The RadICS Platform and Application requirements documents are described in Chapter 7. The alignment of the RPC Radiy and Radics LLC electronic design requirements specifications to RG 1.172, Revision 1, is described in Section 12.

### 5.3.18 Regulatory Guide 1.173

RG 1.173, Revision 1, *Developing Software Life Cycle Processes for Digital Computer Software Used in Safety Systems of Nuclear Power Plants*, endorses IEEE Std 1074-2006, which provides a structured approach for developing a software life cycle program. The life cycle processes for the RadICS Platform and Application ED are described in Chapters 7 and 8. The alignment of the RadICS Platform and Application ED lifecycles to RG 1.173, Revision 1, is described in Chapter 12.

### 5.3.19 Regulatory Guide 1.180

RG 1.180, Revision 1, *Guidelines for Evaluating Electromagnetic and Radio-Frequency Interference in Safety-Related Instrumentation and Control Systems*, endorses IEC 61000, Military Standard (MIL-STD)-461E, IEEE Std 1050-1996, IEEE Std C62.41-1991, and IEEE Std C62.45-1992 with qualifications. Chapter 9 describes the use of RG 1.180, Revision 1, in the electromagnetic and radio-frequency interference qualification test plan. The alignment of the RadICS Platform to RG 1.180, Revision 1, is described in Chapter 12. The licensee for a project-specific application of the RadICS Platform will address the correspondence of the generic qualification envelope for the RadICS Platform with the site-specific qualification bounding envelopes.

### 5.3.20 Regulatory Guide 1.209

RG 1.209, *Guidelines for Environmental Qualification of Safety-Related Computer-Based Instrumentation and Control Systems in Nuclear Power Plants*, endorses IEEE Std 323-2003 with qualifications. Chapter 9 describes the use of RG 1.209 in the RadICS Platform EQ program. The RG also notes that NRC has approved EPRI TR-107330 as an acceptable method for addressing mild-environment qualification of programmable logic controllers (PLCs) that is considered equivalent to and consistent with RG 1.209. The alignment of the RadICS Platform to RG 1.209 is described in Chapter 12. The licensee for a project-

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specific application of the RadICS Platform will address the correspondence of the generic qualification envelope for the RadICS Platform with the site-specific qualification bounding envelopes.

## **5.4 NUREG-0800, Chapter 7, Branch Technical Positions**

The following NRC Branch Technical Positions (BTPs) were assessed for applicability to the RadICS Platform design.

### **5.4.1 Branch Technical Position 7-8**

BTP 7-8, Revision 5, *Guidance on Application of Regulatory Guide 1.22*, provides additional review guidance regarding the use of RG 1.22 for digital systems. The RadICS Platform periodic testing features that would support compliance with BTP 7-8 for a specific project are described in Chapter 6.

### **5.4.2 Branch Technical Position 7-11**

BTP 7-11, Revision 5, *Guidance on Application and Qualification of Isolation Devices*, provides additional review guidance regarding the use of RG 1.75 for I&C systems. As described in Chapter 6, the RadICS Platform uses the following types of qualified isolation devices: Module features described in Section 6.6 and fiber optic cables. Electrical isolation testing is described in Chapter 9. The alignment of the RadICS Platform to the review guidance in BTP 7-11 is described in Chapter 12.

### **5.4.3 Branch Technical Position 7-12**

BTP 7-12, Revision 5, *Guidance on Establishing and Maintaining Instrument Setpoints*, provides additional review guidance regarding the use of RG 1.105 for I&C systems. EPRI TR-107330, Section 4.2.4 requires the qualifier to provide information about the qualified hardware to support an application specific setpoint analysis per ISA-S67.04-1994. Chapter 9 describes how Radics LLC, as both vendor and qualifier, applied this approach and prepared a setpoint analysis support document for the generic RadICS Platform. This documentation is intended to provide sufficient design specification data for a project-specific setpoint analysis to be performed. Compliance of actual system setpoints with BTP 7-12 will be addressed by the licensee on a project-specific basis.

### **5.4.4 Branch Technical Position 7-14**

BTP 7-14, Revision 6, *Guidance on Software Reviews for Digital Computer-Based Instrumentation and Control Systems*, provides a structured approach for developing software using a series of plans. The alignment of the RadICS Platform and Application ED documents to BTP 7-14 is described in Chapter 12.

### **5.4.5 Branch Technical Position 7-17**

BTP 7-17, Revision 6, *Guidance on Self-Test and Surveillance Test Provisions*, provides additional review guidance regarding the use of RGs 1.22, 1.118, and 1.152 for digital I&C systems. The RadICS Platform self-diagnostic test and surveillance test provisions are described in Chapter 6. The alignment of the RadICS Platform to the review guidance in BTP 7-17 is described in Chapter 12. The use of RadICS

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Platform automatic test features as credit for performing Technical Specification surveillance test functions must be assessed on a project-specific basis.

#### **5.4.6 Branch Technical Position 7-18**

BTP 7-18, Revision 5, *Guidance on the Use of Programmable Logic Controllers in Digital Computer-Based Instrumentation and Control Systems*, provides additional review guidance regarding the use of RG 1.152 for the CGD of digital I&C systems. The alignment of the RadICS Platform to the review guidance in BTP 7-18 is described in Chapter 12.

#### **5.4.7 Branch Technical Position 7-19**

BTP 7-19, Revision 6, *Guidance on Evaluation of Diversity and Defense-in-Depth in Digital Computer-Based Instrumentation and Control Systems*, provides guidance for the evaluation of D3 analyses performed on safety-related I&C systems to assess vulnerabilities to digital common cause failures. The RadICS Platform diversity solution described in Chapter 10 provides an acceptable regulatory solution for the digital CCF vulnerabilities present in the RadICS Platform. NRC BTP 7-19, Revision 6, states that there are two design attributes, either of which is sufficient to eliminate consideration of software based or software logic based CCF: diversity or testability. With respect to the diversity option, BTP 7-19 specifies that when sufficient diversity exists in the PS, then the potential for CCF within the channels can be considered to be appropriately addressed without further action.

The RadICS Platform features that would support compliance with BTP 7-19 for a specific project are described in Chapter 10. The D3 assessment for an actual system will be addressed by the licensee on a project-specific basis.

#### **5.4.8 Branch Technical Position 7-21**

BTP 7-21, Revision 5, *Guidance on Digital Computer Real-Time Performance*, provides review guidance to verify that system timing requirements calculated from the design basis events and other criteria have been allocated to the digital computer portion of the system as appropriate, and have been satisfied in the digital system design and implementation. Chapter 6 describes how the RadICS Platform addresses the review guidance in BTP 7-21. The alignment of the RadICS Platform to the review guidance in BTP 7-21 is described in Chapter 12.

### **5.5 NRC NUREGs and NUREG/CRs**

The following NRC NUREG document was assessed for applicability to the RadICS Platform design.

#### **5.5.1 NUREG/CR 6082, Data Communications**

Section 2 of NUREG/CR-6082, *Data Communications*, has 15 questions intended to help focus reviews of data communication systems. An evaluation the RadICS Platform for those questions is provided in Chapter 12.

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## **5.6 NRC Digital I&C Interim Staff Guidance Documents**

The following NRC DI&C-ISG documents were assessed for applicability to the RadICS Platform design.

### **5.6.1 DI&C-ISG-04**

DI&C-ISG-04, Revision 1, *Highly Integrated Control Rooms - Digital Communication Systems*, provides criteria for the evaluation of communication independence features used for interdivisional communication. An evaluation of the RadICS Platform for the DI&C-ISG-04 communication independence criteria is provided in Chapter 12. Alignment with the DI&C-ISG-04 guidance for RadICS Platform communication features is described in Appendix B.

### **5.6.2 DI&C-ISG-06**

The documents submitted by Radics LLC for the NRC generic review of the RadICS Platform are consistent with the guidance in DI&C-ISG-06, Revision 1, *Licensing Process*, which lists the documents expected for a project-specific review. Many of the listed documents do not apply to the generic Tier 3 review of a digital safety I&C platform. Alignment with the DI&C-ISG-06 guidance for supporting documents is described in Appendix C.

## **5.7 Institute of Electrical & Electronics Engineers Standards**

The following IEEE standards were assessed for applicability to the RadICS Platform design.

### **5.7.1 IEEE Std 7-4.3.2-2003**

IEEE Std 7-4.3.2-2003, *Standard Criteria for Digital Computers in Safety Systems of Nuclear Power Generating Stations*, is endorsed by RG 1.152 except for Annexes B to F. Conformance with the requirements of IEEE Std 7-4.3.2-2003 is a method that the NRC staff has deemed acceptable for satisfying the NRC's regulations with respect to high functional reliability and design requirements for computers used in the safety systems of NPPs. The alignment of the RadICS Platform and Application ED development processes to IEEE Std 7-4.3.2-2003 is described in Chapter 12.

### **5.7.2 IEEE Std 323-2003**

IEEE Std 323-2003, *IEEE Standard for Qualifying Class 1E Equipment for Nuclear Power Generating Stations*, is endorsed by RG 1.209 with qualifications. An earlier version, IEEE Std 323-1974 is endorsed by RG 1.89. Chapter 9 described the use of IEEE Std 323-2003 for environmental qualification testing of the RadICS Platform. The alignment of the RadICS Platform to IEEE Std 323-2003 is described in Chapter 12. The licensee for a project-specific application of the RadICS Platform will address the correspondence of the generic qualification envelope for the RadICS Platform with the site-specific qualification bounding envelopes.

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### 5.7.3 IEEE Std 338-1987

IEEE Std 338-1987, *Criteria for the Periodic Surveillance Testing of Nuclear Power Generating Station Safety Systems*, is endorsed by RG 1.118 with qualifications. Chapter 6 provides the coverage of self-diagnostic tests and periodic surveillance testing provisions of the RadICS Platform that can be used to comply with IEEE Std 338-1987. The specific means for complying with IEEE Std 338-1987 must be assessed on a project-specific basis.

### 5.7.4 IEEE Std 344-2004

IEEE Std 344-2004, *IEEE Recommended Practice for Seismic Qualification of Class 1E Equipment for Nuclear Power Generating Stations*, is endorsed by RG 1.100 with qualifications. Chapter 9 described the use of IEEE Std 344-2004 for RadICS Platform seismic qualification testing of RadICS Platform. The alignment of the RadICS Platform seismic qualification testing to IEEE Std 344-2004 is described in Chapter 12.

### 5.7.5 IEEE Std 352-1987

Chapter 9 describes the use of IEEE Std 352-1987, *Guide for General Principles of Reliability Analysis of Nuclear Power Generating Station Safety Systems*, for the generic board/module-level FMEAs.

### 5.7.6 IEEE Std 379-2000

IEEE Std 379-2000, *Application of the Single-Failure Criterion to Nuclear Power Generating Station Safety Systems*, is endorsed by RG 1.53 with qualifications. The standard RadICS Modules components described in Chapter 6 can be implemented in redundant and independent system architectures that comply with the single failure criterion. Representative RadICS Platform system architectures are described in Chapter 2. The specific means for complying with IEEE Std 379-2000 must be assessed on a project-specific basis.

### 5.7.7 IEEE Std 384-1992

IEEE Std 384-1992, *Standard Criteria for Independence of Class 1E Equipment and Circuits*, is endorsed by RG 1.75 with qualifications. The standard RadICS Platform hardware components and associated EDs described in Chapter 6 are designed for establishing and maintaining the independence of safety-related equipment and circuits, and auxiliary supporting features by physical separation and electrical isolation. In a project-specific application, this is accomplished by physically separating the redundant channels, divisions, and trains of the safety system.

Example RadICS Platform system architectures are described in Chapter 2. These typical architectures include the interdivisional communication interfaces that are needed to support voting logics. Communications between redundant divisions and trains are isolated and designed to retain the required independence. Interdivisional communication is accomplished using fiber optic data links that maintain the electrical isolation between divisions.

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The typical RadICS Platform system architectures described in Chapter 2 also include Class 1E to non-Class 1E communications interfaces. Electrical isolation between the Class 1E system and the non-Class 1E system is accomplished using fiber optic data links and one-way (broadcast only) communications from the Class 1E system to the non-Class 1E system.

The alignment of the RadICS Platform to IEEE 384-1992 is described in Chapter 12.

The specific means for complying with the system level independence requirements in IEEE 384-1992 must be assessed on a project-specific basis.

### **5.7.8 IEEE Std 603-1991**

IEEE Std 603-1991, *Criteria for Safety Systems for Nuclear Power Generating Stations*, with the January 30, 1995 correction sheet, is incorporated by reference in 10 CFR 50.55a(h) and endorsed by RG 1.153. Project-specific RadICS Platform-based systems can be configured from the generic RadICS Modules to comply with IEEE Std 603-1991. The RadICS Platform features that would support compliance with IEEE Std 603-1991 for a specific project are described in Chapter 12.

### **5.7.9 IEEE Std 730-1998**

The RPC Radiy QMS and Radics LLC QAPD complies with the intent of IEEE Std 730-1998, *IEEE Standard for Software Quality Assurance Plans*, as described in Chapters 7 and 8.

### **5.7.10 IEEE Std 828-2005**

IEEE Std 828-2005, *IEEE Standard for Software Configuration Management Plans*, is endorsed by RG 1.169. IEEE Std 828-2005 describes a structured approach to software configuration management. The RPC Radiy and Radics LLC approaches to electronic design configuration management are described in Section 7.5. The alignment of the RPC Radiy and Radics LLC configuration management programs to IEEE Std 828-2005 is described in Chapter 12.

### **5.7.11 IEEE Std 829-2008**

IEEE Std 829-2008, *IEEE Standard for Software Test Documentation*, is endorsed by RG 1.170. IEEE Std 829-2008 describes a structured approach to software test documentation. Section 7.4.5.2 describes the RPC Radiy and Radics LLC approaches to Platform and Application ED V&V test documentation. The alignment of RPC Radiy and Radics LLC electronic design test documentation to IEEE Std 829-2008 is described in Chapter 12.

### **5.7.12 IEEE Std 830-1998**

IEEE Std 830-1998, *IEEE Recommended Practice for Software Requirements Specifications*, is endorsed by RG 1.172. IEEE Std 830-1998 is a recommended practice for writing software requirements specifications; however, as a recommend practice, it does not identify any specific requirements. The RadICS Platform and Application requirements documents are described in Chapter 7. The alignment of





the RPC Radiy and Radics LLC electronic design requirements specifications to IEEE Std 830-1998 is described in Chapter 12.

### **5.7.13 IEEE Std 1008-1987**

IEEE Std 1008-1987, *IEEE Standard for Software Unit Testing*, is endorsed by RG 1.171. IEEE Std 1008-1987 describes a structured approach for performing software unit testing. RadICS Platform electronic design testing is described in Chapters 7 and 8. The alignment of RadICS Platform electronic design testing to IEEE Std 1008-1987 is described in Chapter 12.

### **5.7.14 IEEE Std 1012-2004**

IEEE Std 1012-2004, *IEEE Standard for Software Verification and Validation Plans*, is endorsed by RG 1.168 with qualifications. The RPC Radiy and RadICS Platform ED V&V plan documentation complies with the intent of IEEE Std 1012-2004, as described in Chapters 7 and 8.

### **5.7.15 IEEE Std 1028-2008**

IEEE Std 1028-2008, *IEEE Standard for Software Reviews and Audits*, is endorsed by RG 1.168 with qualifications. The RPC Radiy and Radics LLC approaches to reviews and audits comply with the intent of IEEE Std 1028-2008, as described in Chapters 7 and 8.

### **5.7.16 IEEE Std 1050-1996**

IEEE Std 1050-1996, *Guide for Instrumentation and Control Equipment Grounding in Generating Stations*, is endorsed by RG 1.180 with qualifications. The use of IEEE Std 1050-1996 for the RadICS Platform qualification test specimen grounding and shielding is described in Chapter 9 and the RadICS Platform Equipment Qualification Plan (Reference 5-3). The system level aspects of complying with IEEE Std 338-1987 must be assessed on a project-specific basis.

### **5.7.17 IEEE Std 1074-2006**

IEEE Std 1074-2006, *IEEE Standard for Developing Software Life Cycle Processes*, is endorsed by RG 1.173, Revision 1, and provides a structured approach for developing a software life cycle program. The life cycle processes for the RadICS Platform and Application EDs are described in Chapters 7 and 8. The alignment of the RadICS Platform and Application ED lifecycles to IEEE Std 1074-2006 is described in Chapter 12.

## **5.8 Instrument Society of America Standards**

The following ISA standard was assessed for applicability to the RadICS Platform design.

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### 5.8.1 ISA-S67.04-1994

ISA-S67.04-1994, *Setpoints for Nuclear Safety-Related Instrumentation Used in Nuclear Power Plants*, is endorsed by RG 1.105 with qualifications. As described in Section 5.2.3, EPRI TR-107330, Section 4.2.4 requires the qualifier to provide information about the qualified hardware to support an application specific setpoint analysis per ISA-S67.04-1994. Chapter 9 describes the approach Radics LLC, as both vendor and qualifier, used to prepare the setpoint analysis support documentation for the RadICS Platform. This documentation will provide sufficient design specification data for a setpoint analysis to be performed on a project-specific RadICS Platform-based system. The specific means for complying with ISA-S67.04-1994 must be assessed on a project-specific basis.

## 5.9 International Electrotechnical Commission Standards

The following IEC standards were assessed for applicability to the RadICS Platform design.

### 5.9.1 IEC 60880:2006

IEC 60880:2006, *Nuclear Power Plants – Instrumentation and Control Systems Important to Safety – Software Aspects for Computer-Based Systems Performing Category A Functions*, introduces the concept of software lifecycle and details the concept of system safety lifecycle of digital systems given in IEC 61513 to the software portion of the I&C system and details the I&C validation stage in IEC 61513:2001 to the software portion of the system and introduces software-specific issues to the validation process. The life cycle processes for the RadICS Platform ED were established according to the guidance provided in IEC 60880:2006 and were documented in dedicated development plans, which are described in Chapter 7.

### 5.9.2 IEC 60987:2007

IEC 60987:2007, *Nuclear Power Plants – Instrumentation and Control Important to Safety – Hardware Design Requirements for Computer-Based Systems*, sets out the general requirements for the hardware development life-cycle of computer-based systems. The life cycle processes for the RadICS Platform ED were established according to the guidance provided in IEC 60987:2007 and were documented in dedicated development plans, which are described in Chapter 7.

### 5.9.3 IEC 61000

Chapter 9 describes the use of IEC 61000, *Electromagnetic Compatibility*, series standards endorsed by RG 1.180, Revision 1, for the electromagnetic interference (EMI)/radio frequency interference (RFI) qualification testing of the RadICS Platform.

### 5.9.4 IEC 61508:2010

IEC 61508:2010, *Functional Safety of Electrical / Electronic / Programmable Electronic Safety-Related Systems*, provides a means of certifying systems based on predefined SILs. The use of IEC 61508:2010 is described in Section 3.2.2.3.

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### 5.9.5 IEC 61513:2001

IEC 61513:2001, *Nuclear Power Plants – Instrumentation and Control Systems Important to Safety – General Requirements for Systems*, establishes the relationship between NPP safety objectives, requirements for the overall architecture of I&C systems, and requirements of the individual systems important to safety. The life cycle processes for the RadICS Platform ED were established according to the guidance provided in IEC 61513:2001 and were documented in dedicated development plans, which are described in Chapter 7.

### 5.9.6 IEC 62566:2011

IEC 62566:2011, *Nuclear Power Plants – Instruments and Control Important to Safety – Development of HDL-Programmed Integrated Circuits for Systems Performing Category A Functions*, establishes requirements for each stage of the hardware description language (HDL)-Programmed Devices (HPD) lifecycle (requirements specification, design, implementation, verification, integration and validation) to develop highly reliable HPDs for use in I&C systems of NPPs performing safety category A functions. The life cycle processes for the RadICS Platform ED were established according to the guidance provided in IEC 62566:2011 and were documented in dedicated development plans, which are described in Chapter 7.

## 5.10 U.S. Military Standards

The following U.S. MIL-STD was assessed for applicability to the RadICS Platform design.

### 5.10.1 MIL-STD-461E

Chapter 9 describes the use of MIL-STD-461E, *DOD Interface Standard Requirements for the Control of Electromagnetic Interference Characteristics of Subsystems and Equipment*, as endorsed by RG 1.180, Revision 1, for the EMI/RFI qualification testing of the RadICS Platform.

## 5.11 Electric Power Research Institute Technical Reports and Handbooks

The following EPRI documents were assessed for applicability to the RadICS Platform design.

### 5.11.1 EPRI TR-107330

In RG 1.209, NRC noted that it has accepted EPRI TR-107330, *Generic Requirements Specification for Qualifying a Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants* (dated December 1996), as an acceptable method for addressing mild-environment qualification of PLCs that is considered equivalent to, and consistent with, the RG.

The use of EPRI TR-107330 for the RadICS Platform qualification program is described in Chapter 9. The RadICS Platform ED was treated as the 'legacy software' described in Section 7.6 of EPRI TR-107330. Compensatory measures for legacy software are identified in EPRI TR-106439. The use of EPRI TR-107330 for the RadICS Platform CGD program is described in Chapter 4.

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### 5.11.2 EPRI TR-106439

In RG 1.152 Annex C, NRC identifies that EPRI TR-106439, *Guideline on Evaluation and Acceptance of Commercial Grade Digital Equipment for Nuclear Safety Applications* (dated October 1996), contains adequate guidance for the evaluation and acceptance of commercial grade digital equipment for nuclear safety applications. The use of EPRI TR-106439 for the RadICS Platform CGD program is described in Chapter 4.

### 5.11.3 EPRI Handbook 1011710

The purpose of EPRI TR-1011710, *Handbook for Evaluating Critical Digital Equipment and Systems*, is to provide practical guidance to nuclear utility engineers on how to conduct generic and project-specific CDR. The CDR can be used to gain assurance that a given critical digital system or platform has the necessary properties and will function as expected. It is a structured way to investigate and document the potential for unacceptable behavior to occur in service, due to deficiencies in the digital system specification, design, configuration, operation, maintenance, or documentation, or due to misapplication.

The use of EPRI Handbook 1011710 for the RadICS Platform CGD program is described in Chapter 4.

## 5.12 American Society of Mechanical Engineers Standards

The following ASME Standard was assessed for applicability to the RadICS Platform design.

### 5.12.1 ASME NQA-1-2008

The use of NQA-1-2008, *Quality Assurance Program Requirements for Nuclear Facilities*, and the NQA-1a-2009 Addenda to meet 10 CFR Part 50 Appendix B is described in Chapter 3. The alignment of the Radics LLC QAPD to ASME NQA-1-2008 is described in Chapter 12.

## 5.13 Chapter 5 References

- 1 NUREG-0800, NRC Standard Review Plan, Table 7-1, "Regulatory Requirements, Acceptance Criteria, and Guidelines for Instrumentation and Control Systems Important to Safety," Revision 5, March 2007
- 2 *exida* Report No. RAD 14-06-037 R002, "Results of the IEC 61508 Functional Safety Assessment for FPGA-Based Safety Controller RadICS," September 15, 2015
- 3 RadICS Equipment Qualification Test Plan, Document 2016-RTS002-EQTP-004



## 6 RadICS Platform

### 6.1 RadICS Platform Overview

RadICS Platform is a new generation product that was designed in 2010-2011. It is based on more than 10 years of RPC Radiy experience with digital I&C platform design, production, operation, and maintenance. The RadICS Platform is composed of multiple types of Modules, based on the use of FPGA chips as computational, processing, and system-internal control engines for each of the Modules. In terms of its high-level functionality and flexibility, the RadICS Platform is essentially a safety PLC, except that the internal logic is performed by FPGAs instead of microprocessors.

The typical safety-related I&C systems channel configuration, based on the RadICS Platform consists of one seismic-resistant Chassis, which contains one Logic Module (LM) and up to 14 other RadICS Modules (i.e., I/O and optical communication) in any combination of their types. The basic set of I/O Modules types comprises Analog Inputs Module (AIM), Discrete Inputs Module (DIM), Wide Range Analog Inputs Module (WAIM), Thermocouple Inputs Module (TIM), and Resistance Temperature Detector (RTD) Inputs Module (RIM), Discrete Outputs Module (DOM), and Analog Outputs Module (AOM). The Optical Communication Module (OCM) can be used to extend the system to multiple Chassis configuration. It is also possible to provide interchannel links between 2, 3, or 4 channels via fiber-optic communications directly between their LMs for coincidence voting. The RadICS Platform offers a fast response time ( $\leq 10$  milliseconds).

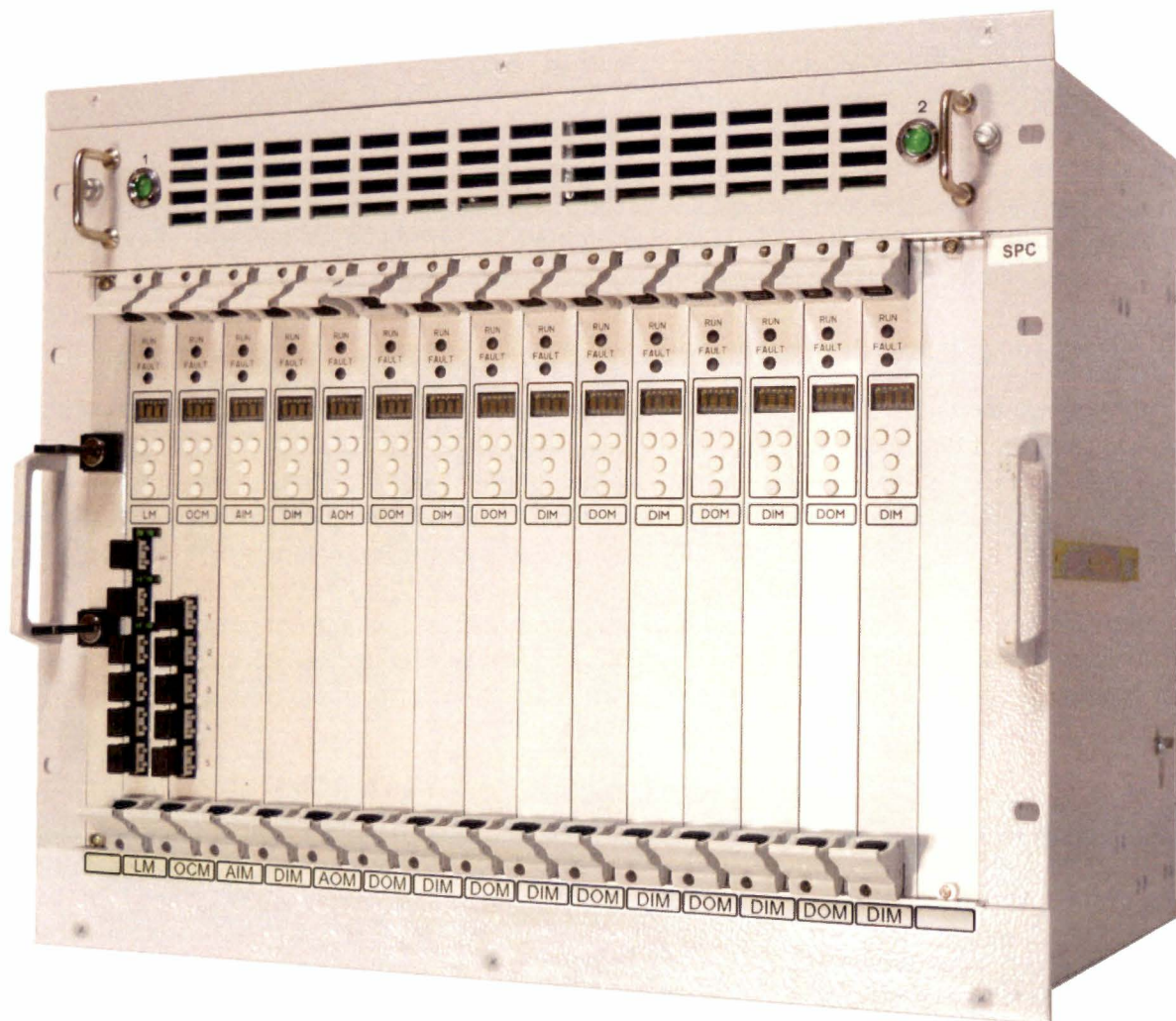
The LM performs input Modules data acquisition, execution of user configured logic, drives the output Modules, and processes diagnostic data from all I/O Modules installed in the RadICS Platform Chassis. The I/O Modules provide interfaces with other devices (e.g., detectors, sensors, actuators, signalization devices). The functionality of each Module is driven by the logic implemented in the ED onboard the FPGA(s).

The seismically-resistant Chassis for RadICS Platform provides protected external interfaces to process I/Os, two independent power supply units (links), communications links, local inputs/outputs (from/to the built-in-Chassis/cabinet detectors/sensors/keys or indicators). Internal Chassis interfaces facilitate connections to the various Modules that are installed within the Chassis by means of dedicated, isolated, point-to-point high-speed LVDS communication lines.

The RadICS Platform is configured using the RPCT and the RadICS AFBL.

A typical RadICS Platform configuration is shown in Figure 6-1.





**Figure 6-1: Typical RadICS Platform Configuration**

The RadICS Platform is itself a single rack-mount Chassis containing all required inputs, outputs and logic processing so that it operates as a single-channel device in de-energize to trip applications. Like a safety PLC, the RadICS Platform functionality is organized on two levels: the generic platform level logic and the customizable application level logic. The RadICS Platform can be configured in two to four channels configurations. In these configurations, a RadICS Platform system can meet U.S. Class 1E requirements.

In normal operation, the RadICS Platform operates in “on-line” mode and performs the safety function defined at the application level. Self-diagnostics are performed by both the application and platform



levels, although they are aimed at different types of faults. Failures detected by either level that are potentially unsafe are converted to safe failures.

In the on-line mode, no reconfiguration, no tuning, and no potentially unsafe connections to other devices are permitted. Monitoring of the RadICS Platform is possible through non-interfering one-way broadcast of application state and hardware status data. In off-line mode, in which the outputs are in the safe state, diagnostic equipment may be connected, and tuning and reconfiguration are possible.

The scope of the RadICS Platform addressed in the Topical Report is shown in Figure 6-2.

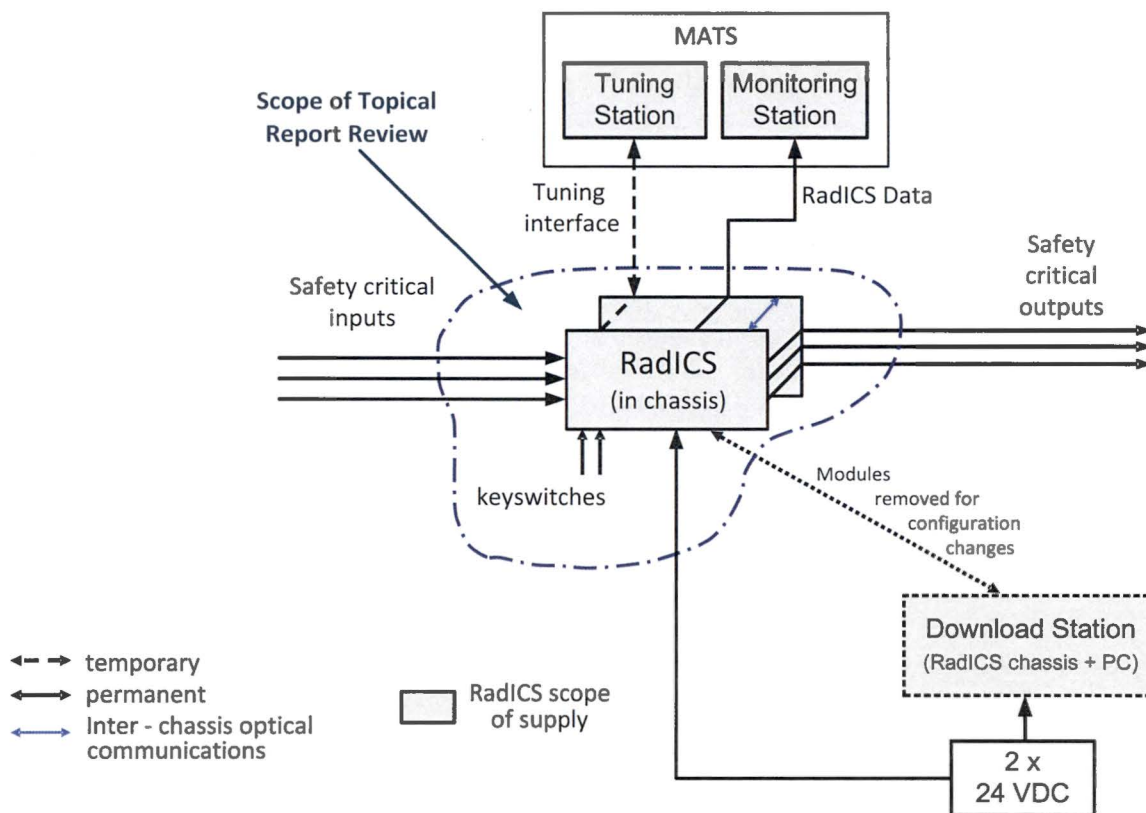


Figure 6-2: Context Diagram of the RadICS Platform

### 6.1.1 RadICS Platform General Attributes

The RadICS Platform has been designed to comply with international nuclear safety I&C requirements. The applicable regulations, regulatory guidance, industry standards, and other guidance applicable to digital safety I&C systems are documented in Chapter 5. The resulting RadICS Platform has the following general attributes:

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- **Fail-safe:** The RadICS Platform assures that, in case of detected failure meeting certain criteria, the outputs associated with a Logic Module achieve a pre-defined safe position.
- **Fault-tolerance:** The RadICS Platform supports system architectures that can meet the redundancy requirements of the single failure criterion. In addition, RadICS LMs can automatically correct its voting logic in case faults are detected, so that system availability is optimized without compromising safety. The criteria establish that no single failure will result in loss of any of the safety functions. The RadICS Platform system architecture is dictated by reliability requirements imposed on the application by the end user's requirements.
- **Diversity:** The RadICS Platform supports system architectures that employ signal diversity to defend against CCF. The RadICS Platform also can be deployed as a diverse system as part of an application-level D3 strategy. The RadICS Platform architectural and technological features provide the RadICS Platform-based integrated I&C systems with robust level of internal diversity, as described in Chapter 10.
- **Functional isolation:** RadICS Platform equipment and communications design prevents propagation of failures between redundant equipment in separate divisions. In addition, communication paths to non-safety I&C systems are electrically isolated with one-way communications from the RadICS Platform to the non- safety I&C system. This prevents faults in a non-safety I&C system from affecting the RadICS Platform.
- **Determinism:** For all processing, the same inputs produce the same outputs within a guaranteed response time
- **Self-diagnostic testing:** Self-diagnostic testing is used to check correct operation of the RadICS Modules and associated ED during startup and normal operation. The startup self-diagnostic tests check for correct operation before the RadICS Platform is released for normal operation. Other self-diagnostic tests are performed during normal operation to check for correct operation of the RadICS Modules. Self-diagnostic testing features check the integrity of the Application Logic each work cycle. Error checking is performed on all digital communications.
- **Ease of use:** Operation and maintenance are simplified by hardware, interfaces, and data transmission, and FPGA electronic designs self-diagnostics.
- **Flexibility:** Architecture flexibility and scalability to tailor general system design to customer needs in terms of number inputs received and actuators to be controlled.
- **Modularity:** The RadICS Platform can be delivered either in standard Chassis to be integrated into existing cabinets (for refurbishment purposes) or in new cabinets.
- **Scalability:** The RadICS Platform has been deployed internationally in a wide variety of safety I&C applications, including RTS, RPCLS, and ESFAS.
- **High quality development process for electronic design:** The electronic design life cycle processes used to develop the generic RadICS Platform baseline and developing the project-specific Application ED are based on recognized standards and include independent V&V.
- **Secure development and operational environment:** The electronic design life cycle processes used for the RadICS Platform establishes a secure development and operational environment for managing the generic RadICS Platform baseline and developing the project-specific Application Logic through the factory test phase. These processes protect against unauthorized, unintended, and unsafe modifications to the system, and support implementation of design requirements that promote integrity and reliability during operation and maintenance in the event of inadvertent operator actions or undesirable behavior of connected equipment.



### 6.1.2 RadICS Platform Fundamental Safety Approach

The RadICS Platform was designed to meet several high-level principles of safety.

- **De-energize to trip**

The RadICS Platform uses the de-energized state as the safe state for each RadICS Module:

- The fault status of the RadICS Platform input Modules is reported to the RadICS LM. For the Faulted mode, the RadICS LM processes such inputs as either opened contact for DIMs or zero voltage/current for AIMs, as specified in the Application Logic.
- All outputs are set to the open contact or zero voltage and zero current state as the safe state.
- All complete failures of RadICS Platform power supplies lead to the safe state. If they result in no effect on the RadICS Platform (e.g., first failure of a redundant power supply), then these failures are annunciated and flagged to the Application Logic, which can then handle the failure condition in accordance with the end user's functional specifications.

- **Automatic Transitions to the Safe State**

The RadICS Platform will drive all safety output Module outputs to the safe state for the first-occurrence of the following:

- Power is off or a Type I or II fault has occurred
- Power is initially turned on
- Startup self-diagnostic tests have not finished successfully
- Platform diagnostic results require it
- Application Logic requires it (which may include the use of RadICS Platform diagnostics reported to the Application Logic through function blocks)
- Set Safety Override (SOR) keyswitch has been used

- **Human Action Required to Leave the Safe State**

The RadICS Platform requires human intervention to release outputs from the safe state and pass them to the control of the Application Logic:

- At completion of startup (also requires that there be no detected failures)
- After the SOR has been activated for any reason
- After any failure that causes a safe-state transition

- **Correct Modules Only**

The RadICS Platform detects the presence of incorrect Modules during the self-diagnostics at startup and will maintain the safe state if any is detected.



- **IEC 61508 Safety Integrity Level 3 Capability by Design** <sup>6,7</sup>

The RadICS Modules are implemented using common Units to the extent possible:

- The RadICS Modules are designed with redundant components where needed to permit self-diagnostic tests and data redundancies are used to permit detection of data corruption with very high probability
- Watchdogs are incorporated on every Module
- CRCs are used on all communications and safety-critical data
- External communications links are all treated as 'black-channel'
- Communications ports are monitored and blocked except when specifically required (e.g., tuning)
- RadICS Modules perform the self-diagnostics and take safe-state action. This involves Application Logic where feasible (i.e., it is competent to take such action) to incorporate end user's functional requirements.
- Application ED is created using the RadICS AFBL
- Failure Modes, Effects, and Diagnostics Analysis (FMEDA) is used to confirm the failure rates and safe failure fractions

- **Application Logic Functionality**

- The Application Logic is implemented in the Application ED using the assembler provided that verifies logic for fundamental errors such as referencing non-existent I/O channels, loop-backs, etc.
- The Application ED is validated after every reconfiguration of the RadICS Platform Application ED.
- Tuning is a controlled activity: a TUNING keyswitch is required to activate the tuning port and the provided Tuning Personal Computer (PC) requires a password.
- The RadICS Platform is isolated from the field during tuning, and the end user performs a functional test of the tuning changes before returning the RadICS Platform to online status.

- **Controlled Scope**

The operational interfaces of the product are clearly defined and designed to minimize the potential for unsafe events:

<sup>6</sup> IEC standard IEC 61508 defines SIL using requirements grouped into two broad categories: hardware safety integrity and systematic safety integrity. A device or system must meet the requirements for both categories to achieve a given SIL. The SIL requirements for hardware safety integrity are based on a probabilistic analysis of the device. In order to achieve a given SIL, the device must meet targets for the maximum allowed probability of dangerous failure and a minimum acceptable safe failure fraction. The concept of 'dangerous failure' is rigorously defined for the system in question, normally in the form of requirement constraints whose integrity is verified throughout system development.

<sup>7</sup> The IEC concept for SIL (Safety Integrity Level) is different from and not to be confused with the IEEE SIL (Software Integrity Level) concept used in IEEE Std 1012 (Reference 6-1).

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- Configuration and calibration changes are performed outside the in-service RadICS Platform Chassis.
- After every configuration change to the Application ED or to the hardware configuration, the RadICS Platform must be revalidated. Configuration self-diagnostic checks are performed during system startup, as described in Section 6.2.6.
- Tuning changes are made only when the RadICS Platform trip outputs are isolated from the field (i.e., the field 'sees' a safe state). After every change to tuning parameters, the effects of the changes must be tested by the end user before reconnecting the field outputs. This means the MATS Tuning PC is not an online tool.
- The monitoring interface to the MATS is one-way broadcast (i.e., non-interfering). Thus, the MATS is also non-interfering. The MATS is supplied by the end user, to meet the end user's Human Factors requirements.
- The RadICS Platform blocks all inward communications with the only exception being tuning inputs when put into TUNING mode by the keyswitch.

### 6.1.3 Maintainability and Operability

The RadICS Platform has several features that support maintenance and operation of RadICS Platform-based systems.

- **On-line Monitoring**

On-line monitoring provides continuous indication of the results of platform diagnostics, RadICS Platform operating mode, presence and state of keyswitches, selected field input and/or Application Logic signals, the current operational Application ED tuning values, and proposed tuning values as they are set by the MATS Tuning PC. RadICS Platform monitoring data sent over to the MATS via a one-way data link. Thus, the plant operators in the control room can be informed of failures detected by the RadICS Platform system and can initiate system maintenance. They can also monitor all access to the system and check entered tuning values for human errors. The MATS also permits the plant operators to confirm the post-tuning testing. All these features lead to maintainers approaching the system with good diagnostic information and verification by control room staff to detect errors before they can adversely affect the plant.

- **Operational Parameter Tuning Capability**

Operational parameters may need to be adjusted during a reactor operating cycle or between cycles. The RadICS Platform provides the ability to tune these parameters via the Fiber Optic Tuning Interface using the MATS. Tuning is normally locked out and is enabled only by a keyswitch. In the TUNING mode, parameters that are specified in the Application ED can be adjusted by connecting a MATS Tuning PC with special software to the RadICS Platform. The RadICS Platform outputs are isolated from the field (i.e., safe state) for tuning. The end user performs functional tests to confirm the tuning values before restoring the system to normal operation. The RadICS Platform also checks tuning values for 'reasonableness' and basic validity. The Application Logic can also be engineered to perform other specified checks. Tuning

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parameters are stored in electrically erasable programmable read-only memory (EEPROM) on the RadICS LM, so they are retained even after power is lost and restored.

- **Minimized Maintenance Error**

The RadICS Platform design incorporates features to minimize the potential for maintain or operator error that could lead to unsafe operation of the product. This includes:

- A non-interfering local status display on every RadICS Module
- Comprehensive diagnostics relayed to the MATS
- Detection of some maintenance errors (e.g., wrong module in a slot)
- Hot-swap capability
- Validated maintenance documentation
- User SOR

- **Hardware Protection**

Protective devices are used at all RadICS Module interfaces:

- Diodes and/or voltage limiters are used as appropriate to protect devices that interface to the field
- Fiber optic interfaces are used where practical
- All interfaces between a Module and the Chassis backplane are galvanically isolated, including power connections

- **Checking of User Configuration and Tuning Values**

Configuration of the Application ED is an offline activity using offline tools. The offline configuration tool checks for detectable errors in coding such as loopbacks, references to Modules in the wrong slot, or the wrong kind of Module. Actual installation errors such as using the wrong slot are detected online at startup. Tuning is normally locked out and is enabled only by a keyswitch. The RadICS Platform outputs are isolated from the field (i.e., safe state) for tuning, and the end user performs functional tests to confirm the tuning values before restoring the system to normal operation. The RadICS Platform also checks tuning values for 'reasonableness' and basic validity.

- **User Safety Override**

The LM and output Modules have SOR Units that allow the user to force the RadICS Platform into the safe state. The SOR Unit overrides all outputs of the Application and Platform ED to drive the outputs to the safe state.

- **Hot Swappable Modules**

The RadICS Platform design permits removing and replacing a Module while the Chassis is powered up (hot swap) or powered down. It is expected that the maintainer follows the appropriate procedures to ensure that maintenance activity does not affect the RadICS Platform operation in a way not foreseen by the Application ED.

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All RadICS Modules have been designed to be hot-swappable to prevent damage due to maintenance error. The normal procedure is to power down the RadICS Platform Chassis before performing maintenance; however, all Modules are hot-swappable, so no damage will occur to a Module even if it is extracted or inserted at power. Plant safety is assured when a hot swap action is performed, since any Module that has been removed will be identified as failed. The LM will make the identification for a hot swap of an I/O Module in its Chassis. The output Modules in the Chassis and other LMs in the system (e.g., other divisions) will make the identification if a LM is removed from a Chassis. The LMs will use the diagnostic information to take the appropriate actions, as specified in the end user's functional requirements for the Application Logic.

Removal of the LM will force all output Modules to the safe state. When a replacement LM is inserted and completes its startup sequence, the LM will return to normal operation. The LM may be held in RUN (SAFE) mode until the SOR is reset unless it is hard-wired to be automatic. Removal of any I/O Module will also force all output Modules to the safe state.

- **Authentication of the RadICS Module Version**

Nuclear standards specifically require authentication of the version of installed software. The hardware version of every RadICS Module is inscribed on the back side of the Module printed circuit board. The ED version installed in the RadICS Module FPGA can be displayed on the 4-character display of the Module.

The RadICS Platform features that support maintenance and operation facilitate timely recognition, location, replacement, repair, and adjustment of malfunctioning equipment, which satisfy the repair requirements of IEEE Std 603-1991 Section 5.10 (Reference 6-2). The RadICS Module version authentication features satisfy the identification requirements of IEEE Std 7-4.3.2-2003 Section 5.11 (Reference 6-3).

#### **6.1.4 FPGA Based Digital Technology**

The RadICS Platform is composed of various standardized Modules, each based on the use of FPGA chips as computational engines.

FPGA-based I&C systems have been developed and applied to applications in the aerospace and process industries since the early 1990s. Although the use of FPGAs in nuclear power plants has lagged in the past, compared to other industries, due to quite conservative approaches, there are an increasing number of FPGA installations in operating nuclear power plants worldwide, most of them provided by RPC Radiy.

FPGA technology is an alternative to microprocessor-based technologies and other types of programmable devices. FPGAs are semiconductor-based programmable devices that can be configured to perform custom-designed functions. It includes two entities: an FPGA chip that is a hardware component that can be tested against hardware qualification requirements, and the electronic design, represented by a set of instructions in HDL to be configured into the FPGA hardware and that can be verified against functional requirements.

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There are two main FPGA chip architectures: fine-grained and coarse-grained. The coarse-grained FPGAs have very large logic blocks (macrocells) with sometimes two or more sequential logic elements, and the fine-grained ones have very simple logic blocks.

Another architectural difference is the technology used to manufacture the FPGA chips. The most common technologies are:

- EPROM/EEPROM/Flash based chips are re-writable types (they allow reprogramming of the FPGA) and non-volatile (no data or logic is lost in case of power losses)
- SRAM based chips are re-writable, but volatile
- Anti-fuse based chips are non-rewritable and non-volatile (one-time programmable)

The RadICS Platform uses SRAM-based FPGAs for the Modules and complex programmable logic devices (CPLDs) for the watchdogs.

The development process of FPGA applications typically consists of requirement specification, design, implementation, and integration along with the associated V&V activities.

The objective of the requirements specification phase is to define precisely all the requirements that apply to the FPGA platform and associated application. These requirements are usually derived by following a top-down approach whereby each system component is allocated functional and safety requirements and interfaces among them are defined.

The most critical phase of the FPGA overall development process is the design phase. Errors made in this phase will dramatically affect all subsequent stages. The development process includes architectural and detailed design activities. The development process for the RadICS Module EDs is described in Chapters 7 and 8.

### 6.1.5 Benefits of FPGA Technology

The application of FPGA technology has significant advantages that can be utilized both in I&C modernization projects of existing nuclear power plants and in I&C designs for new nuclear power plants. These advantages are the following:

- Design, development, implementation, and operation simplicity and transparency
- Easy portability of algorithms and possibility of re-programming, if algorithms or technology may change in the future, but the hardware stays the same
- Reduction of vulnerability of the digital I&C system to cyber-attacks or malicious acts due to the absence of any system software or operating systems
- Faster and more deterministic performance due to capability of executing logic functions and control algorithms in a parallel mode; due to advantage of hardware parallelism inherent to FPGA technology, which can process more data, provide faster input and output response times and execute more instructions per clock cycle than digital signal processors
- Possibility to segregate safety functions and ancillary functions on the same integrated circuit (e.g., such as communication diagnostics and Application ED)
- Diversity with the potential to comply with strict requirements that include, but are not limited to, design, equipment, functional, and electronic design diversity

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- More reliable, testable and error-free end-product due to reduction in the complexity of the V&V and implementation processes
- More direct qualification process for FPGA-based safety systems due to the simplicity and transparency of system architecture and its design process
- Resilience to obsolescence due to the portability of the HDL code between different versions of FPGA chips produced by the same or different manufacturers: even if the FPGA migrates to the next generation, the HDL code remains unchanged

## 6.2 RadICS Chassis-Level Features

### 6.2.1 Theory of Operation

Figure 6-3 illustrates the operation of RadICS Platform and shows the operation of the LM and I/O Modules. Adding more I/O Modules does not change the fundamental operation. This figure shows that there are two levels of logic in the LM (i.e., Application and Platform) and only the Platform level in the I/O Modules.

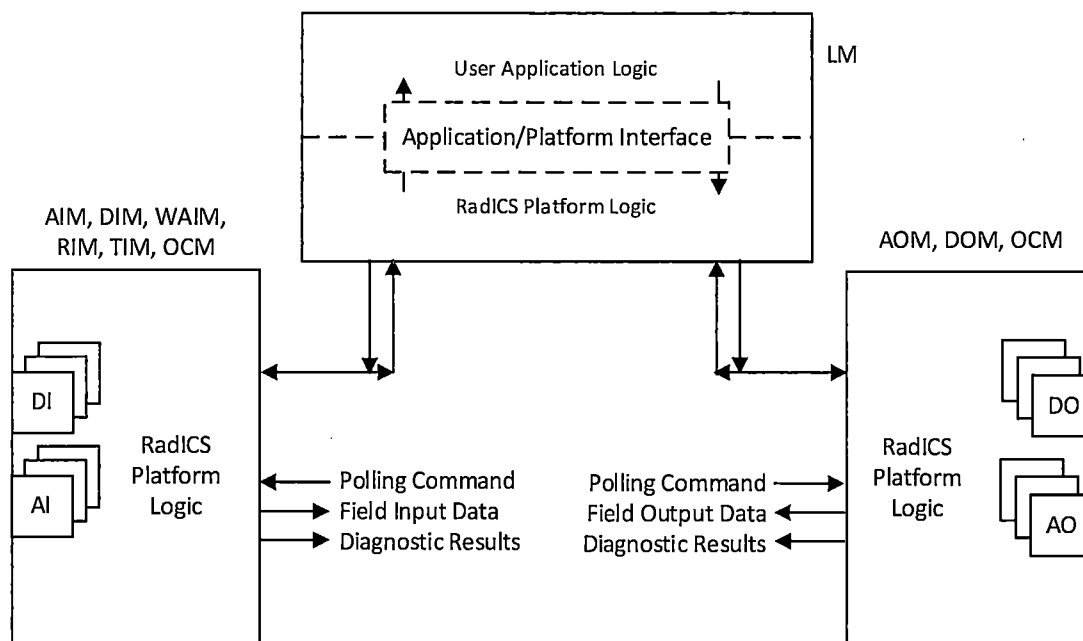


Figure 6-3: Theory of Operation of RadICS Platform

After initialization, the RadICS Platform operates with a standard Work Cycle that is performed cyclically. The basic RadICS Platform Work Cycle includes four Phases:

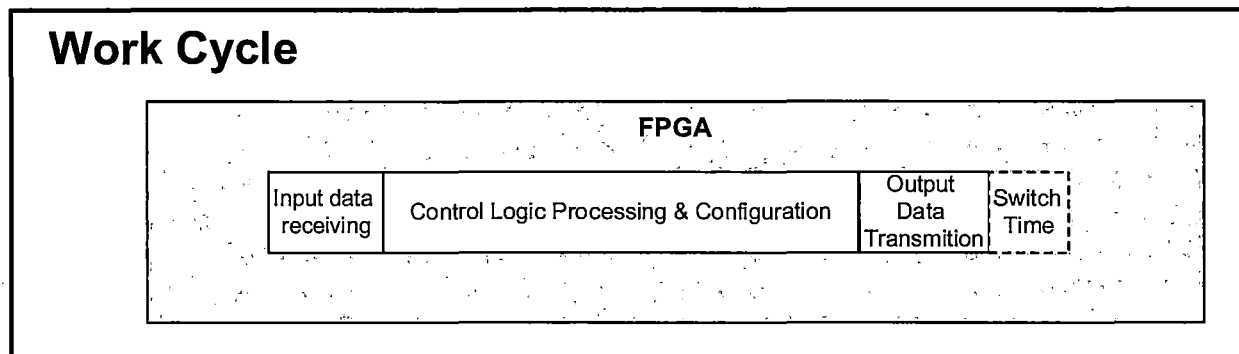
- Input Data Receive – Request and receive input data for the current Work Cycle from I/O Modules and perform Application Logic test code

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- Application Logic Processing and Configuration – Process Application Logic and preparation (i.e., configuration) of communication messages
- Output Data Transmission – Transmit Application Logic processing results to the output Modules
- Switch Time – Allows time for output Modules to complete switching

The standard RadICS Platform Work Cycle is illustrated in Figure 6-4.



**Figure 6-4: RadICS Platform Work Cycle**

The Work Cycle is controlled by the LM, as described in Section 6.2.6.1.2. The other RadICS Modules operate in response to commands from the LM, as described in Sections 6.2.6.2 through 6.2.6.5.

All RadICS Modules include several common elements plus the specialized hardware for their specific purpose. The common hardware elements include:

FPGA	executes all platform control logic (plus Application Logic in the LM) plus extensive diagnostics
CPLD	acts as watchdog, monitors power supplies and FPGA; can force the Module into FAULTED mode, which drives the safe state
Power supply	Each Module taps the two +24 Volts Direct Current (VDC) supply lines on the backplane and develops all needed voltages.
Clocks	Each Module has several independent clocks to provide for self-checking
LVDS	communications on the private backplane lines between Modules (LM $\leftrightarrow$ I/O)
Display	status display on the front of each Module, for maintainer
SOR	Safety Override (on output Modules only): allows a temporary override to force safe state outputs at a system level

These standard features are described further in Section 6.2.5.

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### 6.2.1.1 Chassis

The RadICS Chassis distributes two +24 VDC supplies to every slot. Each Module taps both these supplies for redundancy and develops its own voltages needed to operate all the Units within the Module. This includes the various voltages needed by the FPGA. Any voltages needed by the I/O channels are galvanically isolated on a channel basis.

All RadICS Modules communicate via the backplane, using direct individual lines from each I/O slot to the LM slot. I/O Modules have no direct communication with each other; rather they each have one direct individual line to the LM slot.

### 6.2.1.2 Input/Output Modules

Each I/O Module operates autonomously. Each I/O Module constantly performs self-diagnostic tests on its own common hardware, individual I/O channel hardware, and on its ability to communicate with the LM. The self-testing is interrupted<sup>8</sup> on the individual DIM input channel hardware when the DIM receives a command from the LM. The LM polls the DIM to provide it with field data and self-diagnostic results. The DIM diagnostics resume once the LM command is executed. All the other I/O modules do not interrupt any self-testing or data acquisition when get a request from the LM to send data.

To permit exhaustive self-diagnostics as required by IEC 61508 (Reference 6-4), the individual input or output channels on the I/O Modules have sufficient hardware redundancy so that random hardware failures can be detected by the self-diagnostics. Similarly, data handling in the FPGA involves high-order CRC checks so that the vast majority of functional and memory faults and communications errors are also detected. A separate CPLD acts as a watchdog to detect FPGA failures or failures affecting the FPGA that it cannot detect and puts the Module into FAULTED mode (safe state) if that occurs or the FPGA reports a Type I fault to the watchdog.

For I/O Module channel faults, the I/O Module will continue to operate, but the I/O Module will signal to the LM that the failed channel's data is bad. The 4-character display on the front of the Module will display a fault code instead of RUN and the diagnostic result is reported to the Application Logic. For total Module failure, such as a failure affecting the FPGA, the Module will shut down; this will also be detected by the LM and reported to the Application Logic.

### 6.2.1.3 Optical Communication Module

The OCM is used to extend the capacity and capabilities of the RadICS Platform (i.e., to allow Application Logic running in one chassis LM to use data derived from I/O in other chassis). Each chassis LM can execute logic related to I/O within its own chassis as well share selected data with logic in another chassis. The OCM provides five optically-coupled SIL 3 black-channel links to these expansion chassis by linking an OCM in each pair of chassis.

Failures within one chassis are detectable in another chassis in the following ways:

<sup>8</sup> Interrupted in this context does not mean an interrupt of software execution, because there is no software; instead it means the test logic is momentarily disabled and the command response logic is enabled.





- A Type I fault in an OCM will cause it to stop updating OCMs in other chassis; consequently, an unfaulted chassis will see a communications timeout on the OCM communicating with the faulted chassis.
- A Type I fault in any I/O module except OCM results in setting all modules within that chassis to the safe state, in which case an OCM will continue updating OCMs in other chassis and additional actions from the Application Logic are needed.
- Communications errors between the OCMs will result in error codes set by both OCMs
- User level values can be communicated (e.g., each signal needed in other chassis can be accompanied by 'health' signals, so if an analog input in one chassis fails, the health signal can inform logic in the LM of another chassis that the analog input value is untrustworthy).

The OCM also includes five RS-232/485 channels for communications to external devices, but these are reserved for future use.

#### **6.2.1.4 Logic Module**

The LM includes two separately designed logic configuration levels: the RadICS Platform Logic and the end user Application Logic. Both levels of logic are protected by the same CRC checks and timing checks by the watchdog, as described for the I/O Modules.

#### **6.2.1.5 Operation Modes Overview**

The following text provides an overview of the operation modes for all Modules.

**POWERED-OFF** This mode represents removal of power from the Module or the RadICS Platform, whether by human action or by loss of the power sources. The RadICS Platform is powered off when both 24 VDC supplies are removed. In the powered-off state, all the RadICS Platform outputs are in their safe state.

**STARTUP** In this mode, the FPGA acquires its configuration from EEPROM and this is verified by a CRC check. The FPGA then starts normal operation, including executing the Application Logic, and performs all the self-diagnostic tests applied in RUN mode plus some extra tests. Any Type I fault results in exit to FAULTED mode. If no failures are detected, the Modules exit to RUN (SAFE) or RUN mode (depending on the Module), but it is possible for the operator to trigger exit to CONFIGURATION mode. When the RadICS Platform is powered up, there is a  $[[ \quad ]]$ <sup>a,c,e</sup> second period of operation in STARTUP mode during which all outputs are held in the safe state and the RadICS Platform executes all standard self-diagnostic tests plus some extra startup tests. At the end of STARTUP mode, all Application Logic is initialized, and ready to run.

**RUN (SAFE)**

In this mode, all the Application Logic is up and running, but the outputs are overridden by the SOR and maintained in the safe state. Operator intervention is required to advance to RUN or TUNING mode. There are no conditions of automatic transition to the RUN or TUNING mode. This mode does not exist for input Modules since they do not have field outputs or SOR Units. RUN mode self-diagnostic tests are executed.

At the end of a successful STARTUP mode period (i.e., no Type I faults detected), the RadICS Platform will allow the SOR to be reset and until the SOR is reset, the RadICS Platform operates in RUN (SAFE) mode. In RUN (SAFE) mode, the Application Logic executes normally, setting the internal values of the outputs, but all outputs are subjected to the SOR, which sets the final outputs to the safe state.

Transition out of RUN (SAFE) mode into RUN mode occurs when the Reset-SOR input is closed and all conditions that set the SOR have cleared. There are two options to implement this: 1) manual reset by the operator using a momentary contact keyswitch or 2) installed wiring that holds the reset circuit closed, thus providing an automatic transition from STARTUP mode (i.e., momentarily to RUN (SAFE) mode, and then to RUN mode).

**RUN**

In this mode, all the Application Logic is up and running and controls the outputs. RUN mode self-diagnostic tests are executed.

**TUNING**

In this mode, parameters that the Application Logic design provided for can be adjusted by connecting a MATS Tuning PC with special software to the RadICS Platform.

TUNING mode requires the use of a TUNING key and an end user supplied contact that when closed, indicates that the safety load of the RadICS Platform (i.e., the final actuator) is held in the safe state (controlled by what is called the ARMING key). This permits the end user to fully test the tuning changes under safe conditions, since the output contacts can be opened or closed without affecting plant safety.

**FAULTED**

In this mode, all outputs are forced to the safe state. This mode results from discovery of a Type I fault. The only exit from this mode is via powering off the RadICS Platform.



CONFIGURATION

This mode has two functions: configuration and calibration.

- Configuration: Changes to the Application Logic or configuration of the RadICS Platform must be made in a Chassis equipped for this purpose, called the Download Station (DLS). All Modules also store authentication data in EEPROM that includes version information. This information is sent to the MATS when online. To change or download this data, one uses this mode and the DLS.
- Calibration: Analog Modules (AIM, RIM, TIM, WAIM, and AOM) use this mode to perform hardware calibration. Calibration can be done in the in-service Chassis; however, the application designer must design logic to ensure safety during calibration. Calibration can also be performed when the Modules are removed from the Chassis by using the DLS.

The Application Logic can be designed to detect whether a module is in CONFIGURATION mode and ensure safety. Input signal ports are provided to detect this state and to engage the SOR.

6.2.1.6 Human-Machine Interface

The RadICS Platform consists of functionally dedicated Modules (i.e., each Module performs one kind of I/O) inserted into the slots of the RadICS Chassis. All empty slots are populated with fixed blanks to protect the Chassis interior from dirt and accidental insertion of tools. IEC 61508 requires that the designer “consider” human factors issues. Chassis-related human factor features include:

- Labeling to identify slot allocation
- Visually verifiable tie-down clamps
- Blanks covering all unused slots
- Front mounted fiber optic connectors for LM and OCM
- Rear-connected I/O

The labeling of each slot minimizes the likelihood of a maintenance technician inadvertently inserting a wrong type of Module into any active slot. The RadICS Platform will detect such error via its startup self-diagnostics even if such a mistake is made, as described in Section 6.2.6.1.2. These self-diagnostics would detect an incorrect replacement made during a hot swap when the module goes through the STARTUP Mode.

The tie-down clamps exert a positive pressure on the Modules to ensure they stay inserted during a seismic event. The full insertion of a Module and complete clamp-down are visually verifiable because the clamp rotates to a position in contact with the Module faceplate when correctly closed, and rests at a noticeable angle.

To ensure that Modules can be inserted into active slots only, a permanent dummy plate covers unused Module slots. Even if this feature did not exist, an I/O Module that was inserted would have no effect on the system, since the slot was not enabled in the specific RadICS Platform configuration.



There are fiber-optic connectors on the LM and OCM, which can be used to communicate with LMs in other Chassis. All I/O cables are rear-connected. There is normally no need for access during system operation, so the rear connections eliminate many potential maintenance errors.

The RadICS Platform human-machine interface features satisfy the identification requirements of IEEE Std 603-1991 Section 5.11.

### 6.2.2 RadICS Chassis Configuration

The RadICS Chassis has 2 slots for LMs<sup>9</sup> and 14 slots for other I/O Modules. The mechanical design of the RadICS Chassis (hereinafter referred to as Chassis) is a metal box consists of 16 physical slots accessible from the front for Modules, backplane for providing connections between Modules and power supply for the Modules, and two fans (with associated control board). Each of the slots for Modules is equipped with rails for proper and safe installation. There are 14 physical slots for special Interface Protection Modules (IOPM) associated with the I/O Modules and OCMs that are accessible from the rear (see Figure 6-5). Each Module and IOPM locks into place with a lever at top and bottom. Electrical connection of each Module and IOPM is accomplished by insertion of the board into the Chassis socket. There are no slots for a separate LM Interface Protection Module because the LMs have few I/O channels in their design and the associated protection circuitry is placed on the LM board.

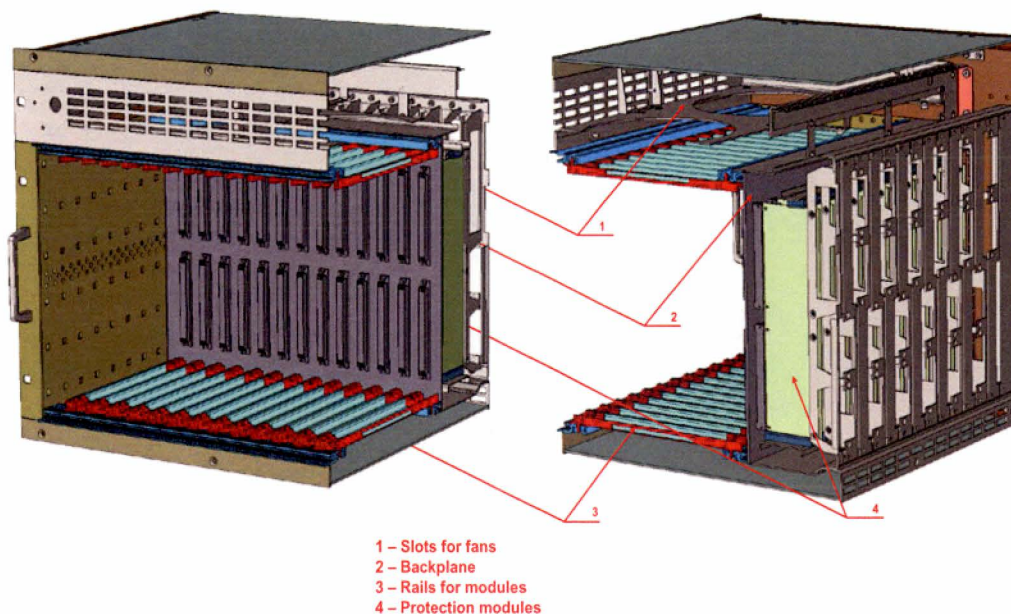


Figure 6-5: RadICS Chassis Design

<sup>9</sup> The mechanical design allows for two LM, but only one LM is used at present.



The Chassis is configured by installation of the distinct types of Modules in accordance with the following configuration constraints:

- Two LM Slots are reserved for LMs in the Chassis (i.e., slots F1 and F2). The qualified configuration will use only one LM, in slot F1
- Modules for Input Signals (i.e., AIM, DIM, RIM, TIM, and WAIM) may be installed in any slot from #1 to #14
- Modules for Output Signals (i.e., DOM and AOM) may be installed in any slot from #1 to #14
- Modules for Optical Communication (i.e., OCM) may be installed in any slot from #1 to #14
- Any slot (except F1 for the LM) may be left empty

Special coding pegs are provided for I/O Modules to prevent a RadICS Module from being inserted into the wrong slot.

The Chassis configuration is shown in Figure 6-6.

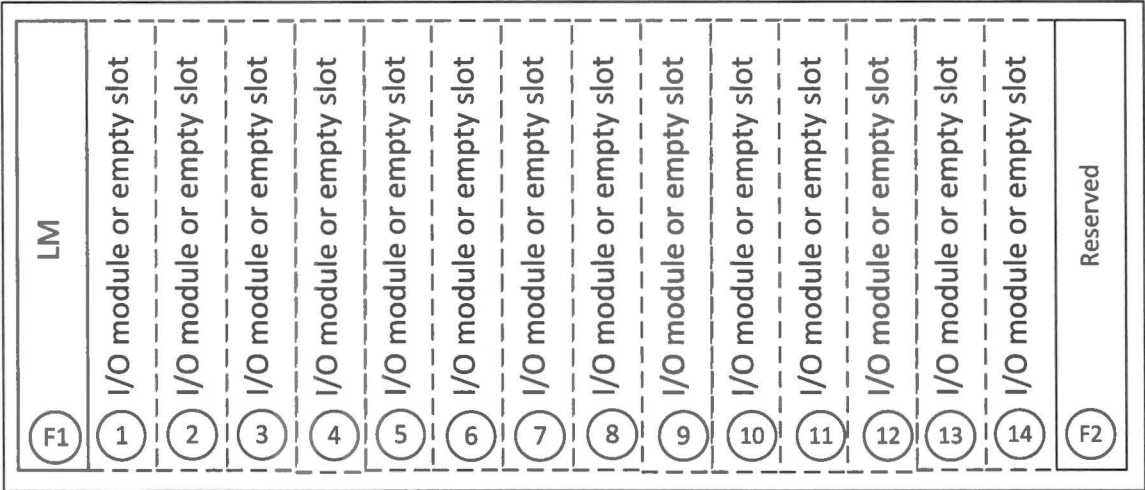


Figure 6-6: RadICS Chassis Configuration

The RadICS Platform Chassis connectors are located on the rear of the Chassis, as shown in Figure 6-7.



[[

]]<sup>a,c,e</sup>

Figure 6-7: Rear of RadICS Chassis Showing Connectors

The [[  
]]<sup>a,c,e</sup> are XR1 and XR2 at the top of the Chassis. The [[  
]]<sup>a,c,e</sup> is XN1 at the far right.

This figure also shows the connectors for individual Modules. Connector XM1 is for the [[  
]]<sup>a,c,e</sup> and appears on the right in the rear view. Two connectors (XA1 and XA2) are used for the AIM, WAIM, RIM, TIM, DIM, and AOM. The Interface Protection Module for the DOM has higher ratings consistent with the duty requirements of the digital output circuits. [[

]]<sup>a,c,e</sup> OCM port connectors XA1 – XA are used for RS-232/485 interfaces. The Interface Protection Module for OCM does not contain any additional protection feature for the OCM and only extends the OCM connections to the back of the chassis and provides connectors for external links. Connector XM2 is not used.





Table 6-1 summarizes the qualified hardware components and the programmable logic configuration items that are included in the RadICS Platform to be qualified.

**Table 6-1: Qualified Components**

Part Number	Description (Hardware Identifier)
A007.C00.V00.R02	Chassis and Backplane Hardware (469116.103-01)
A001.C00.V01.R00	Logic Module Hardware (468243.100)
A001.FV01.FR01.CV02.CR00	LM Platform Electronic Design
A003.C00.V01.R00	Analog Inputs Module Hardware (467482.068)
A008.C00.V00.R01	I/O Interface Protection Module for AIM, WAIM, TIM, DIM, and AOM - Top (468243.102)
A008.C00.V00.R01	I/O Interface Protection Module for AIM, WAIM, TIM, DIM, and AOM - Bottom (468243.102-01)
A003.FV01.FR03.CV01.CR00	AIM Platform Electronic Design
A004.C00.V00.R00	Discrete Inputs Module Hardware (467482.069)
A004.FV00.FR01.CV01.CR00	DIM Platform Electronic Design
A020.C00.V00.R00	Wide Range Analog Inputs Module Hardware (467482.093)
A020.FV00.FR04.CV01.CR00	WAIM Platform Electronic Design
A018.C00.V00.R00	Thermocouple Inputs Module Hardware (467482.096)
A018.FV00.FR04.CV01.CR00	TIM Platform Electronic Design
A019.C00.V00.R01	RTD Inputs Module Hardware (467482.098)
A008.C00.V00.R01	I/O Interface Protection Module for RIM - Top (468243.102-04)
A008.C00.V00.R01	I/O Interface Protection Module for RIM - Bottom (468243.102-05)
A019.FV00.FR04.CV01.CR00	RIM Platform Electronic Design
A002.C00.V03.R00	Analog Outputs Module Hardware (467482.067)
A002.FV01.FR02.CV01.CR01	AOM Platform Electronic Design
A006.C00.V00.R00	Discrete Outputs Module Hardware (468172.057)
A006.FV00.FR01.CV01.CR00	DOM Platform Electronic Design
A008.C00.V00.R01	DOM Interface Protection Module - Top (468243.102-02)
A008.C00.V00.R01	DOM Interface Protection Module - Bottom (468243.102-03)



Part Number	Description (Hardware Identifier)
A005.C00.V00.R01	Optical Communication Module Hardware (468383.044)
A008.C06.V00.R01	OCM Interface Protection Module (468243.103)
A005.FV00.FR02.CV01.CR00	OCM Platform Electronic Design
A014.C00.V00.R00	Ventilation Module Hardware (067319.013-01)
A011.FV00.FR00.CV00.CR00	Ventilation Module Electronic Design
685624.881-06	Cable Assembly for LM
685624.882-06	Cable Assembly for AIM
685624.882-07	Cable Assembly for AIM
685624.883-06	Cable Assembly for AOM
685624.883-07	Cable Assembly for AOM
685624.884-06	Cable Assembly for DIM
685624.884-07	Cable Assembly for DIM
685624.885-06	Cable Assembly for DOM
685624.885-07	Cable Assembly for DOM
685628.288	Cable Assembly for WAIM
685628.288-01	Cable Assembly for WAIM
685628.286-01	Cable Assembly for TIM
685628.286-02	Cable Assembly for TIM
685628.361	Cable Assembly for TIM – Long Version
685628.361-01	Cable Assembly for TIM – Long Version
685628.336	Cable for RIM 2-wire connection
685628.336-01	Cable for RIM 2-wire connection
685628.337	Cable for RIM 3-wire connection
685628.337-01	Cable for RIM 3-wire connection
685628.287	Cable for RIM 4-wire connection
685628.287-01	Cable for RIM 4-wire connection
685624.886-06	Bypass Cable Assembly
685624.886-07	Bypass Cable Assembly
685624.895-20	Fiber Optic Cable Assembly



Part Number	Description (Hardware Identifier)
685628.360-04	Power Supply Cable Assembly
685628.011-02	RS232/485 Serial Cable Assembly

The allocation of Modules to the slots is verified at startup to match the configuration defined in the Application ED. The LM compares information received from the I/O Modules with the expected configuration. The LM will prevent continued operation of the system by transitioning to the FAULTED mode.

All RadICS Modules can be removed or inserted while power is off. The Modules are also designed to be hot-swappable to prevent damage due to maintenance error.

### 6.2.3 Multiple Channels of RadICS

The basic set of Modules that can be used to create application with a choice of higher-level redundant architectures that include 1-out-of-2, 2-out-of-3, and 2-out-of-4 configurations. The single channel Chassis is a common high-level building block that is used for these configurations. Multiple Chassis can be used to extend a single channel configuration for scalability by connections between the OCMs for scalability expansion within a division and between LMs for coincidence voting in multi-division systems.

### 6.2.4 Overview of RadICS Chassis Interfaces

Four standard interfaces are used in the RadICS Platform:

- External Interfaces are used to communicate with another Chassis or specific device
- Internal Interfaces are used for on-board communications within a Module or for Module to Module communications within a Chassis
- Online Interfaces are interfaces that can directly influence a safety-critical system during normal operation
- Offline Interfaces are interfaces used for a safety-critical system configuration when it is out of operation

Table 6-2 shows a list of all existing interfaces of the Chassis and Modules including their classification.

**Table 6-2: Classification of RadICS Chassis and Modules Interfaces**

Interfaces/Type	External	Internal	Online	Offline
24 VDC Power Supply Interface	+	-	+	-
I/O Interface	+	-	+	-
Fiber Optic (RUP) Interface	+	-	+	-



Interfaces/Type	External	Internal	Online	Offline
Fiber Optic (RPP) Interface	+	-	+	-
Fiber Optic (RUP) Interface*	+	-	-	+
Safety Override Interface	+	-	+	-
RS-232/485 Interface	+	-	+	-
Address Interface (on-board jumpers)	-	+	+	-
Tuning Access Interface	+	-	+	-
LVDS Interface	-	+	+	-
Active Serial Programming Interface (ASPI) Interface	+	-	-	+
Joint Test Action Group (JTAG) Interface	+	-	-	+
Serial Peripheral Interface (SPI) Interface	+	-	+	-
Universal Asynchronous Receiver/Transmitter (UART) Interface	+	-	-	+
Watchdog Interface (voltage diagnostic data only)	-	+	+	-
Synchronous Static Random-Access Memory (SSRAM) Interface	-	+	+	-
Real Time Interface	+	-	+	-

\* - for tuning purpose

Figure 6-8 shows a high-level block diagram of the Chassis and its associated external and internal interfaces.



[[

]]<sup>a,c,e</sup>

Figure 6-8: RadICS Chassis Diagram with Internal and External Interfaces

6.2.4.1 RadICS Chassis External Interfaces

All external interfaces of the single channel Chassis are galvanically-isolated interfaces to components outside this Chassis. The Chassis external interfaces are:

- 24 VDC Power Supply Interface is used to provide [[ ]]<sup>a,c,e</sup> to the Chassis. This power interface is safety related.
- I/O Interfaces are provided via connectors on the backplane for the field I/O connections to the I/O Modules and LM. [[

]]<sup>a,c,e</sup>



- LM-to-MATS interface uses a one-way link using the Radiy User Datagram Protocol (UDP)-based interface protocol (RUP) for communications via fiber optical medium. This communication interface is safety related.
- Tuning interface with MATS Tuning PC uses one bidirectional link using the proprietary Radiy Tuning Interface (RUP) via fiber optical medium. This communication interface is not safety critical.
- Tuning Access Interface provides a safety related [[ ]]<sup>a,c,e</sup> to de-energize RUP Fiber Optic Interface. This communication interface is safety related.
- Safety Override Interface uses a safety related [[ ]]<sup>a,c,e</sup>. The LM, AOM, and DOM are equipped with the SOR. When set the SOR will override the normal Application Logic outputs and put the affected Module outputs into the safe state. This communication interface is safety related.
- UART, ASPI, and JTAG Interfaces are special interfaces for [[ ]]<sup>a,c,e</sup>. These communication interfaces are safety related.
- Inter-Chassis link uses the Radiy Proprietary Protocol (RPP) Fiber Optic Interface for safety critical communications that can be used to expand a RadICS Chassis up to a total of [[ ]]<sup>a,c,e</sup> using OCM OPTO Units within a single division and with up to [[ ]]<sup>a,c,e</sup> (e.g., four 2-out-of-4 voting channels) using the LM OPTO Units for connections between LMs in different divisions.

#### 6.2.4.2 RadICS Chassis Internal Interfaces

The single channel Chassis also has internal interfaces that facilitate connections to the various Modules that are installed within the Chassis. These interfaces are at two levels: [[ ]]

[[ ]]<sup>a,c,e</sup>

- [[ ]]

[[ ]]<sup>a,c,e</sup> and is safety critical.

- [[ ]]

[[ ]]<sup>a,c,e</sup> This

interface is not safety critical, because the [[ ]]

[[ ]]<sup>a,c,e</sup>. The [[ ]]

[[ ]]<sup>a,c,e</sup> is a non-safety interface to [[ ]]

[[ ]]<sup>a,c,e</sup>. The slot reserved for

the LM has [[ ]]





function does not impact safety critical operation. The <sup>a,c,e</sup> on a local display unit located on the front panel of the Module. The <sup>a,c,e</sup> does not impact safety critical operation.

6.2.5 RadICS Hardware Modules

The RadICS Modules are implemented using common sub-modules or “Units” to the extent possible.

Module	Highest level Module within the RadICS Platform (e.g., LM, DIM, etc.)
Unit	Low to intermediate level module mounted on one or more Modules (e.g., LVDS transceiver, clock unit, etc.)

6.2.5.1 RadICS Module-Related Features

The aspects of each Module that relate to maintainability are all mounted on the faceplate of the Module as shown in Figure 6-9, with the deliberate exception of the JTAG connector, which is mounted to be inaccessible while the Module is installed in the Chassis. This figure shows the hold-down latches in the closed/locked position.

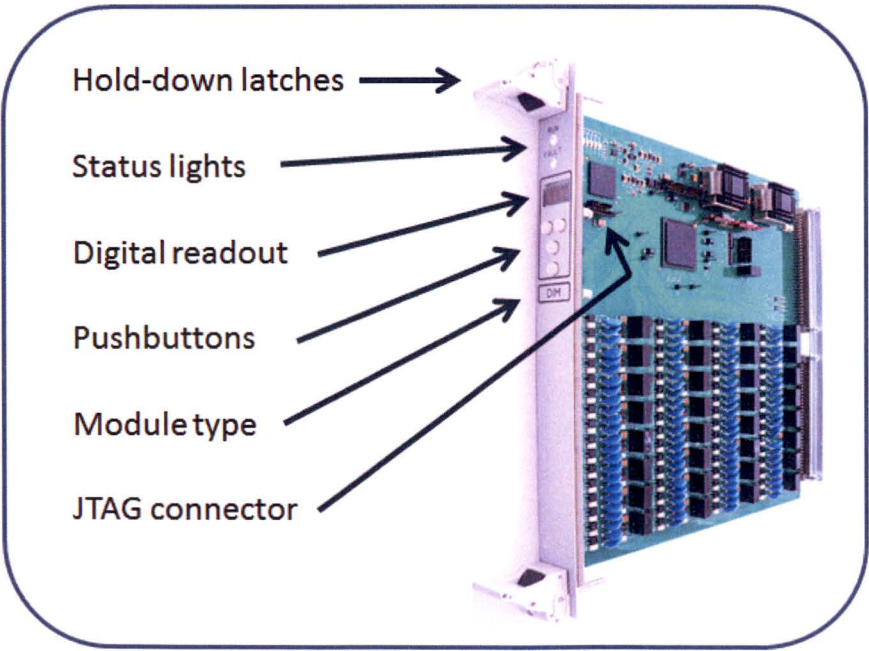


Figure 6-9: Maintenance Features of the RadICS Modules

There are RUN and FAULT status lights on every Module. The RUN light is on when the Module is running normally. The FAULT light illuminates if there is a failure within the RadICS Module detected by



the self-diagnostics (i.e., this does not illuminate if the Platform or Application ED detect a field failure, such as a failed transmitter). The FAULT indication persists until power is removed, so a maintainer can respond to a maintenance order and expect to immediately identify the failed Module.

The digital readout provides two functions: more detailed display of a fault indication, mode status, and status indication used during configuration (downloading of a new electronic design) or during calibration (applicable only to certain Modules). The FAULT readout indication persists until power is removed or until a more serious failure is detected, in which case the more serious failure is displayed.

The pushbuttons allow a maintenance technician to navigate through the menu and to scroll all available fault codes. The pushbuttons also allow entry into CALIBRATION or CONFIGURATION mode (these modes are indistinguishable for safety purposes since the Module is treated as offline in either mode) only if the correct sequence of buttons is pushed in the first 20 seconds following application of power. After this time window, the pushbuttons are only read in CALIBRATION or CONFIGURATION mode.

Each Module carries a Module-type label that the maintenance technician must match against the slot label. This labelling reduces the likelihood of a maintenance error such as mixing up two Modules of different type when re-inserting them. Special coding pegs are provided for I/O Modules to prevent a RadICS Module from being inserted into the wrong slot. In any case the RadICS Platform will detect incorrectly located Modules during the STARTUP Mode self-diagnostic period.

The JTAG and ASPI connectors are not on the faceplate, but rather on the Module PCB, where they cannot be accessed except by removing the Module from the Chassis. Removal of the Module from the Chassis will cause the RadICS Platform to drive all safety outputs to the safe state. Since the ASPI connector (for FPGAs) and the JTAG connector (for CPLDs) are the only means to change the ED configuration of the Module, the system is protected from such errors whether accidental or intentional.

The normal procedure is to power down the RadICS Chassis before performing maintenance; however, all Modules are hot-swappable, so no damage will occur if a Module is extracted or inserted at power. Plant process safety is assured if this sort of action is performed, since any Module that has been removed will be identified as failed. Removal of the LM will force all output Modules to the safe state. When a replacement LM is inserted and completes its startup sequence, the LM will return to normal operation. The LM may be held in RUN (SAFE) mode until the SOR is reset unless it is hard-wired to be automatic. Removal of any I/O Module will also force all output Modules to the safe state.

#### **6.2.5.2 RadICS Module Design Features**

The RadICS Modules are designed with redundant components where needed to permit self-diagnostic tests. Data redundancies are used to permit detection of data corruption with very high probability. Watchdogs are incorporated on every Module. CRCs are used on all communications and safety-critical data. External communications links are all treated as 'black-channel'. Communications ports are monitored and blocked except when specifically required (e.g., tuning). The Modules perform self-diagnostics and either take safe-state action or provide information to the Application Logic for further action.

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The general high-level safety concept for the RadICS Modules employed to meet the target SIL (from IEC 61508) is that, no matter what configuration of Modules is used, an individual Module is designed such that failures that are both dangerous and undetected are limited to less than 10 percent. The RadICS Platform design target is to attempt to meet the same target for each Unit.

The interfaces to Units that are used on more than one Module are standardized. This design strategy maximizes the reuse of proven components and simplifies inter-operation of Modules. The ED of each Module performs self-diagnostics of the Units on the Module. The Units used to compose each Module are identified in Table 6-3.

### Table 6-3: Units Included in RadICS Modules

[illegible]



Unit\Module	LM	DIM	DOM	AIM	AOM	OCM	WAIM	RIM	TIM
Communication Units									
II									
									II <sup>a,c,e</sup>



Figure 6-10 illustrates the typical Module architecture. The key differences between the various Modules are highlighted in the notes below the figure.

[[

]]<sup>a,c,e</sup>

**Figure 6-10: Typical RadICS Module Architecture**

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The purpose of each Unit is described below.

#### **6.2.5.2.1 FPGA Unit**

The FPGA Unit is used to provide input data acquisition, perform the main functions of Module (e.g., data processing, Application Logic execution, etc.), diagnostics, output data conditioning, and data exchange with other Modules (within and beyond the Chassis). The ED of the FPGA is customized to perform the functionality of the specific Module type to meet both functional and integrity requirements specified for the Module.

A CRC check is applied to data transferred from the ASPI during STARTUP mode and a failure of this test prevents the LM from entering RUN mode.

#### **6.2.5.2.2 Clock Unit**

Clock Units are used to generate three separate clocks. Each clock has its own reference quartz oscillator: [[

]]<sup>a,c,e</sup>, as shown in Figure 6-11. [[

]]<sup>a,c,e</sup>



[[

]]<sup>a,c,e</sup>

**Figure 6-11: Data and Signals Exchange Between Different Clock Domains**

Operation of the clock diagnostics is explained in Section 6.8.

#### 6.2.5.2.3 EEPROM Unit

The EEPROM Unit is used for storing different information that is needed for Module operation. The EEPROM Unit performs write/read by frames, data integrity checks, frames numeration checks, and data identification. EEPROM Units are divided into four categories according to the type of data stored:

- [[

]]<sup>a,c,e</sup>

- [[

]]<sup>a,c,e</sup>

- [[

]]<sup>a,c,e</sup>

- [[

]]<sup>a,c,e</sup>

All four types of EEPROM are used in the LM. Only the Service EEPROM is used on the DIM, DOM, AIM, AOM, WAIM, TIM, RIM, and OCM.

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[[

]]<sup>a,c,e</sup>

**6.2.5.2.4 Input Units**

The Input Units are used to provide input data acquisition and directly interact with the I/O Interfaces. The Analog-to-Digital Conversion (ADC) Unit is galvanically isolated, includes active diagnostics and provides receiving one analog input signal that can be multiplied by installing a jumper. The Wide Range Analog-to-Digital Conversion (WADC) Unit is galvanically isolated, includes active diagnostics and provides receiving one analog input signal that can be multiplied by installing a jumper. The Thermocouple-to-Digital Conversion (TDC) Unit is galvanically isolated, includes active diagnostics and provides receiving one thermocouple input signal that can be multiplied by installing a jumper. The Resistance Temperature Detector (RTD) Unit is galvanically isolated, includes active diagnostics and provides receiving an RTD sensor signal by two, three or four-wire connections. The DIU Unit is galvanically isolated, includes active diagnostics, and provides for receiving discrete input signals and monitoring of the transmission path.

[[

]]<sup>a,c,e</sup>

DIU Unit self-diagnostics are performed continuously to check the state of input switch for stuck on/off conditions. Diagnostic test results are reported to the LM and Application ED.

**6.2.5.2.5 Output Units**

The Output Units are used to provide output data conditioning and directly interact with I/O Interfaces. The Discrete Output (DOU) Unit is galvanically isolated, includes active diagnostics, and provides for transmitting discrete output signals and monitoring of the transmission path. The Digital-to-Analog Conversion (DAC) Unit is galvanically isolated, includes active diagnostics, and provides analog output signal conditioning. Safe state of the output Unit is open output discrete signal for DOU and 0 V and 0 mA for DAC.

DOU Unit self-diagnostics are performed continuously to check the state of output switch for stuck on/off conditions. Diagnostic test results are reported to the LM and Application ED.

[[

]]<sup>a,c,e</sup>

**6.2.5.2.6 Safety Override Unit**

The SOR Unit is used to provide a trip into the safe state of Modules by de-energizing the field-effect transistors or DAC circuit (current and voltage) in the Output Units, irrespective of Output Unit control signals from the FPGA Unit. The SOR Unit directly interacts with the Safety Override Interface. SOR

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performs the function to put the Output Units in the safe state independent of FPGA status or commands from it. The SET-SOR switch is used set the SOR. When the SOR is set, all application safety outputs are overridden and placed in the safe state by the RadICS Platform. The RESET-SOR switch is used to reset the SOR provided that no Type I faults have been detected. The SOR allows the maintenance technician to quickly set all safety outputs to the safe state for any reason, and to restore the system when the work is complete. An SOR state signal is provided to the FPGA to check if SOR is set or not when SOR keys are set. The use of the SOR Unit must be integrated with the user-specific actuation logic for energize-to-trip applications.

#### **6.2.5.2.7 Power Supply and Watchdog Unit**

The PSWD Unit is used to provide all Hardware Units with power supply voltages, control the power supply voltages, and perform hardware self-diagnostics of the FPGA Unit. The PSWD Unit is galvanically isolated with the active diagnostics and used for power supply, watchdog heartbeat monitoring, and voltage control with the active diagnostics. The PSWD Unit controls each output voltage, after its conversion, on operating range deviations, as well as executes the FPGA operability control functions. The PSWD Unit receives a heartbeat signal from the FPGA Unit and [[

]]<sup>a,c,e</sup>

Operation of the PSWD Unit is described in Section 6.8.

#### **6.2.5.2.8 Address Unit**

The Address Unit is only used on the LM for providing power to the jumpers placed on the backplane to determine the unique LM identifier within the chassis during Module startup. The LM identifier uniquely identifies LMs in the system while loading information from the Configuration, Tuning, and Application Netlist EEPROMs and for use with the MATS Tuning PC and for reporting various kinds of information to the MATS. [[

]]<sup>a,c,e</sup>

#### **6.2.5.2.9 Active Serial Programming Interface Unit**

The ASPI Unit is one of the standardized interfaces on a Module used for FPGA configuration. The FPGA configuration is read from the ASPI Unit and the FPGA is configured to perform its function as part of the power-up sequence. The ASPI, which includes FLASH memory, is used for writing, storing and reading of FPGA configuration. Access to the FLASH memory is provided only during project-specific manufacturing.

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[[

]]<sup>a,c,e</sup>

**6.2.5.2.10 Indication Board Unit**

The Indication Board Unit is used to indicate the mode and self-diagnostic status of the Module on a local display unit located on the front panel of the Module. The Indication Board Unit can also indicate various kinds of service information for each Module type (e.g., unique LM identifier, identifier, onboard temperature, slot number, etc.). The Indication Board Unit can also be used to transition a Module to CONFIGURATION mode.

**6.2.5.2.11 Synchronous Static Random-Access Memory Unit**

The SSRAM Unit is used for storing different temporary information needed for the Application Logic in the LM. The SSRAM Unit stores Application Logic netlist data, which is read from the AppNetlist EEPROM data in STARTUP and uploaded to SSRAM. Then it will be read each Work Cycle from SSRAM and processed.

[[

]]<sup>a,c,e</sup>

**6.2.5.2.12 Communication Units**

The Communication Units are used to provide the data and data exchange within and between Chassis. The Communication Units use different protocols: RPP, RUP, and RS-232 based Protocol (RS-232). The LAN Unit is used for communication with peripheral devices (e.g., MATS). The OPTO Unit is used for optical transceiving with the same Unit in another Module of the same type. The LVDS Unit is used for point-to-point communication between two Modules within one Chassis. The RS-232/485 Unit is used for one-way communication with peripheral devices.

The use of the communication units is described in Section 6.3.2.

**6.2.5.2.13 Real Time Unit**

The Real Time Unit is used for receiving real-time data from an externally supplied time input not a part of the RadICS Platform. The Real Time Unit has the capability to duplicate and store the externally supplied time. In case the externally supplied time input is lost, the Real Time Unit can continue to supply a time input to the FPGA Unit.

The Real Time Unit does not affect any safety function performed by the LM. The time signal is not used by any safety function. The Real Time Unit uses a dedicated data format that is distinct from formats used by safety critical logic and data so that safety logic would detect corruption of safety data by the time signal. The time signal is only used for the purpose of placing time stamps on the one-way data communications to the MATS. The Real Time Unit is galvanically isolated.



### **6.2.5.3 Ventilation Module**

The RadICS Platform has a Ventilation Module (VM) that is used for driving chassis fans. The VM performs only one function (i.e., driving fans) and does not exchange data with other RadICS Modules. The VM is controlled by a CPLD that processes data received from the fans (e.g., indication of voltage and speed) and external devices (e.g., control switches and alarm indications). The VM can detect fan failures; however, this capability is not critical, since unexpected stoppage of fans will cause chassis internal temperatures to increase, which are detected by other monitoring features, as described in Sections 6.2.5.2.7 and 6.8.

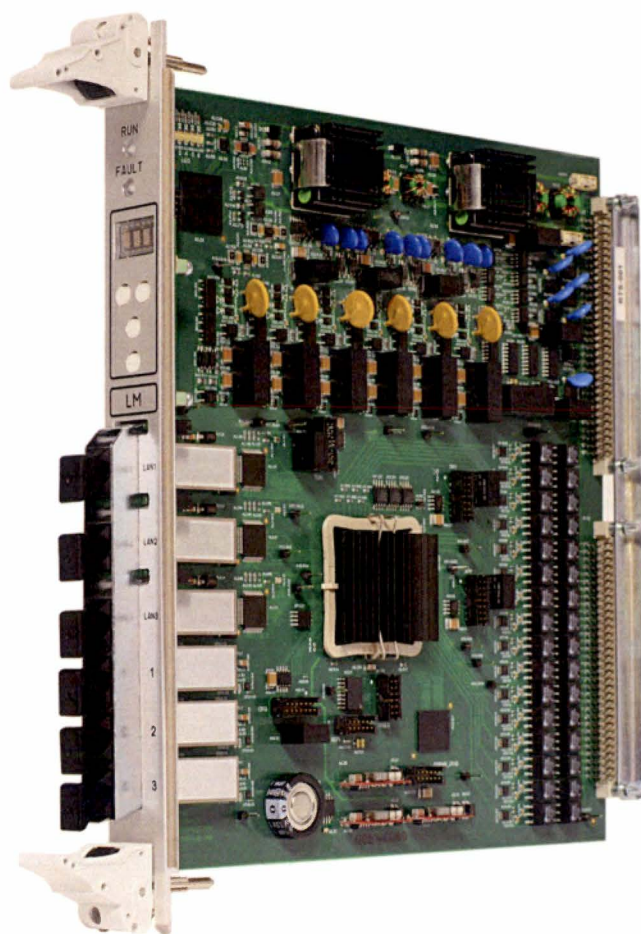
## **6.2.6 Hardware Module Specifications**

The RadICS Hardware Modules are described in the following sections, which describe the technical specifications, operation, and failure detection and prevention for each Module.

### **6.2.6.1 Logic Module**

The LM is used for data exchange with Modules in Chassis and Units within Module and execution of Application Logic specified by the end user's functional requirements.





### LM Product Highlights

- Dedicated FPGA chip for user configurable control logic
- Robust self-diagnostics ensure higher reliability and early fault detection with safety-focused fault management
- Segregation of application logic, self-diagnostics, and watchdog functions assures safety-critical functionality
- Diverse watchdog heartbeat monitoring and extensive functionally diverse self-diagnostics
- 14 LVDS full duplex lines for communication with OCM and I/O Modules
- 3 galvanic-isolated discrete inputs (2 available, 1 reserved)
- 6 fast discrete outputs with embedded diagnostics of the outputs state
- 3 fiber optical lines for internal system communications
- 1 input for MATS Tuning PC programming access key signal
- 3 Fast Ethernet (100 BASE-FX) optical communication lines
- Hot swappable

#### 6.2.6.1.1 LM Technical Specifications

The technical specifications for the LM are:

FPGA capacity	capacity to handle > 500 application blocks
Memory	8 megabit (FPGA internal) 4*2 megabit (four external EEPROMs) 2 megabit (external SSRAM)
Discrete inputs	24 VDC, 10 milliamps maximum, Form A “dry” contact with galvanic isolation between inputs
Discrete inputs overvoltage protection	up to 150 VDC continuous
Access key signal input	discrete signal (24 VDC, 0 to 10 milliamp) receiver with optic-isolation



Discrete outputs	“dry” contact: up to 48 V, 0.2 A (AC/DC), galvanic-isolated by optic-relays
Discrete outputs overvoltage protection	up to +60 VDC/VAC continuous
Communication ports	three fiber optic communication ports for MATS support with LAN1 port assigned to the Tuning function and LAN2 and LAN3 ports are assigned to the Monitoring function three for fiber optic RPP cross division interfaces
Application logic processing cycle	up to 2.5 milliseconds for control logic up to 2.5 milliseconds for I/O Modules signals/data processing
Diagnostic data exchange cycle	up to 5 milliseconds
Ethernet / protocol	100 BASE-FX IP/UDP
LVDS line speed	100 Megabit/second
LVDS line protocol	proprietary protocol with integrity checking (CRC), galvanic-isolated Tx / Rx
Fiber optical lines speed	100 Megabit/second
Self-diagnostic functions	diverse watchdog unit, hardware error detection, checksum analysis, active diagnostics with internal fault detection, functionally diverse continuous self-diagnostic tests, power supply fault detection
Power supply / consumption	2 independent inputs – 24 (20.4 – 28.8) VDC / 0.92 A ( $\pm 0.15$ A)
Indications	2 status LED indicators (RUN/FAULT) 4-character dot matrix symbol-indicator for current operational mode, service info, and providing errors codes
Operating temperature	4.4 to 60 °C (40 to 140 °F)
Operating humidity	10 to 90% relative humidity, non-condensing

The functional diagram of the LM is shown in Figure 6-12.



[[

]]<sup>a,c,e</sup>

**Figure 6-12: Functional Diagram of the LM**

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#### 6.2.6.1.2 LM Operation

The LM operation requirements are to:

1. Exchange data with other Modules within the Chassis and with LMs in other Chassis (e.g., channel voting),
2. Process and execute Application Logic specified by the end user,
3. Transmit RadICS Platform diagnostic and Application ED processing data to the MATS, and
4. Provide means to change tuning values.

The LM operating modes and possible modes transitions are shown in Figure 6-13.

[[

]]<sup>a,c,e</sup>

**Figure 6-13: LM Mode Transition Diagram**

In the POWERED-OFF mode the LM does not perform any functions. All Hardware Units are de-energized; all outputs are in the safe state; no data transmitted or received; and configuration and tuning changes are not allowed. The LM can transition to the STARTUP mode if the Module is energized.

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In STARTUP Mode, the LM performs the following functions:

1. [[

]]<sup>a,c,e</sup>

All functions of RUN mode are then performed, but a [[

]]<sup>a,c,e</sup>. In the [[

]]<sup>a,c,e</sup>. After [[

]]<sup>a,c,e</sup>, the LM will transition into

[[

]]<sup>a,c,e</sup> The LM can

transition to the [[

]]<sup>a,c,e</sup> if the Module is de-energized.

In RUN (SAFE) mode the LM performs the following functions:

1. [[

]]<sup>a,c,e</sup>

The LM can transition to the POWERED-OFF mode if the Module is de-energized. The LM can transition to the [[

]]<sup>a,c,e</sup>.

The LM will transition to the TUNING Mode if the SOR is set, Application Logic is setting SOR, and TUNING key and ARMING key are present. The LM will transition into [[

]]<sup>a,c,e</sup>. The LM will also transition into [[

]]<sup>a,c,e</sup>



In RUN Mode, the LM performs the following functions:

1. All Hardware Units are energized [[

]]<sup>a,c,e</sup>

3. Module performs the following sequence of actions:

- a. Input Data Receiving Phase:

- [[

]]<sup>a,c,e</sup>

- b. Application Logic Processing and Configuration Phase:

- [[

]]<sup>a,c,e</sup>

- c. Output Data Transmission Phase:

- [[

]]<sup>a,c,e</sup>

- d. Switch Time Phase:

- [[

]]<sup>a,c,e</sup>

4. Performed periodically or constantly during all processes described above:

a. [[

]]<sup>a,c,e</sup>

The LM can transition to the POWERED-OFF mode if the Module is de-energized. The LM will transition to the [[

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]]<sup>a,c,e</sup>. The LM will transition to the [[  
]]<sup>a,c,e</sup> are present. The LM will transition into [[  
]]<sup>a,c,e</sup>

In TUNING Mode, the LM performs the following functions:

1. [[

]]<sup>a,c,e</sup>

4. The following actions are performed periodically or constantly during all processes described above:  
a. [[

]]<sup>a,c,e</sup>

5. MATS Tuning PC tests the password.

The LM can transition to the POWERED-OFF mode if the Module is de-energized. The LM will transition to the [[

]]<sup>a,c,e</sup>. The LM will transition into [[  
]]<sup>a,c,e</sup>

In FAULTED Mode, the LM performs the following functions:

1. [[



]]<sup>a,c,e</sup>

The LM in the [[

]]<sup>a,c,e</sup>.

In CONFIGURATION Mode, the LM performs the following functions:

1. [[

]]<sup>a,c,e</sup>

In CONFIGURATION Mode, the LM can transition to the POWERED-OFF mode if the Module is de-energized. The LM will transition into [[

]]<sup>a,c,e</sup>

#### 6.2.6.1.3 LM Failure Detection and Prevention

The LM is designed to detect the following failures that are potentially dangerous unless revealed by self-diagnostics and reported to the Application Logic:

- [[

]]<sup>a,c,e</sup>

The safety concept for the LM includes the following features:

- [[



- $\text{]]}^{a,c,e}$ , as described in Section 6.4.2.
- $\text{]]}^{a,c,e}$ , as described in Section 6.4.
- $\text{]]}^{a,c,e}$ , as described in Section 6.4.3.

$\text{]]}^{a,c,e}$ , as described in Section 6.4.4.1.



- [[

,c,e

When in the STARTUP and RUN modes, the LM sets its state and the state of the RadICS Platform as a whole, according to the LM self-diagnostics and the diagnostics results reported by the other modules in the chassis, as noted below. The LM also reports these conditions via the IBU and the MATS.

Module type	Fault type I	Fault type II	Fault type III
Input Modules (AIM, DIM, WAIM, TIM, RIM, and OCM)	[[ ]] <sup>a,c,e</sup>	[[ ]] <sup>a,c,e</sup>	[[ ]] <sup>a,c,e</sup>
Output Modules (DOM, AOM)	[[ ]] <sup>a,c,e</sup>	[[ ]] <sup>a,c,e</sup>	[[ ]] <sup>a,c,e</sup>
LM	[[ ]] <sup>a,c,e</sup>	[[ ]] <sup>a,c,e</sup>	[[ ]] <sup>a,c,e</sup>

† DBAL = Decided by Application Logic (i.e., Application Logic specifies how to handle faults of I/O Modules).

Once an error condition has been detected, the error state continues to be reported on the Indication Board Unit and via the MATS until either power is removed or a higher-level error is detected.

The following actions are taken in response failures locally on LM and on other Modules:

1. Removal of Module:
  - a. LM outputs are disconnected from the field
  - b. I/O Modules detect loss of communication from the LM
2. PSWD detects power supply or FPGA CRAM failure
  - a. PSWD cuts power to all units except itself and IBU
  - b. IBU shows failure code
  - c. LM goes to FAULTED Mode and trips all outputs to safe state
  - d. I/O Modules detect loss of communication from the LM
3. Communication fails – I/O Modules do not receive commands from LM
  - a. I/O Modules detect loss of communication from LM and output Modules go to RUN(SAFE) Mode and sets all outputs to safe state redundantly (i.e., the SOR is set and all individual channels are commanded to the safe output value)
  - b. IBU shows failure code
4. Communication fails – LM does not receive response from an I/O Module
  - a. LM detects loss of communication from the Module
  - b. LM sends flag to trip all output Modules to safe state
  - c. All output Modules detect this flag and redundantly set all output channels to safe state (i.e., the SOR is set and all individual channels are commanded to the safe output value)
  - d. Application Logic may redundantly detect this via Module state signals and substitute a safe state value for all output channels
  - e. LM sets all data from the Module to zero value
5. Communication fails – loss of LAN connection
  - a. LM detects loss of connection
  - b. IBU shows failure code

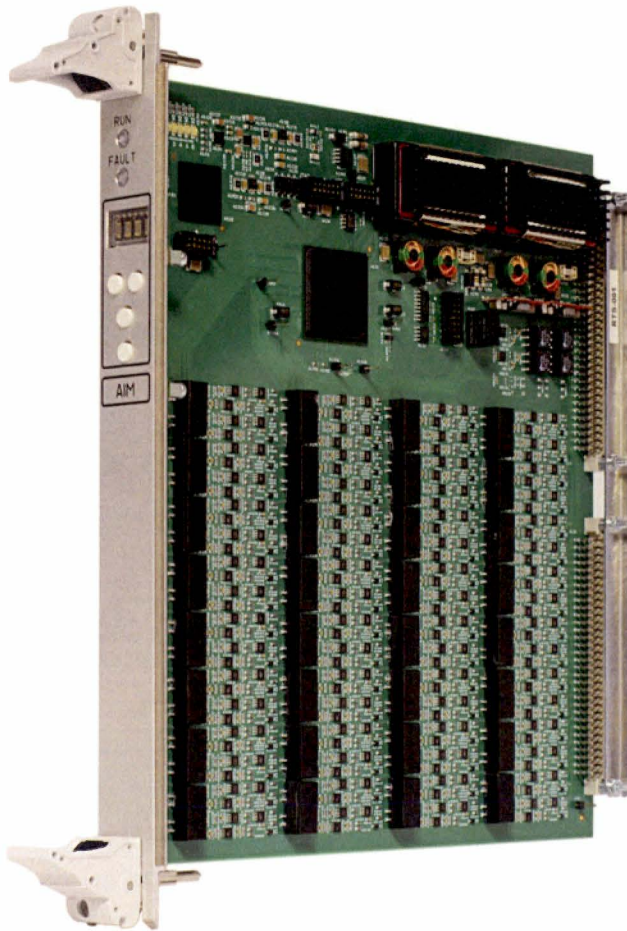


6. LM reports high-level failure (e.g., CRC check error) of FPGA
  - a. FPGA detects the failure and stops updating the heartbeat signal to the PSWD
  - b. PSWD cuts power to all Units except itself and IBU
  - c. IBU shows failure code
  - d. I/O Modules detect loss of communication from the LM
7. LM reports Type I faults during Application Logic execution
  - a. FPGA detects the failure and stops updating the heartbeat signal to the PSWD
  - b. PSWD cuts power to all Units except itself and IBU
  - c. IBU shows failure code
  - d. I/O Modules detect loss of communication from the module

#### **6.2.6.2     *Analog Inputs Module***

The AIM is used for the acquisition of analog signals (0 V to +5.1 V) and the conversion to engineering units. The AIM has 32 independent input channels.





### AIM Product Highlights

- High density 32 channel analog inputs with built-in hardware redundancy and self-diagnostics for highly reliable operation, filtering, calibration, and random hardware failure detection
- Robust self-diagnostics ensure higher reliability and early fault detection with safety-focused fault management
- Segregation of input processing, self-diagnostics, and watchdog functions assure safety-critical functionality
- 18-bit analog/digital (A/D) conversion in each analog input channel
- 2 LVDS full duplex lines (redundant diagnostic and control data exchange)
- Diverse watchdog heartbeat monitoring and extensive functionally diverse self-diagnostics
- Built-in calibration
- Hot swappable

#### 6.2.6.2.1 AIM Technical Specifications

The technical specifications for the AIM are:

Input analog signal range	0 to +5.1 V (0 to 20 milliamp using external resistor installed in connection/junction box) Differential input impedance: not less than 1 MΩ.
A/D conversion resolution	18 bits / 400 kilo samples per second (kSPS)
Common mode rejection ratio	> 86 dB
Overall accuracy	0.04% of full scale for 0 to +5.1 V (at 25 °C) 0.04% of full scale in current mode (at 25 °C)





Input channel isolation	all input channels are galvanic-isolated up to 250 V <sub>RMS</sub> AC or 250 VDC field-to-Chassis and channel-to-channel
Overvoltage protection	±60 VAC/VDC continuous (using external protection elements installed in Chassis)
Information package exchange cycle	5 milliseconds
Diagnostic package exchange cycle	5 milliseconds
LVDS line speed	100 Megabit/second
LVDS line protocol	proprietary protocol with integrity checking (CRC), galvanic-isolated Tx / Rx
Self-diagnostic functions	diverse watchdog unit, hardware error detection, checksum analysis, active diagnostics with internal fault detection, functionally diverse continuous self-diagnostic tests, power supply fault detection
Power supply / consumption	2 independent inputs – 24 (20.4 – 28.8) VDC / 0.85 A (± 0.15 A)
Indications	2 status LED indicators (RUN/FAULT); 4-character dot matrix symbol-indicator for providing current operational mode, service information, and errors codes
Operating temperature	4.4 to 60 °C (40 to 140 °F)
Operating humidity	10 to 90% relative humidity, non-condensing

The functional diagram of the AIM is shown in Figure 6-14.



[[

]]<sup>a,c,e</sup>

**Figure 6-14: Functional Diagram of the AIM**

#### **6.2.6.2.2 AIM Operation**

The AIM operation requirements are to:

1. Acquire analog signals from field sensors:
2. Filter, scale the analog signals, and convert to floating point format; and
3. Perform data exchange with the LM.

The AIM operating modes and possible modes transitions are shown in Figure 6-15.

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[[

]]<sup>a,c,e</sup>

Figure 6-15: AIM Mode Transition Diagram

In the POWERED-OFF mode the AIM does not perform any functions. All Hardware Units are de-energized, no data transmitted or received, configuration changes are not allowed. The AIM can transition to the STARTUP mode if the Module is energized.

In STARTUP Mode, the AIM performs the following functions:

1. [[

]]<sup>a,c,e</sup>

All functions of RUN mode are then performed, but a [[  
]]<sup>a,c,e</sup>. In the [[  
]]<sup>a,c,e</sup> After [[  
]]<sup>a,c,e</sup>, the AIM will transition into RUN mode or into [[  
]]<sup>a,c,e</sup>



In RUN Mode, the AIM performs the following functions:

1. All Hardware Units are energized
2. [[ ]]<sup>a,c,e</sup>
3. Module performs two [[ ]]<sup>a,c,e</sup> of actions:

a. Data Processing:

- Input data acquisition from ADC Units
- Scaling and filtering of input data
- Comparison of processed input data

b. Data Transmission/Receiving:

- Data transmission
  - [[ ]]

- Data receiving
  - [[ ]]

4. Performed periodically or constantly during all processes described above:
  - a. [[ ]]

The AIM can transition to the POWERED-OFF mode if the Module is de-energized. The AIM will transition into [[ ]]<sup>a,c,e</sup>

In FAULTED Mode, the AIM performs the following functions:

1. [[ ]]

]]<sup>a,c,e</sup>

The AIM in the [[ ]]<sup>a,c,e</sup>.

In CONFIGURATION Mode, the AIM performs the following functions:

1. [[ ]]



]]<sup>a,c,e</sup>

In CONFIGURATION Mode, the AIM can transition to the [[  
]]<sup>a,c,e</sup>. The AIM will transition into [[  
]]<sup>a,c,e</sup>

6.2.6.2.3 AIM Failure Detection and Prevention

The AIM is designed to detect deviations from the specified accuracy, execution of analog-to-digital conversion, or response time for the signals transmitted to LM. The data with detected errors are flagged as invalid. The safety concept for the AIM includes the following features:

- [[  
  
]]<sup>a,c,e</sup>, as described in Section 6.4.2.
- [[  
  
]]<sup>a,c,e</sup>, as described in Section 6.4.
- [[  
  
]]<sup>a,c,e</sup>, as described in Section 6.4.3.

]]<sup>a,c,e</sup>

Once an error condition has been detected, the error state continues to be reported on the Indication Board Unit and via the MATS until either power is removed or a higher-level error is detected.

The following actions are taken in response failures locally on AIM and on other Modules:

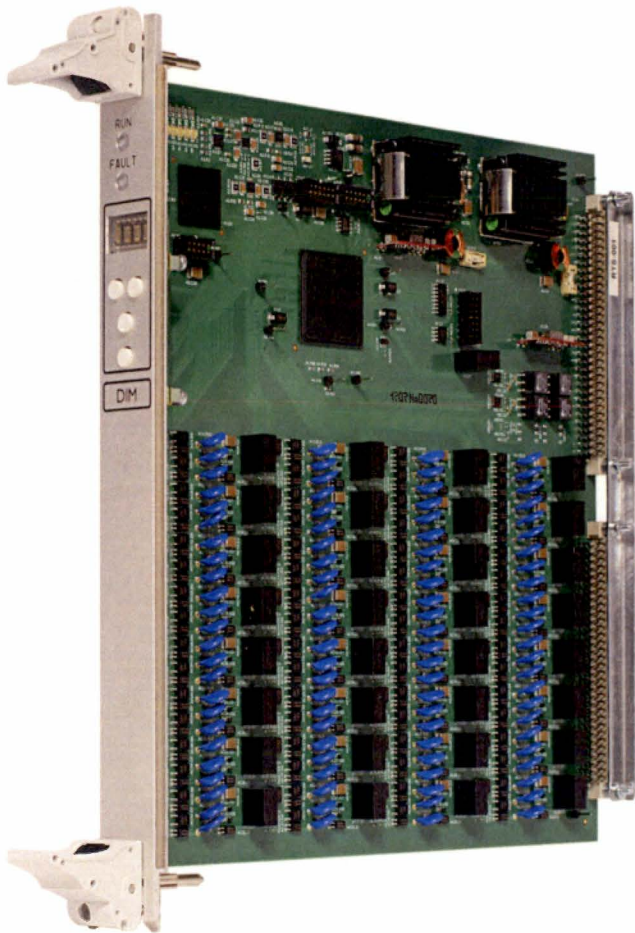


1. Removal of Module:
  - a. AIM inputs are disconnected from the field
  - b. LM detect loss of communication from the AIM
2. PSWD detects power supply or FPGA CRAM failure
  - a. PSWD cuts power to all units except itself and IBU
  - b. IBU shows failure code
  - c. LM detects loss of communication from the AIM
3. Communication fails – AIM does not receive commands from LM
  - a. AIM detect loss of communication from LM
  - b. IBU shows failure code
  - c. LM detects loss of communication from the AIM
4. Communication fails – LM does not receive response from AIM
  - a. LM detects loss of communication from the AIM
  - b. LM sends flag to trip all output Modules to safe state
  - c. All output Modules detect this flag and redundantly set all output channels to safe state (i.e., the SOR is set and all individual channels are commanded to the safe output value)
  - d. Application Logic may redundantly detect this via Module state signals and substitute a safe state value for all output channels
5. AIM reports high-level failure (e.g., CRC check error) of FPGA
  - a. FPGA detects the failure and stops updating the heartbeat signal to the PSWD
  - b. PSWD cuts power to all Units except itself and IBU
  - c. IBU shows failure code
  - d. LM detects loss of communication from the AIM
6. AIM reports channel-level failure
  - a. AIM sets status flag for the Application Logic to detect
  - b. IBU shows failure code
  - c. Application Logic detects failure via input signal bus and provide appropriate for the Application Logic design actions

### **6.2.6.3 Discrete Inputs Module**

The DIM is used for the acquisition of discrete dry contact signals via DIU Units and transmission to LM via LVDS Transceiver Unit. The DIM has 32 independent input channels.





**DIM Product Highlights**

- High density 32 channel discrete dry-contact inputs with built-in hardware redundancy and line integrity checks for hardware failure detection  
Robust self-diagnostics ensure higher reliability and early fault detection with safety-focused fault management.
- Segregation of input processing, self-diagnostics, and watchdog functions assures safety-critical functionality.
- Independent FPGA for discrete input processing, self-diagnostics, and fail-safe functional behavior
- 2 LVDS (redundant diagnostic and control data exchange)
- Diverse watchdog heartbeat monitoring and extensive functionally diverse self-diagnostics
- Hot swappable

**6.2.6.3.1 DIM Technical Specifications**

The technical specifications for the DIM are:

Internal power supply for each independent discrete input	24 VDC / 10 milliamps maximum (Form A “dry” contact)
Input channel isolation	all input channels are galvanic-isolated up to 250 V <sub>RMS</sub> AC or 250 VDC field-to-Chassis and channel-to-channel
Input channel isolation method	optic relay
Overvoltage protection	150 VDC continuous (using external protection elements installed in Chassis)
Information package exchange cycle	5 milliseconds



Diagnostic package exchange cycle	5 milliseconds
LVDS line speed	100 Megabit/second
LVDS line protocol	proprietary protocol with integrity checking (CRC), galvanic-isolated Tx / Rx
Self-diagnostic functions	diverse watchdog unit, hardware error detection, checksum analysis, active diagnostics with internal fault detection, functionally diverse continuous self-diagnostic tests, power supply fault detection
Power supply / consumption	2 independent inputs – 24 (20.4 – 28.8) VDC / 0.77 A ( $\pm$ 0.15 A)
Indications	2 status LED indicators (RUN/FAULT); 4-character dot matrix symbol-indicator for providing current operational mode, service information, and errors codes
Operating temperature	4.4 to 60 °C (40 to 140 °F)
Operating humidity	10 to 90% relative humidity, non-condensing

The functional diagram of the DIM is shown in Figure 6-16.



[[

]]<sup>a,c,e</sup>

**Figure 6-16: Functional Diagram of the DIM**

#### **6.2.6.3.2 DIM Operation**

The DIM operation requirements are to:

1. Acquire discrete dry contact signals and
2. Perform data exchange with the LM.

The DIM operating modes and possible modes transitions are shown in Figure 6-17.

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[[

]]<sup>a,c,e</sup>

**Figure 6-17: DIM Mode Transition Diagram**

In the POWERED-OFF mode the DIM does not perform any functions. All Hardware Units are de-energized, no data transmitted or received, configuration changes are not allowed. The DIM can transition to the STARTUP mode if the Module is energized.

In STARTUP Mode, the DIM performs the following functions:

1. [[

]]<sup>a,c,e</sup>

All functions of RUN mode are then performed, but a [[

]]<sup>a,c,e</sup>. In the [[]]<sup>a,c,e</sup>. After [[]]<sup>a,c,e</sup>, the DIM will transition into RUN mode [[]]<sup>a,c,e</sup>

In RUN Mode, the DIM performs the following functions:

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1. All Hardware Units are energized.
2. [[ ]]<sup>a,c,e</sup>
3. Module performs the following sequence of actions:
  - a. Data Processing
    - Input data acquisition [[ ]]<sup>a,c,e</sup>
  - b. Data Transmission/Receiving:
    - Data transmission
      - [[ ]]

- Data receiving
  - [[ ]]

4. Performed periodically or constantly during all processes described above:
  - a. [[ ]]

]]<sup>a,c,e</sup>

The DIM can transition to the POWERED-OFF mode if the Module is de-energized. The DIM will transition into [[ ]]

In FAULTED Mode, the DIM performs the following functions:

1. [[ ]]

]]<sup>a,c,e</sup>

The DIM in the [[ ]]

In CONFIGURATION Mode, the DIM performs the following functions:

1. [[ ]]

]]<sup>a,c,e</sup>





In CONFIGURATION Mode, the DIM can transition to the POWERED-OFF mode if the Module is de-energized. The DIM will transition into [[

]]<sup>a,c,e</sup>

### 6.2.6.3.3 DIM Failure Detection and Prevention

The DIM is designed to detect input data updates that are slower than the specified time or data corruption for the signals transmitted to LM. The safety concept for the DIM includes the following features:

- [[
- ]]<sup>a,c,e</sup>, as described in Section 6.4.2.
- [[ ]]<sup>a,c,e</sup>, as described in Section 6.2.5.2.4.
- [[ ]]<sup>a,c,e</sup>, as described in Section 6.4.
- [[

- ]]<sup>a,c,e</sup>, as described in Section 6.4.3.
- [[

]]<sup>a,c,e</sup>

Once an error condition has been detected, the error state continues to be reported on the Indication Board Unit and via the MATS until either power is removed or a higher-level error is detected.

The following actions are taken in response failures locally on DIM and on other Modules:

1. Removal of Module:
  - a. DIM inputs are disconnected from the field
  - b. LM detect loss of communication from the DIM
2. PSWD detects power supply or FPGA CRAM failure
  - a. PSWD cuts power to all units except itself and IBU
  - b. IBU shows failure code

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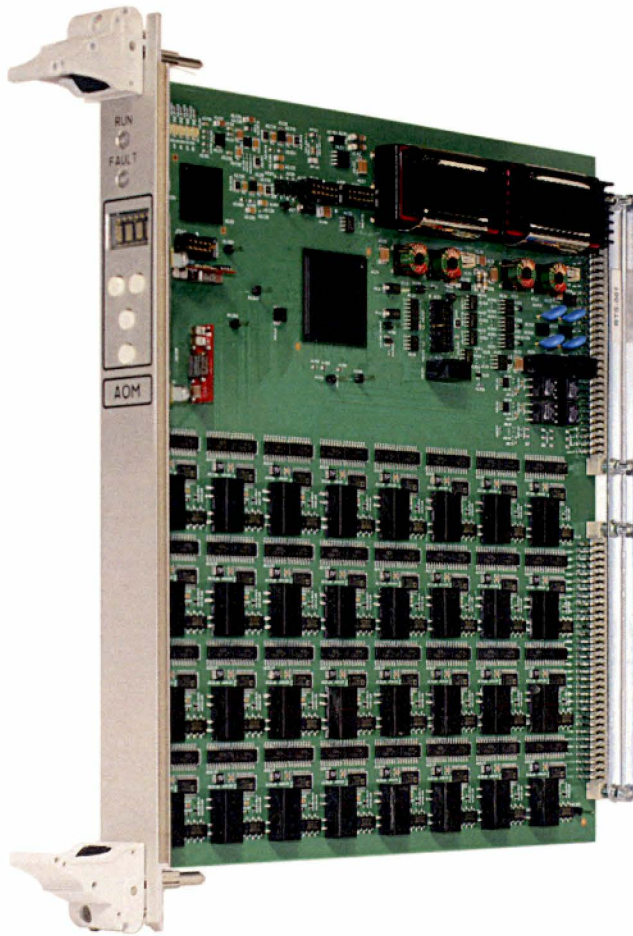




- c. LM detects loss of communication from the DIM
- 3. Communication fails – DIM does not receive commands from LM
  - a. DIM detect loss of communication from LM
  - b. IBU shows failure code
  - c. LM detects loss of communication from the DIM
- 4. Communication fails – LM does not receive response from DIM
  - a. LM detects loss of communication from the DIM
  - b. LM sends flag to trip all output Modules to safe state
  - c. All output Modules detect this flag and redundantly set all output channels to safe state (i.e., the SOR is set and all individual channels are commanded to the safe output value)
  - d. Application Logic may redundantly detect this via Module state signals and substitute a safe state value for all output channels
- 5. DIM reports high-level failure (e.g., CRC check error) of FPGA
  - a. FPGA detects the failure and stops updating the heartbeat signal to the PSWD
  - b. PSWD cuts power to all Units except itself and IBU
  - c. IBU shows failure code
  - d. LM detects loss of communication from the DIM
- 6. DIM reports channel-level failure
  - a. DIM sets status flag for the Application Logic to detect
  - b. IBU shows failure code
  - c. Application Logic detects failure via input signal bus and provide appropriate for the Application Logic design actions

#### **6.2.6.4    *Analog Outputs Module***

The AOM is used for the conditioning of analog output signals and data exchange with LMs. The AOM has 32 independent output channels.



### AOM Product Highlights

- High density 32 channel analog outputs designed to detect conditioned output signals that exceed accuracy and response time diagnostic tolerances.
- Independent FPGA for analog output processing, self-diagnostics, and fail-safe functional behavior
- Robust self-diagnostics ensure higher reliability and early fault detection with safety-focused fault management.
- Segregation of output processing, self-diagnostics, and watchdog functions assures safety-critical functionality
- 16-bit analog/digital (A/D) conversion in each channel
- 2 LVDS full duplex lines (redundant diagnostic and control data exchange)
- Diverse watchdog heartbeat monitoring and extensive functionally diverse self-diagnostics
- Built-in calibration
- Hot swappable

#### 6.2.6.4.1 AOM Technical Specifications

The technical specifications for the AOM are:

Output range	0 to +5 V / 4 to 20 milliamp / $\pm 10$ V / 0 to 5 milliamps
D/A conversion resolution	16 bits
Output signal value accuracy	0.04% of full scale (at 25 °C)
Maximum output load	up to 1.2 kilo ohm (k $\Omega$ ) for current output minimum of 1 k $\Omega$ for voltage output
Internal power supply on each output channel	$\pm 15$ V / $\pm 35$ milliamp



Output analog channel isolation	all output channels are galvanic-isolated up to 250 V <sub>RMS</sub> AC or 250 VDC field-to-Chassis and channel-to-channel
Overvoltage protection	±60 VAC/VDC continuous (using external protection elements installed in Chassis)
Output signal update cycle	5 milliseconds
Diagnostic package exchange cycle	up to 250 milliseconds
LVDS line speed	100 Megabit/second
LVDS line protocol	proprietary protocol with integrity checking (CRC), galvanic-isolated Tx / Rx
Self-diagnostic functions	diverse watchdog unit, hardware error detection, checksum analysis, active diagnostics with internal fault detection, functionally diverse continuous self-diagnostic tests, power supply fault detection
Power supply / consumption	2 independent inputs – 24 (20.4 – 28.8) VDC / 1.42 A (± 0.15 A)
Indications	2 status LED indicators (RUN/FAULT); 4-character dot matrix symbol-indicator for providing current operational mode, service information, and errors codes
Operating temperature	4.4 to 60 °C (40 to 140 °F)
Operating humidity	10 to 90% relative humidity, non-condensing

The functional diagram of the AOM is shown in Figure 6-18.



[[

]]<sup>a,c,e</sup>

**Figure 6-18: Functional Diagram of the AOM**

#### **6.2.6.4.2 AOM Operation**

The AOM operation requirements are to:

1. Perform data exchange with the LM,
2. Process data received from LM,
3. Condition control signals for DAC Units, and
4. Send feedback in floating point format.

The AOM operating modes and possible modes transitions are shown in Figure 6-19.

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[[

]]<sup>a,c,e</sup>

Figure 6-19: AOM Mode Transition Diagram

In the POWERED-OFF mode the AOM does not perform any functions. All Hardware Units are de-energized, no data transmitted or received, configuration changes are not allowed. The AOM can transition to the STARTUP mode if the Module is energized.

In STARTUP Mode, the AOM performs the following functions:

- 1. [[

]]<sup>a,c,e</sup>

All functions of RUN mode are then performed, but a [[  
]]<sup>a,c,e</sup>. The AOM can transition to the [[



]]<sup>a,c,e</sup>. In the [[  
 ]]<sup>a,c,e</sup>. After [[  
 ]]<sup>a,c,e</sup>, the AOM will transition into [[  
 ]]<sup>a,c,e</sup>

In RUN (SAFE) mode the AOM performs the following functions:

1. All HW Units are energized [[

]]<sup>a,c,e</sup>

The AOM can transition to the POWERED-OFF mode if the Module is de-energized. The AOM can transition to the RUN mode [[

]]<sup>a,c,e</sup>. The AOM will transition into [[  
 ]]<sup>a,c,e</sup>

In RUN Mode, the AOM performs the following functions:

1. All Hardware Units are energized.
2. [[  
 ]]<sup>a,c,e</sup>
3. Module performs the following sequence of actions:
  - a. Data Processing:
    - [[

]]<sup>a,c,e</sup>

- b. Data Transmission/Receiving:
  - Data transmission
    - [[

]]<sup>a,c,e</sup>

- Data receiving
  - [[

]]<sup>a,c,e</sup>

4. Performed periodically or constantly during all processes described above:
  - a. [[

]]<sup>a,c,e</sup>





The AOM can transition to the POWERED-OFF mode if the Module is de-energized. The AOM can transition to the [[

]]<sup>a,c,e</sup>. The AOM will transition into [[  
]]<sup>a,c,e</sup>

In FAULTED Mode, the AOM performs the following functions:

1. [[

]]<sup>a,c,e</sup>

The AOM in the [[

]]<sup>a,c,e</sup>.

In CONFIGURATION Mode, the AOM performs the following functions:

1. [[

]]<sup>a,c,e</sup>

In CONFIGURATION Mode, the AOM can transition to the POWERED-OFF mode if the Module is de-energized. The AOM will transition into [[

]]<sup>a,c,e</sup>

#### 6.2.6.4.3 AOM Failure Detection and Prevention

The AOM is designed to detect deviations between the signals received from LM and conditioned output signals that exceed the specified accuracy or an output data conditioning process that exceeds the specified response time. The safety concept for the AOM includes the following features:

- [[

]]<sup>a,c,e</sup>, as described in Section 6.4.2.

- [[

]]<sup>a,c,e</sup>, as described in Section 6.4.2.

- [[

]]<sup>a,c,e</sup>, as described in Section 6.4.

- [[



- ]]<sup>a,c,e</sup>, as described in Section 6.4.3.

]]<sup>a,c,e</sup>

Once an error condition has been detected, the error state continues to be reported on the Indication Board Unit and via the MATS until either power is removed or a higher-level error is detected.

The following actions are taken in response failures locally on AOM and on other Modules:

1. Removal of Module:
  - a. AOM inputs are disconnected from the field
  - b. LM detect loss of communication from the AOM
2. PSWD detects power supply or FPGA CRAM failure
  - a. PSWD cuts power to all units except itself and IBU
  - b. IBU shows failure code
  - c. AOM goes to FAULTED Mode and trip all outputs to safe state
  - d. LM detects loss of communication from the AOM
3. Communication fails – AOM does not receive commands from LM
  - a. AOM detect loss of communication from LM and goes to RUN(SAFE) Mode and sets all outputs to safe state redundantly (i.e., the SOR is set and all individual channels are commanded to the safe output value)
  - b. IBU shows failure code
  - c. LM detects loss of communication from the AOM
4. Communication fails – LM does not receive response from AOM
  - a. LM detects loss of communication from the AOM
  - b. LM sends flag to trip all output Modules to safe state
  - c. All output Modules detect this flag and redundantly set all output channels to safe state (i.e., the SOR is set and all individual channels are commanded to the safe output value)
  - d. Application Logic may redundantly detect this via Module state signals and substitute a safe state value for all output channels

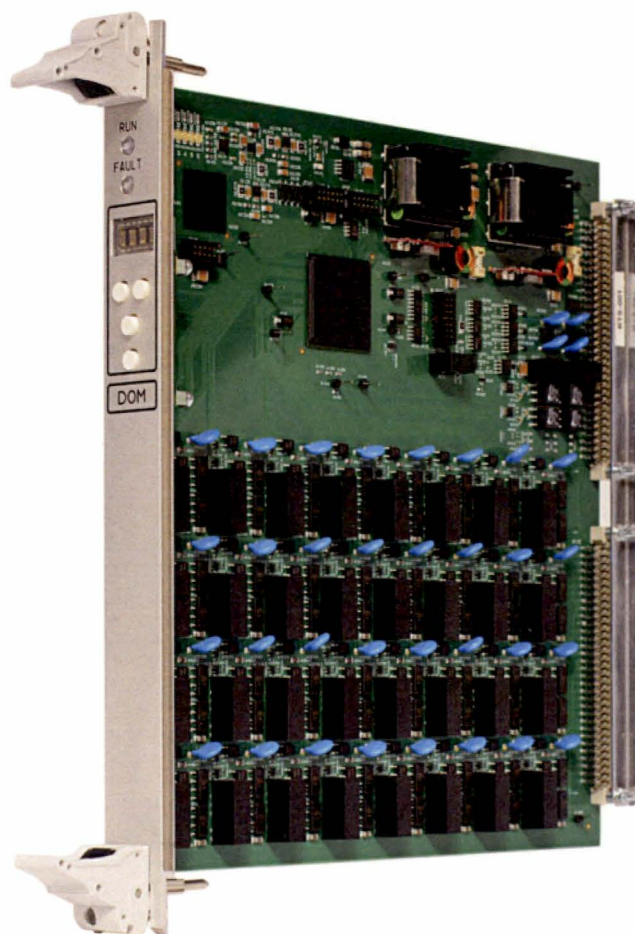
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5. AOM reports high-level failure (e.g., CRC check error) of FPGA
  - a. FPGA detects the failure and stops updating the heartbeat signal to the PSWD
  - b. PSWD cuts power to all Units except itself and IBU
  - c. IBU shows failure code
  - d. LM detects loss of communication from the AOM
6. DOM reports channel-level failure
  - a. AOM reports the channel-failed status to the LM
  - b. IBU shows failure code
  - c. Application Logic detects failure via input signal bus and sends a command to drive this output and/or any other outputs to safe state

#### **6.2.6.5 Discrete Outputs Module**

The DOM is used for driving the galvanically isolated dry contact signals. Its safe state is open contact. The DOM has 32 independent output channels.



### DOM Product Highlights

- High density 32 channel Form-A optically isolated, fuse and overvoltage protected discrete outputs
- Independent FPGA for discrete input processing, self-diagnostics, and fail-safe functional behavior
- Robust self-diagnostics ensure higher reliability and early fault detection with safety-focused fault management
- Segregation of input processing, self-diagnostics, and watchdog functions assures safety-critical functionality
- 2 LVDS (redundant diagnostic and control data exchange)
- Diverse watchdog heartbeat monitoring and extensive functionally diverse self-diagnostics
- Fuse and Overvoltage protected outputs
- Hot swappable

#### 6.2.6.5.1 DOM Technical Specifications

The technical specifications for the DOM are:

Output channel load voltage / current (maximum switching voltage / current)	up to 48 VDC, 0.2 A, Form A contact
Output channel isolation	all output channels are galvanic-isolated up to 250 V <sub>RMS</sub> AC or 250 VDC field- to-Chassis and channel-to-channel
Output channel isolation method	optical relay
Output overvoltage protection	up to ±60 VDC/VAC continuous (using external protection elements installed in Chassis)





Information package exchange cycle	5 milliseconds
Diagnostic package exchange cycle	up to 5 milliseconds
LVDS line speed	100 Megabit/second
LVDS line protocol	proprietary protocol with integrity checking (CRC), galvanic-isolated Tx / Rx
Self-diagnostic functions	diverse watchdog unit, hardware error detection, checksum analysis, active diagnostics with internal fault detection, functionally diverse continuous self-diagnostic tests, power supply fault detection
Power supply / consumption	2 independent inputs – 24 (20.4 – 28.8) VDC / 0.63 A ( $\pm 0.15$ A)
Indications	2 status LED indicators (RUN/FAULT); 4-character dot matrix symbol-indicator for providing current operational mode, service information, and errors codes
Operating temperature	4.4 to 60 °C (40 to 140 °F)
Operating humidity	10 to 90% relative humidity, non-condensing

The functional diagram of the DOM is shown in Figure 6-20.



[[

]]<sup>a,c,e</sup>

**Figure 6-20: Functional Diagram of the DOM**

#### **6.2.6.5.2 DOM Operation**

The DOM operation requirements are to:

1. Driving of discrete dry contact signals and
2. Perform data exchange with the LM.

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The DOM operating modes and possible modes transitions are shown in Figure 6-21.

[[

]]<sup>a,c,e</sup>

**Figure 6-21: DOM Mode Transition Diagram**

In the POWERED-OFF mode the DOM does not perform any functions. All Hardware Units are de-energized, no data transmitted or received, configuration changes are not allowed. The DOM can transition to the STARTUP mode if the Module is energized.

In STARTUP Mode, the DOM performs the following functions:

1. All Hardware Units are energized [[



]]<sup>a,c,e</sup>

All functions of RUN mode are then performed, but a [[

]]<sup>a,c,e</sup>. In the [[

]]<sup>a,c,e</sup>. After [[

]]<sup>a,c,e</sup>, the DOM will transition into [[  
]]<sup>a,c,e</sup>

In RUN (SAFE) mode the DOM performs the following functions:

1. [[

]]<sup>a,c,e</sup>

The DOM can transition to the POWERED-OFF mode if the Module is de-energized. The DOM can transition to the [[

]]<sup>a,c,e</sup>. The DOM will transition into [[

]]<sup>a,c,e</sup>. The LM will also transition into [[

]]<sup>a,c,e</sup>

In RUN Mode, the DOM performs the following functions:

1. All Hardware Units are energized.
2. [[  
]]<sup>a,c,e</sup>
3. Module performs the following sequence of actions:
  - a. Data Processing:
    - [[
  - b. ata Transmission/Receiving:
    - Data transmission
      - [[
    - Data receiving
      - [[

]]<sup>a,c,e</sup>

]]<sup>a,c,e</sup>



4. Performed periodically or constantly during all processes described above:
- a. [[

]]<sup>a,c,e</sup>

The DOM can transition to the POWERED-OFF mode if the Module is de-energized. The DOM will transition into [[

]]<sup>a,c,e</sup>. The DOM will transition into  
]]<sup>a,c,e</sup>

[[

In FAULTED Mode, the DOM performs the following functions:

1. [[

]]<sup>a,c,e</sup>

The DOM in the [[ ]]<sup>a,c,e</sup>

In CONFIGURATION Mode, the DOM performs the following functions:

1. [[

]]<sup>a,c,e</sup>

In CONFIGURATION Mode, the DOM can transition to the POWERED-OFF mode if the Module is de-energized. The DOM will transition into [[

]]<sup>a,c,e</sup>

**6.2.6.5.3 DOM Failure Detection and Prevention**

The DOM is designed to detect deviations between the signals received from LM and conditioned output signals that exceed the specified accuracy or an output data conditioning process that exceeds the specified response time. The safety concept for the DOM includes the following features:

- [[ ]]<sup>a,c,e</sup>, as described in Section 6.4.2.
- [[ ]]<sup>a,c,e</sup>, as described in Section 6.4.



- [[

]]<sup>a,c,e</sup>, as described in Section 6.4.3.

- [[

]]<sup>a,c,e</sup>

Once an error condition has been detected, the error state continues to be reported on the Indication Board Unit and via the MATS until either power is removed or a higher-level error is detected.

The following actions are taken in response failures locally on DOM and on other Modules:

1. Removal of Module:
  - a. DOM inputs are disconnected from the field
  - b. LM detect loss of communication from the DOM
2. PSWD detects power supply or FPGA CRAM failure
  - a. PSWD cuts power to all units except itself and IBU
  - b. IBU shows failure code
  - c. DOM goes to FAULTED Mode and trip all outputs to safe state
  - d. LM detects loss of communication from the DOM
3. Communication fails – DOM does not receive commands from LM
  - a. DOM detect loss of communication from LM and goes to RUN(SAFE) Mode and sets all outputs to safe state redundantly (i.e., the SOR is set and all individual channels are commanded to the safe output value)
  - b. IBU shows failure code
  - c. LM detects loss of communication from the DOM
4. Communication fails – LM does not receive response from DOM
  - a. LM detects loss of communication from the DOM
  - b. LM sends flag to trip all output Modules to safe state

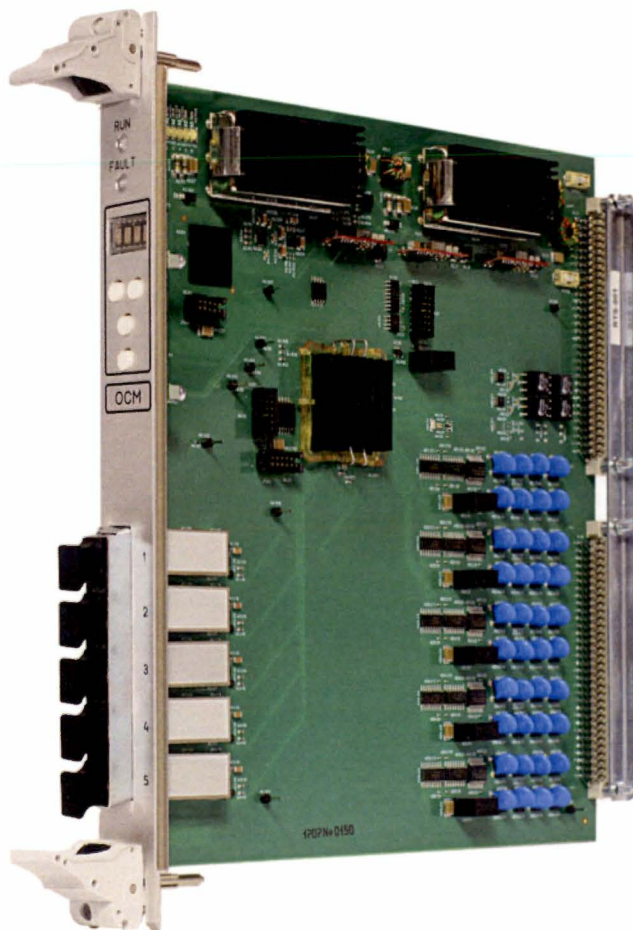


- c. All output Modules detect this flag and redundantly set all output channels to safe state (i.e., the SOR is set and all individual channels are commanded to the safe output value)
  - d. Application Logic may redundantly detect this via Module state signals and substitute a safe state value for all output channels
- 5. DOM reports high-level failure (e.g., CRC check error) of FPGA
  - a. FPGA detects the failure and stops updating the heartbeat signal to the PSWD
  - b. PSWD cuts power to all Units except itself and IBU
  - c. IBU shows failure code
  - d. LM detects loss of communication from the DOM
- 6. DOM reports channel-level failure
  - a. DOM reports the channel-failed status to the LM
  - b. IBU shows failure code
  - c. Application Logic detects failure via input signal bus and sends a command to drive this output and/or any other outputs to safe state

#### **6.2.6.6    *Optical Communication Module***

The OCM is intended for receiving and transmitting data via Fiber Optic (RPP) Interface that is used to extend the RadICS Platform to additional chassis, and for transmitting data via RS-232/485 Interfaces in a way that can be customized to be compatible with old systems. A pair of OCMs, which include OPTO Units, act as the isolating data transceivers between different Chassis (point-to-point communication). The OCM has five independent Optical Transceiver Units. Each of them performs transceiving data from/to other Chassis with OCMs. The OCM also has five independent RS-232/485 Transmitter Units to transmit data to older style monitoring systems.





### OCM Product Highlights

- 5 independent fiber optic communication ports for full duplex communications between channels or expansion racks
- 5 RS-232/RS-485 interfaces for one-way communication with peripheral devices
- Independent FPGA for data communication, self-diagnostics, and fail-safe functional behavior
- Robust self-diagnostics give early fault detection for safety-focused fault management
- Segregation of communications processing, self-diagnostics, and watchdog functions assures safety-critical functionality
- Galvanic isolation for external communication lines with robust and dedicated communication links to Logic Module for secure data transfer
- 2 LVDS lines (redundant diagnostic and control data exchange)
- Diverse watchdog heartbeat monitoring and extensive functionally diverse self-diagnostics
- Hot swappable

#### 6.2.6.6.1 OCM Technical Specifications

The technical specifications for the OCM are:

Fiber optical lines type	optical full duplex
LVDS lines type	hardwired full duplex
Fiber optical lines speed	100 Megabit/second
LVDS lines speed	100 Megabit/second
RS-232 interfaces speed	up to 115,200 Bauds
RS-485 interfaces speed	up to 10 Megabit/second
RS-232/RS-485 interfaces protection	up to 250 V <sub>RMS</sub> (line to line) up to 250 V <sub>RMS</sub> (line to ground) power cross condition
Information package exchange cycle	5 milliseconds





Diagnostic package exchange cycle	5 milliseconds
Fiber optical line protocol	proprietary protocol with integrity checking (CRC), galvanic-isolated Tx / Rx
LVDS line protocol	proprietary protocol with integrity checking (CRC), galvanic-isolated Tx / Rx
Isolation	all lines are galvanic-isolated
Self-diagnostic functions	diverse watchdog unit, hardware error detection, checksum analysis, active diagnostics with internal fault detection, functionally diverse continuous self-diagnostic tests, power supply fault detection
Power supply / consumption	2 independent inputs – 24 (20.4 – 28.8) VDC / 0.5 A ( $\pm 0.15$ A)
Indications	2 status LED indicators (RUN/FAULT); 4-character dot matrix symbol-indicator for providing current operational mode, service information, and errors codes
Operating temperature	4.4 to 60 °C (40 to 140 °F)
Operating humidity	10 to 90% relative humidity, non-condensing

The functional diagram of the OCM is shown in Figure 6-22.



[[

]]<sup>a,c,e</sup>

**Figure 6-22: Functional Diagram of the OCM**

#### **6.2.6.6.2 OCM Operation**

The OCM operation requirements are to:

1. Perform data exchange via optical communications with other OCM Modules.
2. Perform data exchange with LM.
3. Perform information integrity check for each received data packet.
4. Provide data for external sinks via RS-232/485 Interface.

The OCM operating modes and possible modes transitions are shown in Figure 6-23.

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[[

]]<sup>a,c,e</sup>

**Figure 6-23: OCM Mode Transition Diagram**

In the POWERED-OFF mode the OCM does not perform any functions. All Hardware Units are de-energized, no data transmitted or received, configuration changes are not allowed. The OCM can transition to the STARTUP mode if the Module is energized.

In STARTUP Mode, the OCM performs the following functions:

1. [[

]]<sup>a,c,e</sup>

All functions of RUN mode are then performed, but a [[

]]<sup>a,c,e</sup>. In the [[
]]<sup>a,c,e</sup>. After [[
]]<sup>a,c,e</sup>, the OCM will transition into RUN mode or into

[[

]]<sup>a,c,e</sup>

In RUN Mode, the OCM performs the following functions:

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1. All Hardware Units are energized.
2. [[ ]]<sup>a,c,e</sup>
3. Module performs the following sequence of actions:
  - a. Data receiving from LM and transmission to field:
    - Data receiving:
      - [[ ]]
    - Data transmission (identically for each of five OPTO Units):
      - [[ ]]
  - b. Data receiving from field and transmission to LM:
    - Data receiving (identically for each of five OPTO Units):
      - [[ ]]
    - Data transmission
      - [[ ]]
4. [[ ]]
5. Performed periodically or constantly during all processes described above:
  - a. [[ ]]

The OCM can transition to the POWERED-OFF mode if the Module is de-energized. The OCM will transition into [[ ]]

In FAULTED Mode, the OCM performs the following functions:

1. [[ ]]

The OCM in the [[ ]]



In CONFIGURATION Mode, the OCM performs the following functions:

- 1. [[

]]<sup>a,c,e</sup>

In CONFIGURATION Mode, the OCM can transition to the POWERED-OFF mode if the Module is de-energized. The OCM will transition into [[

]]<sup>a,c,e</sup>

**6.2.6.6.3 OCM Failure Detection and Prevention**

The OCM is designed to detect incorrect data received (based on CRC) from LM or other OCMs. The data with detected errors are flagged as invalid. The safety concept for the OCM includes the following features:

- [[

]]<sup>a,c,e</sup> as described in Section 6.4.2.

- [[

]]<sup>a,c,e</sup>, as described in Section 6.4.

- [[

]]<sup>a,c,e</sup>, as described in Section 6.4.3.

- [[



]]<sup>a,c,e</sup>

Once an error condition has been detected, the error state continues to be reported on the Indication Board Unit and via the MATS until either power is removed or a higher-level error is detected.

The following actions are taken in response failures locally on OCM and on other Modules:

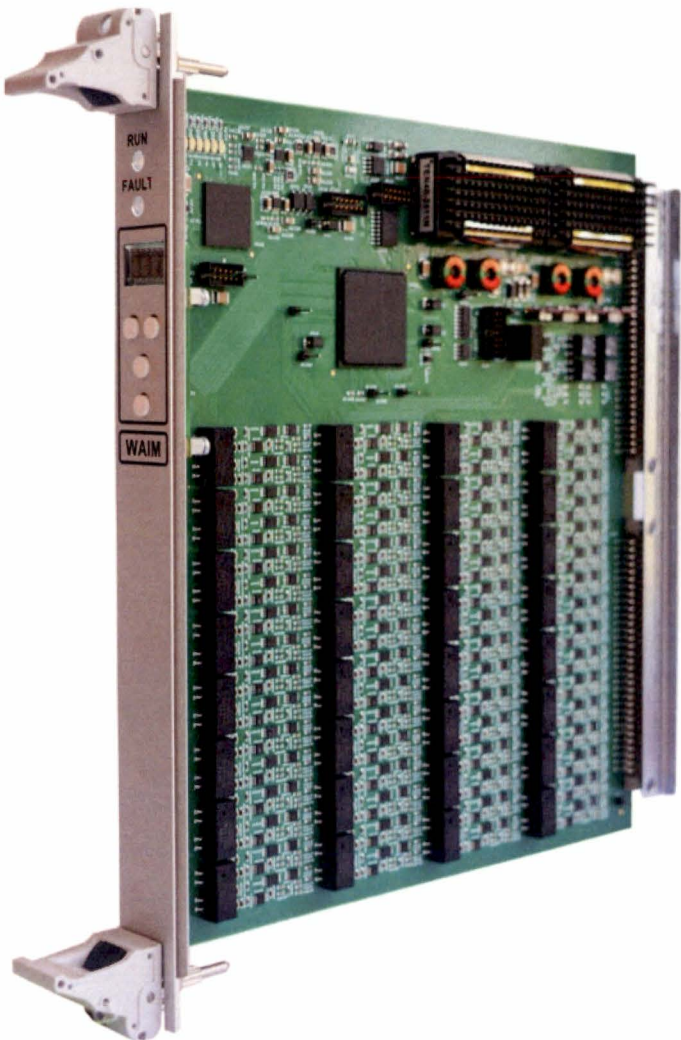
1. Removal of Module:
  - a. OCM optical and RS transceivers are disconnected from the field
  - b. LM detect loss of communication from the OCM
2. PSWD detects power supply or FPGA CRAM failure
  - a. PSWD cuts power to all units except itself and IBU
  - b. IBU shows failure code
  - c. LM detects loss of communication from the OCM
3. Communication fails – OCM does not receive commands from LM
  - a. OCM detect loss of communication from LM
  - b. OCM stops output data via fiber-optic and RS-232/485 interfaces
  - c. Other chassis detects time out
  - d. IBU shows failure code
  - e. LM detects loss of communication from the OCM
4. Communication fails – LM does not receive response from OCM
  - a. IBU shows failure code
  - b. LM detects loss of communication from the OCM
  - c. LM sends flag to trip all output Modules to safe state
  - d. All output Modules detect this flag and redundantly set all output channels to safe state (i.e., the SOR is set and all individual channels are commanded to the safe output value)
  - e. Application Logic may redundantly detect this via Module state signals and substitute a safe state value for all output channels
5. Communication fails – OCM lost connection with other chassis
  - a. OCM detects loss of communication with other chassis
  - b. IBU shows failure code
  - c. OCM marks received optical data as invalid
  - d. OCM output to LM zero value data
6. OCM reports high-level failure (e.g., CRC check error) of FPGA
  - a. FPGA detects the failure and stops updating the heartbeat signal to the PSWD
  - b. PSWD cuts power to all Units except itself and IBU
  - c. IBU shows failure code
  - d. LM detects loss of communication from the OCM
7. OCM gets wrong transceiving parameters
  - a. OCM detects this failure
  - b. OCM stops data transceiving via fiber-optic and RS-232/485 interfaces
  - c. IBU shows failure code





6.2.6.7 Wide Range Analog Inputs Module

The WAIM is used for the acquisition of analog signals (-10 V to +10 V DC) and the conversion to engineering units. The WAIM has 32 independent input channels.



WAIM Product Highlights

- High density 32 channel analog inputs with built-in hardware redundancy and self-diagnostics for highly reliable operation, filtering, calibration, and random hardware failure detection
- Robust self-diagnostics ensure higher reliability and early fault detection with safety-focused fault management
- Segregation of input processing, self-diagnostics, and watchdog functions assure safety-critical functionality
- 18-bit analog/digital (A/D) conversion in each analog input channel
- 2 LVDS full duplex lines (redundant diagnostic and control data exchange)
- Diverse watchdog heartbeat monitoring and extensive functionally diverse self-diagnostics
- Built-in calibration
- Hot swappable

6.2.6.7.1 WAIM Technical Specifications

The technical specifications for the WAIM are:

Input analog signal range	±10 V DC (with ±11 overrange monitoring capability) Differential input impedance: not less than 1 MΩ.
A/D conversion resolution	18 bits / 400 kSPS
Response time	5 milliseconds



Common mode rejection ratio	> 86 dB
Overall accuracy	0.04% of full scale (at 25 °C)
Input channel isolation	all input channels are galvanic-isolated up to 250 V <sub>RMS</sub> AC or 250 VDC field-to-Chassis and channel-to-channel
Overvoltage protection	±60 VAC/VDC continuous (using external protection elements installed in Chassis)
Information package exchange cycle	5 milliseconds
Diagnostic package exchange cycle	5 milliseconds
LVDS line speed	100 Megabit/second
LVDS line protocol	proprietary protocol with integrity checking (CRC), galvanic-isolated Tx / Rx
Self-diagnostic functions	diverse watchdog unit, hardware error detection, checksum analysis, active diagnostics with internal fault detection, functionally diverse continuous self-diagnostic tests, power supply fault detection
Power supply / consumption	2 independent inputs – 24 (20.4 – 28.8) VDC /1.01 A (± 0.15 A)
Indications	2 status LED indicators (RUN/FAULT); 4-character dot matrix symbol-indicator for providing current operational mode, service information, and errors codes
Operating temperature	4.4 to 60 °C (40 to 140 °F)
Operating humidity	10 to 90% relative humidity, non-condensing

The functional diagram of the WAIM Unit is shown in Figure 6-24.



[[

]]<sup>a,c,e</sup>**Figure 6-24: Functional Diagram of the WAIM**

The functional diagram of the WAIM is the same as the AIM shown in Figure 6-14 except that the WADC Unit replaces the ADC Unit.

**6.2.6.7.2 WAIM Operation**

The WAIM operation requirements is the same as that described for the AIM in Section 6.2.6.2.2 except that data is acquired from the WADC Units rather than the ADC Units.

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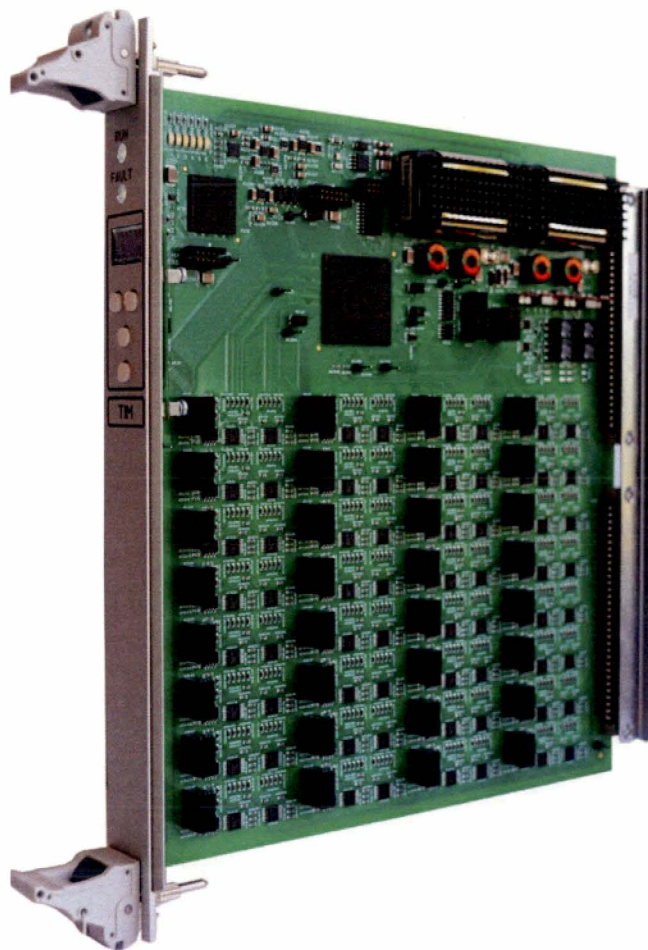


#### 6.2.6.7.3 WAIM Failure Detection and Prevention

The WAIM failure detection and prevention are the same as those described for the AIM in Section 6.2.6.2.3.

#### 6.2.6.8 Thermocouple Inputs Module

The TIM is used for the acquisition of various types of thermocouple input signals and the conversion to engineering units. The TIM has 32 independent input channels.



#### TIM Product Highlights

- High density 32 channel analog inputs with built-in hardware redundancy and self-diagnostics for highly reliable operation, filtering, calibration, and random hardware failure detection
- Robust self-diagnostics ensure higher reliability and early fault detection with safety-focused fault management
- Segregation of input processing, self-diagnostics, and watchdog functions assure safety-critical functionality
- 19 bit delta-sigma analog/digital (A/D) conversion in each analog input channel
- 2 LVDS full duplex lines (redundant diagnostic and control data exchange)
- Diverse watchdog heartbeat monitoring and extensive functionally diverse self-diagnostics
- Built-in calibration
- Hot swappable

#### 6.2.6.8.1 TIM Technical Specifications

The technical specifications for the TIM are:

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Supported sensor types	Type B, E, J, K, N, R, S, T with internal conversion $mV \rightarrow t^{\circ}C$ . Also supports raw millivolts (mV) acquisition (to support any other sensor type with external conversion into temperature performed in Logic Module).
A/D conversion resolution	19 bits delta-sigma analog-to-digital conversion
Response time	300 milliseconds
Common mode rejection ratio	> 86 dB
Overall accuracy	Type B: 0.15% of full scale (at 25 °C) Type R, S, T: 0.1% of full scale (at 25 °C) Others: 0.04% of full scale (at 25 °C)
Input channel isolation	all input channels are galvanic-isolated up to 250 V <sub>RMS</sub> AC or 250 VDC field-to-Chassis and channel-to-channel
Overvoltage protection	±60 VAC/VDC continuous (using external protection elements installed in Chassis)
Information package exchange cycle	5 milliseconds
Diagnostic package exchange cycle	5 milliseconds
LVDS line speed	100 Megabit/second
LVDS line protocol	proprietary protocol with integrity checking (CRC), galvanic-isolated Tx / Rx
Self-diagnostic functions	diverse watchdog unit, hardware error detection, checksum analysis, active diagnostics with internal fault detection, functionally diverse continuous self-diagnostic tests, power supply fault detection
Power supply / consumption	2 independent inputs – 24 (20.4 – 28.8) VDC / 0.4 A (± 0.1 A)
Indications	2 status LED indicators (RUN/FAULT); 4-character dot matrix symbol-indicator for providing current operational mode, service information, and errors codes
Operating temperature	4.4 to 60 °C (40 to 140 °F)
Operating humidity	10 to 90% relative humidity, non-condensing

The functional diagram of the TIM is shown in Figure 6-25.



[[

]]<sup>a,c,e</sup>**Figure 6-25: Functional Diagram of the TIM**

The functional diagram of the TIM is the same as the AIM shown in Figure 6-14 except that the TDC Unit replaces the ADC Unit.

**6.2.6.8.2 TIM Operation**

The TIM operation requirements is the same as that described for the AIM in Section 6.2.6.2.2 except that data is acquired from the TDC Units rather than the ADC Units.

**6.2.6.8.3 TIM Failure Detection and Prevention**

The TIM failure detection and prevention are the same as those described for the AIM in Section 6.2.6.2.3.

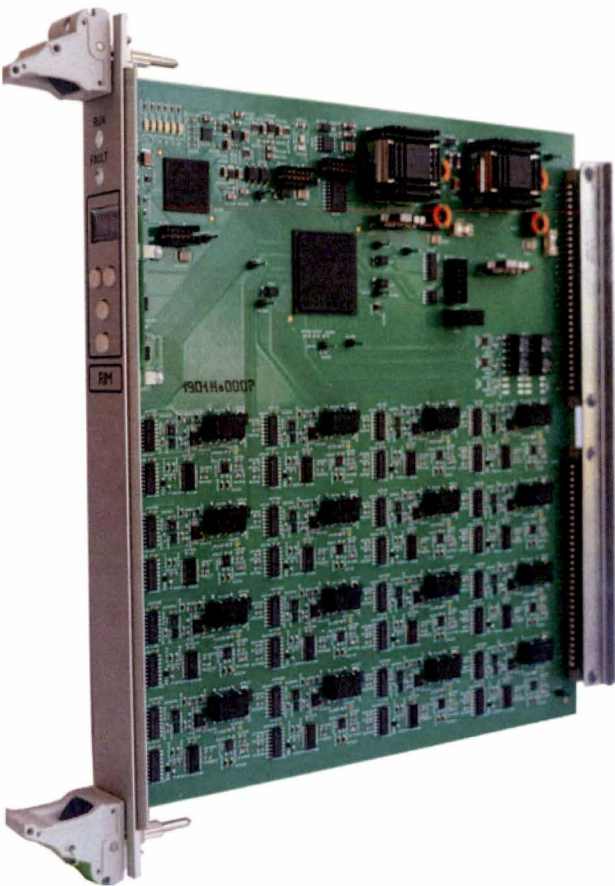
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6.2.6.9 Resistance Temperature Detector Inputs Module

The RIM is used for the acquisition of various types of RTD input signals and the conversion to engineering units. The RIM has 8 independent input channels.



RIM Product Highlights

- High density 8 channel analog inputs with built-in hardware redundancy and self-diagnostics for highly reliable operation, filtering, calibration, and random hardware failure detection
- Robust self-diagnostics ensure higher reliability and early fault detection with safety-focused fault management
- Segregation of input processing, self-diagnostics, and watchdog functions assure safety-critical functionality
- 18-bit analog/digital (A/D) conversion in each analog input channel
- 2 LVDS full duplex lines (redundant diagnostic and control data exchange)
- Diverse watchdog heartbeat monitoring and extensive functionally diverse self-diagnostics
- Built-in calibration
- Hot swappable

6.2.6.9.1 RIM Technical Specifications

The technical specifications for the RIM are:

Input analog signal range	5-1500 $\Omega$ (0-1600 $\Omega$ over-range monitoring capabilities) 4 signal sub-ranges: 5-198 $\Omega$ ; 5-398 $\Omega$ ; 5-795 $\Omega$ ; 5-1500 $\Omega$
---------------------------	--



Supported sensor types	2-, 3- and 4-wire connection schemes supported Raw resistance ( $\Omega$ ) measurement (to support any specific sensor type with external conversion into temperature performed in Logic Module) 5 pre-defined RTD sensor types support with adjustable $R_0$ (up to 350 $\Omega$ ) and $R \rightarrow t$ conversion performed internally by module Supported RTD types: <ul style="list-style-type: none"> <li>- Platinum (<math>\alpha=0.00385</math> per <math>^{\circ}\text{C}</math>) – corresponds to IEC 751</li> <li>- Platinum (<math>\alpha=0.00391</math> per <math>^{\circ}\text{C}</math>)</li> <li>- Copper (<math>\alpha=0.00428</math> per <math>^{\circ}\text{C}</math>)</li> <li>- Copper (<math>\alpha=0.00426</math> per <math>^{\circ}\text{C}</math>)</li> <li>- Nickel (<math>\alpha=0.00617</math> per <math>^{\circ}\text{C}</math>)</li> </ul>
A/D conversion resolution	18 bits / 400 kSPS
Response time	100 milliseconds
Common mode rejection ratio	> 86 dB
Input channel isolation	all input channels are galvanic-isolated up to 250 V <sub>RMS</sub> AC or 250 VDC field-to-Chassis and channel-to-channel
Overvoltage protection	$\pm 60$ VAC/VDC continuous (using external protection elements installed in Chassis)
Information package exchange cycle	5 milliseconds
Diagnostic package exchange cycle	5 milliseconds
LVDS line speed	100 Megabit/second
LVDS line protocol	proprietary protocol with integrity checking (CRC), galvanic-isolated Tx / Rx
Self-diagnostic functions	diverse watchdog unit, hardware error detection, checksum analysis, active diagnostics with internal fault detection, functionally diverse continuous self-diagnostic tests, power supply fault detection
Power supply / consumption	2 independent inputs – 24 (20.4 – 28.8) VDC / 0.29 A ( $\pm 0.1$ A)
Indications	2 status LED indicators (RUN/FAULT); 4-character dot matrix symbol-indicator for providing current operational mode, service information, and errors codes
Operating temperature	4.4 to 60 $^{\circ}\text{C}$ (40 to 140 $^{\circ}\text{F}$ )
Operating humidity	10 to 90% relative humidity, non-condensing

The functional diagram of the RIM is shown in Figure 6-26.



[[

]]<sup>a,c,e</sup>

**Figure 6-26: Functional Diagram of the RIM**

The functional diagram of the RIM is the same as the AIM shown in Figure 6-14 except that RTD Units replaces the ADC Unit.

**6.2.6.9.2 RIM Operation**

The RIM operation requirements is the same as that described for the AIM in Section 6.2.6.2.2 except that data is acquired from the RTD Units rather than the ADC Units.

**6.2.6.9.3 RIM Failure Detection and Prevention**

The RIM failure detection and prevention are the same as those described for the AIM in Section 6.2.6.2.3.

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## 6.3 Communications

The RadICS Platform includes various interfaces and protocols, including fiber optic interfaces and LVDS protocol for inter-Module and inter-Chassis connectivity purposes. The RadICS Platform communication features contribute to the predictability and repeatability of the design and satisfy the system integrity requirements of IEEE Std 603-1991 Section 5.5 and IEEE Std 7-4.3.2-2003 Sections 5.5.1 and 5.6. Additional aspects of the RadICS Platform communication independence features comply with DI&C-ISG-04, Revision 1 guidance regarding inter-divisional communication.

### 6.3.1 Basic Concepts

Physical and functional Independence of communication channels is achieved by selecting appropriate system architectures and data communication protocols. The implementation of radial (point-to-point) architecture in RadICS Platform interchannel communication links provides the RadICS Platform with the capability to maintain failure-free data exchange between I&C components even when one of the channels has failed. Additional measures designed to achieve the desired physical and functional independence are the application of fiber-optic communication lines for data exchange between I&C components and the separation of safety and control functions from information and diagnostic functions.

Three types of communication categories are defined for the RadICS Platform.<sup>10</sup> They are as follows:

- White Channel - Communication channel in which all hardware and software components (including electronic design) are designed implemented and validated according to IEC 61508. Implication: trusted safety channel
- Grey Channel - Communication channel with some evidence of design or validation according to IEC 61508. Implication: an untrusted channel that has some known design features which reduce the diagnostics needed to be able to trust the channel (e.g., point-to-point wiring rules out aliasing as a source of error)
- Black Channel - Communication channel without available evidence of design or validation according to IEC 61508. Implication: totally untrusted channel; all safety measures must be taken by functions connected to the two ends of the channel

In the RadICS Platform architecture, all communications with other Modules within the same Chassis are based on dedicated slot-to-slot (point-to-point) connections between predefined specific slot locations. I/O Modules can communicate only with the LM within the same Chassis. Physically the Chassis and LVDS channel will support a LM Module in slot F1. This eliminates the need for any slot specific addressing for I/O Modules. The LM also has a dedicated slot so that it does not require any additional address information to communicate with any other Modules within the same Chassis.

Each set of point-to-point communication paths between an I/O Module and the Chassis LM uses four physical lines to provide fully independent full duplex differential communications in both directions for each link. This link is the LVDS interface. The backplane communication is safety-related and designed as a SIL 3 black-channel.

<sup>10</sup> IEC 61784-3:2010 has a description of white, grey and black channels (Reference 6-5)

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The RadICS Platform architecture design eliminates the need for slot addresses since all communications within the Chassis take place using dedicated point-to-point connections between slot positions so that only two Modules have access to those signal paths. The participants in these communications are therefore uniquely identified without the possibility of cross interference, except by multiple physical short circuits between physical lines, which are nearly impossible to occur and would be detected if it occurred. Additional within-Chassis communications communication checking measures are implemented in the Platform ED. For example, inserted messages are detected by invalid sequence numbers and potentially protocol or media access violations. Corruptions and collisions would be detected by the packet level CRC. The communication error checking techniques are described in Section 6.4.3.

The FPGA Unit acquires input data, executes Module logic functions (e.g., data processing, Application Logic, etc.), performs diagnostics, and conditions output data. [[

]]<sup>a,c,e</sup>

In general, all communications interfaces are treated as safety critical using the measures summarized below (the broadcast link to the MATS is not safety critical but uses all the measures below except acknowledgement). Table 6-4 summarizes all the links, the protocol used, and the safety criticality according to IEC 61508. The RadICS Platform uses several types of communication links that are utilized as an external interface from the board, as well as, several communication links that utilized internally on the board. External communication links can be used for inter-divisional and intra-divisional communications depending on the system configuration and architecture, as indicated in the table below.



Table 6-4: Summary of Communications Links

Communication Link	Protocol	Usage	Safety Criticality
LM $\leftrightarrow$ I/O Modules and OCMs via backplane LVDS	RPP	Communication between LM and other Modules within the same Chassis	[[ ]] <sup>a,c,e</sup>
OCM $\leftrightarrow$ OCM via fiber optic cable	RPP	Communication between LMs in different racks via the OCM. Extends the RadICS Platform capabilities by adding I/O or processing expansion in another chassis and can be used for inter- and intra-divisional communication.	[[ ]] <sup>a,c,e</sup>
LM $\leftrightarrow$ LM via fiber optic cable	RPP	Extends the RadICS Platform capabilities by adding I/O or processing expansion in another chassis and can be used for inter- and intra-divisional communication.	[[ ]] <sup>a,c,e</sup>
PSWD $\leftrightarrow$ FPGA	RSWP	Inter-unit interface within a module between the PSWD CPLD and FPGA for self-diagnostics and watchdog functions.	[[ ]] <sup>a,c,e</sup>





Communication Link	Protocol	Usage	Safety Criticality
LM → MATS via fiber optic cable (broadcast)	RUP	One-way data broadcast to the MATS for monitoring purposes.	[[  ]] <sup>a,c,e</sup>
MATS Tuning PC ↔ LM via fiber optic cable (temporary connection)	RUP	Temporary bidirectional connection for the purpose of modifying the Application ED operational (tuning) parameters	[[  ]] <sup>a,c,e</sup>
UART interface	RPU	Temporary connection used to download and upload configuration data to and from EEPROM via FPGA internal RAM while in CONFIGURATION mode (only accessible with Module inserted into DLS chassis)	[[  ]] <sup>a,c,e</sup>
SPI interface	RSPE <sup>11</sup>	Inter-unit interface for data exchange between FPGA and EEPROMs (Configuration and Tuning)	[[  ]] <sup>a,c,e</sup>

Several additional measures are utilized for communications to support the RadICS Platform fundamental safety approach.

- CRCs are used on all communications and safety-critical data. External communications links are all treated as 'black-channel'.
- Communications ports are monitored and blocked except when specifically required (e.g., tuning).
- The interface to the MATS is one-way broadcast (i.e., non-interfering), rated at SIL 2. Thus, the MATS is also non-interfering. (Note: The MATS is supplied to the end user, to meet project-specific Human Factors requirements.)
- The RadICS Platform blocks all inward communications with the only exception being tuning inputs when put into TUNING mode by the keyswitch.

<sup>11</sup> RSPE – Radiy SPI-based Protocol for EEPROM



- Implementation of the lower levels of the transmission path between two OCMs is not relevant to analysis of safety communications based upon the black channel concept, since all necessary integrity measures are included as a part of the safety application level of the protocol.
- All communication links between OCMs are configured as point-to-point data exchanges with only one data source and one data sink.

### 6.3.2 RadICS Communication Hardware Components

The basic RadICS Platform communications interfaces and dedicated hardware Modules are described in Sections 6.2.4.2, and 6.2.6.6, and 6.3. This section describes how the board level communication components work. There are four board level communication components:

- OPTO Unit
- LVDS Unit
- LAN Unit
- RS-232/485 Unit

The primary purpose of these components is to enable data exchange within and between the RadICS Chassis as well as external devices. Several different communication protocols are utilized, as described in Section 6.3.3.

- Radiy Proprietary Protocol – RPP
- Radiy UDP based Protocol – RUP
- RS-232 based Protocol – RS-232
- Radiy Protocol for UART Interface (RPU)
- Radiy SPI-based Protocol for EEPROM (RSPE)
- Radiy Watchdog Interface Channel Level Protocol (RSWP)

Diagnostics of the components are performed through RadICS Platform ED by analyzing the data and the transmission protocols that are transmitted through each component. The fiber optic RUP Interface is de-energized, if the TUNING key is not in Tuning position and RadICS Platform is not in TUNING mode. All external communications links are optically isolated and the output to the monitoring station is non-interfering (one-way broadcast).

#### 6.3.2.1 Optical Transceiver Unit

The OPTO Unit is used for optical transceiving with another OPTO Unit in another OPTO Unit in another Module for fiber optic inter-Chassis communication (i.e., not within the same Chassis). The OPTO Unit uses a standard optical transceiving interface (i.e., AFCT-5971ALZ or equivalent optical transceiver and LC connectors) and the RPP protocol. The OPTO Unit converts electric signals to optical signals and vice versa, provides galvanic isolation for resistance to external influences on optical signals, and for signal transmission outside the Chassis. OPTO Units consists of two parts (i.e., optical transceiver and converters for receiving and transmitting) that provide full duplex communication mode. All communication links of the OPTO Unit are executed according point-to-point principle between two different Modules. Every communication link has its own identification (i.e., OPTO port unique address and OPTO port data unique identification) to allow for detection of an incorrect connection between

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two devices. Each communication link identifier is unique within the complete system (i.e., not just one chassis). The OPTO Unit is safety related. The OPTO Units are hardware devices that can be seen in the lower left of the pictures of the Logic Module and Optical Communication Modules in RadICS Topical Report Sections 6.2.6.1 and 6.2.6.6, respectively.

The OPTO Unit is considered a black-channel device so all data sent via this Unit is subject to the communications protocol for the link in question, which includes complete data validation by ED. The error detection methods are described in Section 6.4.

**6.3.2.2    LVDS Transceiver Unit**

The LVDS Unit is used for point-to-point communication between the LM (in slot 1) and any I/O or communication Module (in slots 2 through 15) in the same Chassis. LVDS provides galvanic isolation and converts the unidirectional discrete electric signal in the form of a differential signal using two symmetrical links. LVDS consists of a receiver and transmitter, providing full-duplex operation supported by an LVDS Transceiver Unit located on other Modules in the same Chassis. All communication links of LVDS are implemented on point-to-point principle between two different Modules (e.g., LM to AIM). The RPP communication protocol is used for data exchange between LM with I/O Modules and OCMs within the Chassis, as described in Table 6-4. The LVDS Unit is safety related.

The LVDS Unit is considered a black-channel device so all data sent via this Unit is subject to the communications protocol for the link in question, which includes complete data validation by the RadICS Platform ED. The error detection methods are described in Section 6.4.

**6.3.2.3    LAN Transceiver Unit**

The LAN Unit is used for communication with a peripheral device (e.g., MATS or MATS Tuning PC). It uses RUP to transmit data to the MATS. When the LAN Unit is designated for use with a MATS Tuning PC, the Unit is in de-energized state except in the TUNING Mode. Dedicated protocols are used for specific purposes: RUP for the Tuning interface and RUP for the one-way broadcast to the MATS. A fiber-optic cable is used to galvanically isolate the LM from the external Unit. The LAN Unit is safety related.

For a RadICS Platform-based system in a Class 1E application, by design and architecture connections to a non-Class 1E communication link is not allowed. These connections are verified during the design and V&V processes. This design approach provides a non-interfering communication interference. The Interfaces and Data Transmission Self-Diagnostics described in RadICS Topical Report Section 6.4.3 provide additional defense-in-depth for unwanted connection that was made inadvertently. [[

]]<sup>a,c,e</sup>

The cases are allowed for the connection of non-1E class equipment to a safety division. Connections to the LM are as follows:

- Tuning Interface (described in Section 6.9)
- MATS (described in Sections 6.3 and 6.6)

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- OCM RS-232/485 Transmitter Unit (described in Section 6.2.5.2.12)

[[

]]<sup>a,c,e</sup> as shown in RadICS Topical Report Figure 6-12. [[

]]<sup>a,c,e</sup>

For the TUNING interface, the LAN Transceiver Unit receiving port is connected for the TUNING interface; however, the [[

]]<sup>a,c,e</sup>

The LAN Transceiver Unit is [[ unless the keyswitch is turned on. When the TUNING keyswitch is turned on, the RadICS Platform outputs, associated with the LM being tuned, are isolated from the field (i.e., placed in safe state) for tuning. A fiber-optic cable is used to galvanically isolate the LM from the MATS Tuning PC.

[[

]]<sup>a,c,e</sup> As a result, a hardwired one-way communication interface is implemented.

The LAN Unit is considered a black-channel device so all data sent via this Unit is subject to the communications protocol for the link in question, including rejection of incoming transmissions where not allowed. The error detection methods are described in Section 6.4.

#### **6.3.2.4 RS-232/485 Transmitter Unit**

The RS-232/485 Unit is used for one-way communication with a peripheral device (e.g., data acquisition system). The RS-232/485 Unit uses the RS-232/485 Interface to transmit data. Dedicated protocols are used for specific purposes: RS-232/485 Interface (RPP). The OCM one-way interface is implemented using the RS-232/485 Transmitter Unit. The RS-232/485 Transmitter Unit Controller is implemented in the OCM FPGA, as shown on Figure 6-22. [[

]]<sup>a,c,e</sup> The

RS-232/485 Unit is safety related. Digital isolators are used to galvanically isolate the RS-232/485 connections.

The RS-232/485 Unit is considered a black-channel device so all data sent via this Unit is subject to the communications protocol for the link in question, including rejection of incoming transmissions where not allowed. The error detection methods are described in Section 6.4.

### **6.3.3 Communication Protocols**

The RadICS Platform uses several types of data communication:

- Client-server (safety-related point-to-point as in the I/O Module response to interrogation by the LM)
- Broadcast (non-safety related as in the on-line reporting of plant data and RadICS Platform status to MATS)

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- Transformational (as in a transceiver used for communication between LMs in the same division (safety-related) or between LM and MATS Tuning PC (non-safety related))

In all cases, two things are specified for the communications link to meet IEC 61508 requirements:

- Sequence of operations
- Data packet construction, including validation data and demonstration that it is of adequate capability to detect errors for the SIL target

Safety features of all communication interfaces used in the RadICS Platform are listed in Table 6-5.



Table 6-5: Safety Features of RadICS Communication Interfaces

[[





]]<sup>a,c,e</sup>

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The RadICS Platform data transmission protocols are divided into two levels:

- Transport Level Protocols – intended to transmit (transport) fixed amounts of any data and to provide Channel Level Protocol organization; data integrity checks are part of protocol service data.
- Channel Level Protocols – intended to organize a data exchange channel with defined data structure; consist of multiple frames of Transport Level Protocols; data integrity check means can be present as part of data.

### **6.3.3.1    *Transport Level Protocols***

Transport Level Protocols are:

- RPP (Radiy Proprietary Protocol) – is basic for all in-Chassis and inter-Chassis communications
- RUP (Radiy UDP-based Protocol) – is used for communication with MATS and MATS Tuning PC
- RS-232 (Radiy RS-232-based Protocol) – is basic for communications with other equipment via RS-232 interface
- RPU (Radiy Protocol for UART Interface) – is basic for data exchange via UART interface with the DLS
- RSPE (Radiy SPI-based Protocol for EEPROM) – is basic for data exchange between FPGA and EEPROM

#### **6.3.3.1.1    Radiy Proprietary Protocol**

RPP is basic protocol for data exchange within Chassis and for inter-Chassis data exchange.

RPP has the following message structure:

[[

]]<sup>a,c,e</sup>

RPP has error detection methods based on the requirements in IEC 61508 Part 2, clause 7.4.11.

Error Type	Inherent Defenses	Added Defenses
Corruption	-	[[ ]]a,c,e
Unintended repetition	-	[[ ]]a,c,e
Incorrect sequence	Backplane: Lack of any storage mechanism in the black channel.	[[ ]]a,c,e
Loss	-	[[ ]]a,c,e
Unacceptable delay	-	[[ ]]a,c,e
Insertion	Point-to-point: there is no other signal source in any channel	[[ ]]a,c,e
Masquerade	Point-to-point: there is no other signal source in any channel	[[ ]]a,c,e
Addressing		[[ ]]a,c,e

#### 6.3.3.1.2 Radiy UDP-based Protocol

RUP is basic protocol for data exchange with external devices (e.g., MATS, MATS Tuning PC, etc.).

RUP has the following message structure:



II

]]<sup>a,c,e</sup>

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RUP has error detection methods based on the requirements in IEC 61508 Part 2, clause 7.4.11.

Error Type	Inherent Defenses	Added Defenses
Corruption	-	[[]] <sup>a,c,e</sup>
Unintended repetition	-	[[]] <sup>a,c,e</sup>
Incorrect sequence	Incorrect sequence of frames or transmission sessions is not crucial. Numerator affects only CRC to add dynamically changing parameter in case of static data.	[[]] <sup>a,c,e</sup>
Loss	-	[[]] <sup>a,c,e</sup>
Unacceptable delay	-	[[]] <sup>a,c,e</sup>
Insertion	-	[[]] <sup>a,c,e</sup>
Masquerade	-	[[]] <sup>a,c,e</sup>

#### 6.3.3.1.3 Radiy RS-232-based Protocol

RS-232 is a one-way protocol and used for communications with old equipment via RS-232 interface. RS-232 uses standard UART protocol as a base without parity bit and bitrate of data transceiving is constant. The data bits are sent within each byte least significant bit (LSB) first. This standard is also referred to as "little endian". The data bytes are also sent within each word LSB first.



RS-232 has the following message structure:

[[  
|

-  
-  
-  
-  
-  
-  
-  
-

]]<sup>e</sup>

#### 6.3.3.1.4 RPU Radiy Protocol for UART Interface

RPU is basic for data exchange via UART interface with the DLS to download/upload data to/from FPGA internal RAM for further downloading/uploading to/from EEPROM.

RPU has the following message structure:

[[

]]<sup>a,c,e</sup>

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Error Type	Inherent Defenses	Added Defenses
Corruption	-	[[ ]] <sup>a,c,e</sup>
Unintended repetition	Repetition is not dangerous. Same data will be re-stored in same addresses two or more times.	-
Incorrect sequence	Order in which data will be stored is not crucial. It is only crucial to store whole data package.	[[ ]] <sup>a,c,e</sup>
Loss	-	[[ ]] <sup>a,c,e</sup>
Unacceptable delay	-	[[ ]] <sup>a,c,e</sup>
Insertion	Point-to-point: there is only one source.	[[ ]] <sup>a,c,e</sup>
Masquerade	Point-to-point	[[ ]] <sup>a,c,e</sup>

RSPE is basic for data exchange between FPGA and EEPROM.



RSPE has the following message structure:

[[

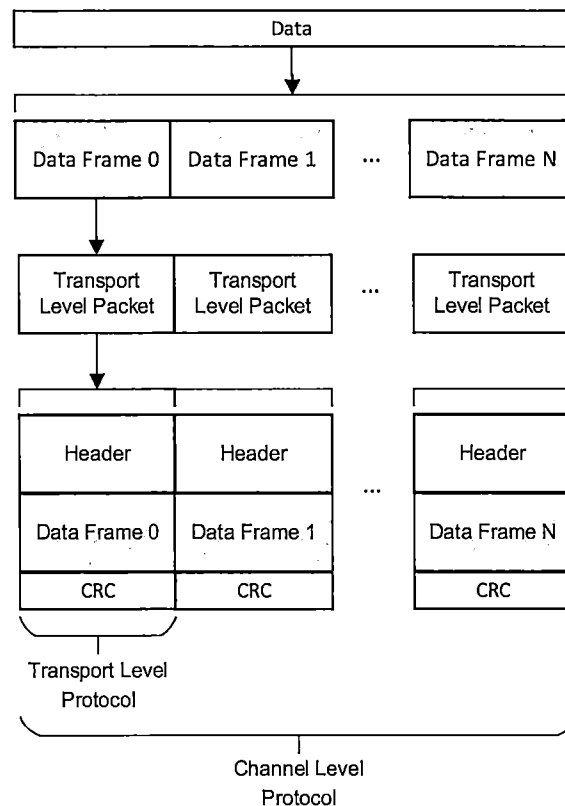
]]<sup>a,c,e</sup>

The read process is very simple. The RadICS Module FPGA specifies the frame number it wants to read. The frame number is transformed into an absolute EEPROM address offset. The EEPROM data frame includes the data and a CRC-64 checksum calculated that includes the frame address. Data integrity checks are performed during frame downloading, which include checks of the embedded frame address. RSPE has error detection methods based on the requirements in IEC 61508 Part 2, clause 7.4.11.

Error Type	Inherent Defenses	Added Defenses
Corruption	-	[[ ]] <sup>a,c,e</sup>
Unintended repetition	Repetition is not dangerous. Same data will be re-stored in same addresses two or more times.	-
Incorrect sequence	Order in which data will be stored is not crucial. It is only crucial to store whole data package.	[[ ]] <sup>a,c,e</sup>
Loss	CRC-64 calculated and uploaded to EEPROM with data will be used during the downloading process for integrity checking.	-
Unacceptable delay	See discussion for RPU Transport and SPIP Channel protocols.	[[ ]] <sup>a,c,e</sup>
Insertion	Point-to-point: EEPROM and FPGA are hard-wired. No connector is present.	-
Masquerade	Point-to-point: EEPROM and FPGA are hard-wired. No connector is present.	-

### 6.3.3.2 Channel Level Protocols

Channel Level Protocols are protocols for each interface specified in Table 6-5. They all are based on Transport Level Protocols. The Channel Level Protocol is a sequence of Transport Level Protocol frames. The general approach to a channel level protocol is shown in Figure 6-27.



**Figure 6-27: General Channel Level Protocol**

The Channel Level Protocols are described below, except for the proprietary Altera protocols used to configure the RadICS Modules.

#### 6.3.3.2.1 LVDS Interface Channel Level Protocol

LVDS Interface Protocol is based on RPP and is a sequence of RPP frames. It has all the functionality of RPP with the following additional error detection methods:

Error Type	Inherent Defenses	Added Defenses
Unacceptable delay		[[ ]] <sup>a,c,e</sup>

#### 6.3.3.2.2 Fiber Optic Inter-Chassis Interface Channel Level Protocol

FOIP is based on RPP and is a sequence of RPP frames. It has all the functionality of RPP with the following additional error detection methods:

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Error Type	Inherent Defenses	Added Defenses
Unacceptable delay		[[ ]] <sup>a,c,e</sup>
Insertion	Point-to-point: there is no other signal source in any channel	[[ ]] <sup>a,c,e</sup>
Masquerade	Point-to-point: there is no other signal source in any channel	[[ ]] <sup>a,c,e</sup>

#### 6.3.3.2.3 Fiber Optic Monitoring Interface Channel Level Protocol

FOMP is based on RUP and is a sequence of RUP frames. It has all the functionality of RUP with the following additional error detection methods:

Error Type	Inherent Defenses	Added Defenses
Unintended repetition	Repetition is not dangerous. Same data will be re-stored in same addresses two or more times.	[[ ]] <sup>a,c,e</sup>
Unacceptable delay	No acknowledgement mechanism to prevent any control from MATS	[[ ]] <sup>a,c,e</sup>
Insertion	-	[[ ]] <sup>a,c,e</sup>
Masquerade	-	[[ ]] <sup>a,c,e</sup>

#### 6.3.3.2.4 Fiber Optic Tuning Interface Channel Level Protocol

FOTP is based on RUP and is a sequence of RUP frames. It has all the functionality of RUP with the following additional error detection methods:

Error Type	Inherent Defenses	Added Defenses
Unintended repetition	Repetition is not dangerous. Same data will be re-stored in same addresses two or more times.	[[ ]] <sup>a,c,e</sup>
Unacceptable delay	-	[[ ]] <sup>a,c,e</sup>



Error Type	Inherent Defenses	Added Defenses
Insertion	-	[[ ]] <sup>a,c,e</sup>
Masquerade		[[ ]] <sup>a,c,e</sup>

#### 6.3.3.2.5 RS-232 Interface Channel Level Protocol

RSCP is based on RS-232 and is a sequence of RS-232 frames. It has all the functionality of RUP with any additional error detection methods defined during the ED AD development stage.

#### 6.3.3.2.6 Radiy Watchdog Interface Channel Level Protocol

RSWP is channel level protocol that does not have a dedicated transport level protocol. It is intended for communications between FPGA and the CPLD in the PSWD Unit.

RSWP has the following message structure:

[[

]]<sup>a,c,e</sup>

RSWP has error detection methods based on the requirements in IEC 61508 Part 2, clause 7.4.11.



Error Type	Inherent Defenses	Added Defenses
Corruption	-	[[ ]] <sup>a,c,e</sup>
Insertion	-	[[ ]] <sup>a,c,e</sup>

#### 6.3.3.2.7 SPI Interface Channel Level Protocol

SPIP is based on RSPE and is a sequence of RSPE frames. It has all the functionality of RSPE with the following additional error detection methods:

Error Type	Inherent Defenses	Added Defenses
Incorrect sequence	-	[[ ]] <sup>a,c,e</sup>
Unacceptable delay	Protocol delay is not dangerous because there are other mechanisms for delay checking. It is critical to read all the data stored in EEPROM without delays in STARTUP Mode. There are special mechanisms to control such delays outside the communication protocol (i.e., DiagData Controller - Fault Processing Block) and to trip the Module to FAULTED Mode (Level I fault).	-

#### 6.3.3.2.8 UART Interface Channel Level Protocol

UICP is based on RPU and is a sequence of RPU frames. It has all the functionality of RSPE with the following additional error detection methods:

Error Type	Inherent Defenses	Added Defenses
Unintended repetition	Repetition is not dangerous. Same data will be re-stored in same addresses two or more times	[[ ]] <sup>a,c,e</sup>
Incorrect sequence	Is not dangerous. Order in which data will be stored is not crucial. It is only crucial to store whole data package. During STARTUP Mode, data is read and checked for integrity using CRC-64 calculated (including frame number). Important to write data to proper address with correct CRC-64.	[[ ]] <sup>a,c,e</sup>





## 6.4 Platform Diagnostics

Each RadICS Module of RadICS Platform has built-in self-diagnostics capabilities. Automated tests are executed continuously during system operation. These tests include data integrity checking that is performed on each of the following general processes: data transmission, data reading/writing, and data processing.

Each RadICS I/O Module has its own diagnostic controller that gathers the internal diagnostic data and sends it to the LM. The LM diagnostic controller gathers the internal LM diagnostic data and sends it and the I/O Module diagnostic information to the MATS through a one-directional transmission line.

When a failure is detected, a generalized fault signal is sent to the MATS interface and other user specified alarm systems. These alarms allow maintenance personnel to quickly determine the place, time, character, and hazard degree of the failure.

The RadICS Platform self-diagnostic testing features are designed to be independent from the executing control functions. Performance of the self-diagnostic testing, as well as failures of self-diagnostic testing features, do not affect the performance of the rest of the RadICS Platform system, and do not deteriorate its performance. The self-diagnostic test results can influence the RadICS Platform operation (e.g., Type I fault detection will transition a RadICS Module to FAULTED Mode).

Self-diagnostics are performed by both the Application and Platform ED levels and are aimed at different types of faults. Failures detected by either level that are potentially unsafe are converted to safe failures. The RadICS Modules perform the self-diagnostics and take safe-state action. This involves Application Logic where feasible (i.e., it is competent to take such action) to allow the end user to specify the actions taken in the event of certain failures. The Modules are designed with redundant components where needed to permit self-diagnostic tests and data redundancies are used to permit detection of data corruption with very high probability. The RadICS Platform detects the presence of non-safety Modules during the self-diagnostics at startup and will maintain the safe state if any such Modules are detected.

Continuous automatic monitoring, as well as failures of the RadICS Platform diagnostic features do not affect the operation of the rest of the RadICS Platform system, and do not deteriorate its performance. This is attained due to the diagnostic features independent of the features executing control functions.

The RadICS Platform built-in self-diagnostics support the predictability and repeatability of the design, that satisfy the system integrity requirements of IEEE Std 603-1991 Section 5.5 and IEEE Std 7-4.3.2-2003 Sections 5.5.1, 5.5.3, and 5.6. The RadICS Platform built-in self-diagnostics capabilities facilitate timely recognition, location, replacement, repair, and adjustment of malfunctioning equipment, which satisfy the repair requirements of IEEE Std 603-1991 Section 5.10.

### 6.4.1 General Diagnostics Concept

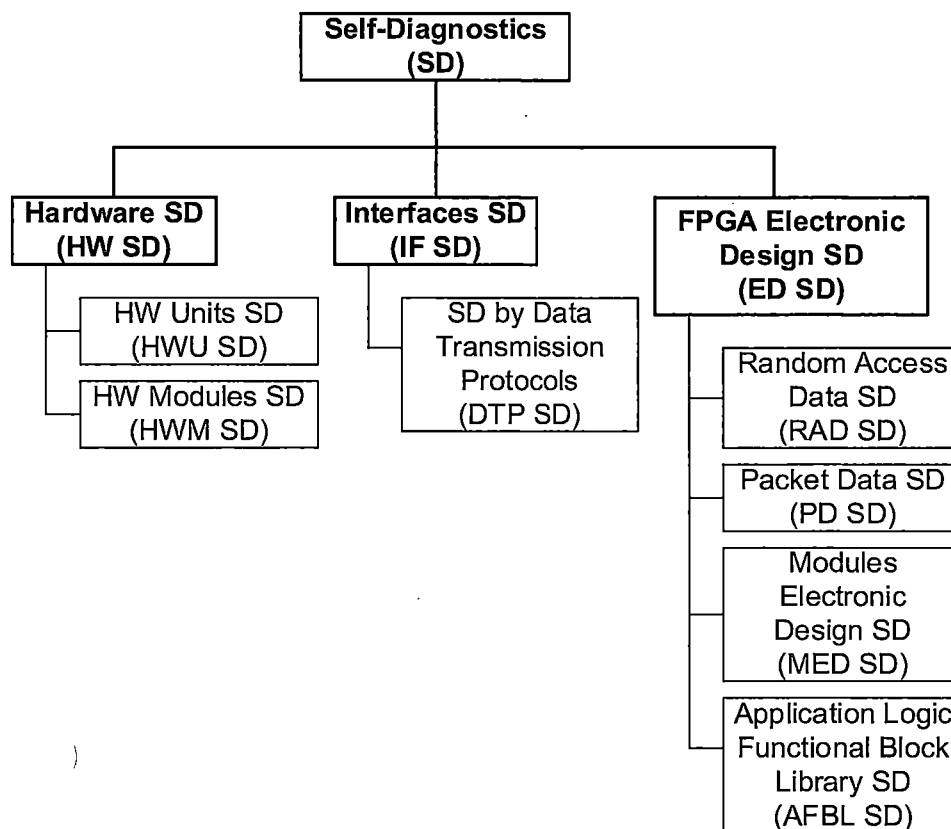
Techniques for safety integrity and functional safety assurance that are used in RadICS Platform can be divided into three main groups:

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- Hardware Self-Diagnostics
- Interfaces and Data Transmission Self-Diagnostics
- Platform EDs Self-Diagnostics

All self-diagnostic parts are integrated with each other. Figure 6-28 illustrates the self-diagnostics technique classification.



**Figure 6-28: Self-Diagnostics Techniques Classification**

HW SD includes the following:

- [[

]]<sup>a,c,e</sup>

IF SD includes the following:

- [[

]]<sup>a,c,e</sup>



Electronic Design Self-Diagnostics (ED SD) includes the following:

- [[

]]<sup>a,c,e</sup>

Faults detected by self-diagnostics can be divided into three types at a Module level and at a system level.

At the Module level:

- Type I Faults – Platform control logic could not guarantee trip to safe state (e.g., a self-diagnostic test detects an FPGA fault). [[
- Type II Faults – Hardware or part of ED cannot properly perform its functions [[

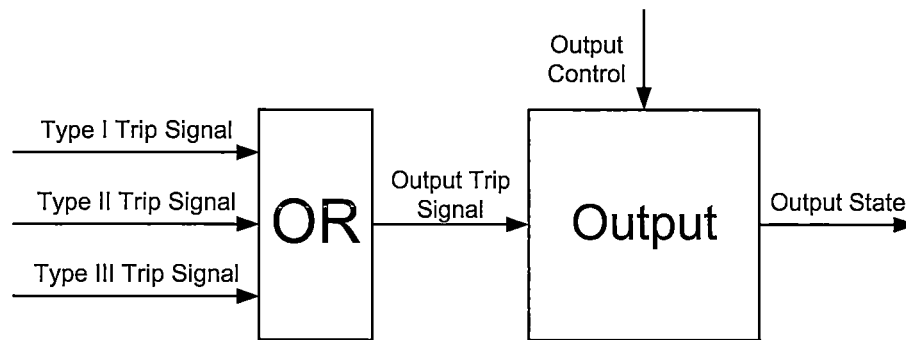
]]<sup>a,c,e</sup>

- Type III Faults – User defines criticality of detected errors and their processing algorithm (performed by Application Logic). Platform and Application ED can guarantee trip to safe state (e.g., an out-of-range input, a failed input channel, or a failed input Module (whatever the cause) in which case the Application Logic decides how serious the failure is).

At the system level:

- Input Module Faults – If an input Module suffers a Type III Fault, the Application Logic in the LM can decide (by Application Logic) how to manage it, as specified by the end user's functional requirements).
- Logic Module Faults – If the LM suffers a Type I or Type II fault, all outputs are driven to the safe state.
- Output Module Faults – If an output Module detects a Type I fault, it is de-energized and the LM will trip to the safe state when it detects the loss of communication with the de-energized output Module. If an output Module detects a Type II fault, it will drive its outputs to the safe state and report this to the LM. If an output Module detects a Type III fault, the Application Logic in the LM can decide (by Application Logic) how to manage it, as specified by the end user's functional requirements).

So, there are three ways to trip a RadICS Platform-based system into a safe state. Each of them can perform trip of outputs. Figure 6-29 illustrates this safety feature.



**Figure 6-29: Ways Outputs Can Trip to Safe State**

Table 6-6 lists faults detected by the RadICS LM.

**Table 6-6: Faults Detected by RadICS LM**

Fault Type	Detected Fault
Type I	<ul style="list-style-type: none"> <li>• []</li> </ul>



Fault Type	Detected Fault
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Fault Type	Detected Fault
Type II	<ul style="list-style-type: none"><li>• <math>\mathbb{I}^{\text{a,c,e}}</math></li></ul>





Fault Type	Detected Fault
	<div>]]<sup>a,c,e</sup></div>
Type III	<div><ul style="list-style-type: none"><li>• [[</li></ul></div>



Fault Type	Detected Fault
	<p style="text-align: right;">]]<sup>a,c,e</sup></p>

The self-diagnostic performance requirements are:

- [[

]]<sup>a,c,e</sup>

### 6.4.2 Hardware Self-Diagnostics

HWU SDs are described in Section 6.2.5.2. HWM SDs are described in Section 6.2.6.

### 6.4.3 Interfaces and Data Transmission Self-Diagnostics

IF SD of communications is crucial for providing safety integrity and functional safety. IF SD is performed by Platform ED SD, since interfaces cannot perform any actions except data transmission.

Generalized measures intended to provide IF SD are:

- [[



]]<sup>a,c,e</sup>

DTP SD, due to the specific structure of each protocol, allow implementation of reliable IF SD. Each transmitted data packet includes the following data:

- [[

]]<sup>a,c,e</sup>

The identification information in the transmitted data packets, which carries source and sink of information (i.e., Module type, protocol, protocol version, optical communication descriptor, etc.) allows for verification that the information was generated by a proper source, has an appropriate format, and sent to the correct Module will be accepted.

The numerator information in the packet allows for verification that all the received data packets refer to the same data transmission cycle. Adding the numerator (i.e., 16 bit counter that increments every 5 millisecond work cycle) to the data for CRC calculation increase static error detection capability. Even if the data are static and there is a static error in memory or a in data transmission path that cannot be detected in this work cycle, the CRC will be changed in next work cycle and error will be detected. Data are encoded (inverted or not) by numerator's LSB, so even if data are static during at least two work cycles memory cells and data paths will be diagnosed if they are stuck in one state. Adding the address to the data for CRC calculation gives the assurance that data was stored in right memory cell and that data were read from right memory cell. The Numerator's LSB is stored with data and CRC in memory, so it can be unambiguously defined whether data are new or old (from previous work cycle) by comparing stored LSB with current LSB. Numerator monotony control allows for detection of missed data transmissions.

[[

]]<sup>a,c,e</sup>

DTP SDs are implemented by ED SD facilities, as interfaces themselves are not able to implement necessary activities. DTP SD is assured by using the following techniques:

- [[

]]<sup>a,c,e</sup>

In such a way, each interface is covered by diagnostics to provide safety integrity and functional safety.

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#### 6.4.4 FPGA ED Components Self-Diagnostics

The RadICS Platform ED SD directly receives, processes, and conditions data for RadICS Platform operation. ED SD includes:

- Random-access data self-diagnostics (RAD SD)
- Packet data self-diagnostics (PD SD)
- Modules electronic design self-diagnostics (MED SD)
- AFBL self-diagnostics (AFBL SD)
- Data Transmission Protocols (DTP SD)
- EEPROM data compatibility check

##### 6.4.4.1 *Random-Access Data and Packet Data Self-Diagnostics*

RAD SD is intended for random-access data integrity diagnostics while transmission, storing, reading, and writing. The following characteristics are included in RAD SD:

- [[

]]<sup>a,c,e</sup>

PD SD is intended for the packet data integrity self-diagnostics while transmission, storing, reading, and recording. The following characteristics are included in PD SD:

- [[

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]]<sup>a,c,e</sup>

**6.4.4.2    Module Electronic Design Self-Diagnostics**

MED SD includes several self-diagnostics techniques:

- [[

]]<sup>a,c,e</sup>

Application of RAD SD or PD SD to all the data within the ED provides self-diagnostics coverage for all PFBL elements that were used for the creation of the ED and through which data are transmitted (e.g., memory, multiplexer, controllers, etc.). The following characteristics are included in RAD SD or PD SD:

- [[

]]<sup>a,c,e</sup>

Figure 6-30 shows how RAD SD is used for data path diagnostic coverage.



[[

]]<sup>a,c,e</sup>

Figure 6-30: RAD SD Usage for Providing MED SD

[[

]]<sup>a,c,e</sup>. By this method, diagnostics on “stuck at” state of components and data paths are provided even with static input data.

DP2 diagnostics component implements the following functions:

- [[



]]<sup>a,c,e</sup>

DP5 diagnostics component implements the following functions:

- [[

]]<sup>a,c,e</sup>

DP6 diagnostic component implements the following functions:

- [[

]]<sup>a,c,e</sup>

Figure 6-31 shows how PD SD is used for data path diagnostic coverage.

[[

]]<sup>a,c,e</sup>

Figure 6-31: PD SD usage for providing MED SD

[[





]]<sup>a,c,e</sup>

#### **6.4.4.3     *Application Logic Functional Block Library Self-Diagnostics***

[[

]]<sup>a,c,e</sup>

Figure 6-32: Approach for Assuring AFBL Integrity

#### 6.4.4.4 Data Transmission Protocols

DTP SD is implemented by ED SD facilities, as interfaces themselves are not able to implement the necessary SD activities. DTP SD is assured by using the following techniques:

- [[

]]<sup>a,c,e</sup>

By using these methods each interface is covered by diagnostics to provide safety integrity and functional safety.

#### 6.4.4.5 EEPROM Data Compatibility Check

A unique ID (i.e., 64-bit hash code) is stored in the Tuning, Application Netlist, and Configuration EEPROMs. These unique IDs are read during STARTUP mode and compared to ensure match for the chassis, as a safety critical function. They continue to be compared during other modes but these comparisons are not treated as safety critical.

### 6.5 Redundancy

The RadICS Platform modular architecture is convenient for building redundant systems. RadICS Platform provides for three kinds of redundancy management:

- Architecture-based active redundancy management: Safety I&C systems typically are comprised of several separate, independent divisions (typically three or four). Output signals from each

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division are issued through output boards into the hardware voting logic or via communications links to inter-divisional voting divisions (e.g., ESFAS voters) depending on system architecture. The degree and architecture of redundancy is dictated by reliability requirements imposed on the application. The RadICS Modules can be configured as single channels, voting logic configurations, such as 2-out-of-3, 2-out-of-4, or variations of these configurations. The general design principle of the redundant architecture is to comply with the single failure criterion provided in IEEE Std 379-2000 (Reference 6-6).

- Hardware-based active redundancy management: Redundancy is built into the hardware for inputs, outputs, and power supplies.
  - For inputs, the ADC, WADC, TDC, or RTD Units provide redundancy of input analog signal results after analog-to-digital conversion and the analog signal is also transmitted to the redundant Unit for scaling and filtration and analog-to-digital conversion.
  - For outputs, the safety concept is based on 1-out-of-2 taken twice redundancy for de-energize to trip, plus testing of individual switches. To open the discrete output, all four switches are opened; however, at least one in each pair must open. Once a safety condition is detected by the application or the platform, all four outputs are de-energized.
  - For power supplies, the PSWD Unit receives redundant 24 VDC power supply and is used for its converting into the voltage levels (for example into +1.2 V, +3.3 V, etc.), necessary for all RadICS Module operation.

The criteria establish that no single failure will result in loss of any of the safety functions. RadICS Platform-based systems can be configured to meet these requirements using the standard RadICS Modules, which will satisfy U.S. requirements for single failure tolerance defined in IEEE Std 603-1991 Section 5.1, RG 1.53 (Reference 6-7), and IEEE Std 379-2000.

## 6.6 Independence

The RadICS Platform and applications meet independence requirements by incorporating features to ensure, physical and functional separation between redundant devices performing safety functions. By implementing these design features, the RadICS Platform systems maintain their required safety functions in the presence of a single fault in any of their components.

The RadICS Platform design incorporates the following features: galvanic isolation and shielding of input, output and power supply circuits in each channel using electrical or optical isolation devices; physical separation (using distance, barriers, or both) between redundant channels, independent redundant power supplies, physical and functional separation of devices performing safety and non-safety functions.

Physical and functional independence of communication channels is achieved by selecting appropriate system architectures and data communication protocols. The implementation of radial (point-to-point) architecture in our interchannel communication links provides us with the capability to maintain failure-

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free data exchange between I&C components even when one of the channels has failed. Additional measures designed to achieve the desired physical and functional independence are the application of fiber-optic communication lines for data exchange between I&C components and the separation of safety and control functions from information and diagnostic functions. The interface to the MATS is one-way broadcast via a fiber optic link controlled by the RadICS Platform.

These independence features also satisfy U.S. requirements for independence defined in IEEE Std 603-1991 Section 5.6, RG 1.75 (Reference 6-8), and IEEE Std 384-1992 (Reference 6-9).

Physical and functional independence of functional elements on the Module FPGA is established for each channel and each monitoring element during the development of the ED AD for each RadICS Module. The functional elements include bond wires and pin-out and their own separated inputs and outputs that are not routed through another channel or functional element. The Project ED Design Procedure specifies that for each FPGA design element that requires physical and functional independence, create a logical design partition for that design element and assign the design partition to a LogicLock location constraint. These constraints are implemented using the Quartus II development tool.

The RadICS Platform independence features satisfy the independence requirements of IEEE Std 603-1991 Section 5.6 for the RadICS Platform equipment. The RadICS Platform isolation features also satisfy IEEE Std 384-1992, as endorsed by RG 1.75, Revision 3. The RadICS Platform communication independence features satisfy the system independence requirements of IEEE Std 7-4.3.2-2003 Section 5.6.

## **6.7 Safety Override Operation**

The SOR is a supplementary safety function of the RadICS Platform that permits a temporary override to safe-state values of the safety-critical outputs of the system when the SOR is set and allows a return to normal operation when the SOR is reset. The SOR may be used under administrative control to manually set RadICS Modules to a safe state while a maintainer is working in the rack. It can also be activated by the Application Logic, as specified by the end user's functional requirements.

The SOR can be set (i.e., outputs are set to the safe state) under any of several conditions and can be reset only by operator (or hardwired) action when all setting conditions are clear.

The SOR is quite different from the FAULTED mode. In FAULTED mode, the RadICS Platform is irrevocably driven to the safe state, and this can be recovered only by powering down and powering-up the RadICS Chassis or LM. In contrast, the SOR can be reset by the operator if the setting conditions have been cleared. Every Module that contains output channels (e.g., LM, AOM, and DOM) includes the SOR capability.

The Set-SOR function always takes precedence over the reset SOR function.

The SOR is set globally (i.e., it affects all output Modules) under any of the following conditions:

- By RadICS Platform Logic during STARTUP mode
- By Application Logic, as specified by the end user's functional requirements



- By external hardware setting 2-out-of-3 of the Set-SOR input contacts to the LM and every DOM/AOM
- By external hardware setting 2-out-of-3 of the Set-SOR input contacts to the LM only. The LM communicates this to all output Modules.

The SOR is set locally (i.e., to affect only the specific output Module) under any of the following conditions:

- By Application Logic, as specified by the end user's functional requirements
- By external hardware setting 2-out-of-3 of the Set-SOR input contacts to 1 or more DOM/AOM

The SOR is reset globally under either of the following conditions:

- By closing the Reset-SOR input contacts to LM and all I/O output Modules one-time (momentary contact) and closing Set-SOR input contacts to LM and all I/O output Modules on continuing basis (continuous contact) or Set-SOR contacts stay closed (if setting SOR was performed by RadICS Platform ED).
- By closing the Reset-SOR input contact to the LM and closing Set-SOR input contacts if none of the SOR-setting conditions is currently set.

The SOR is reset locally under all the following conditions:

- By closing the Reset-SOR input contacts and closing Set-SOR input contacts to the specific DOM/AOM or DOMs/AOMs if none of the global SOR-setting conditions is currently set, none of the local SOR-setting conditions is currently set, and the LM SOR is not set.

Figure 6-33 shows the functional diagram of the SOR Unit.



[[

]]<sup>a,c,e</sup>

**Figure 6-33: Functional Diagram of SOR Unit**

The set safety override inputs are normally “high” because the Set-SOR keyswitch is closed. When the operator opens the Set-SOR keyswitch, the safety override inputs drop and the flip-flop resets to open the power switch and de-energize the output Units connected to it. Similarly, a Set-SOR from the FPGA will also open the power switch and de-energize the output Units connected to it.

The 2-out-of-3 Set-SOR switch logic is used to provide immunity from spurious operation.

The FPGA Unit detects disagreements when SOR keys are set but SOR state signal shows not set and generates a Type I fault.

The use of the SOR feature can be remotely monitored from the control room and therefore there is an independent check that authorized access to the system is following safe practices.

The RadICS Platform SOR facilitates testing and timely replacement and repair of malfunctioning equipment, which satisfies the test, calibration, and repair requirements of IEEE Std 603-1991 Sections 5.7 and 5.10.



## 6.8 PSWD Operation

The PSWD Unit receives redundant 24 VDC power supplies and converts them into the voltage levels necessary for Module operation. PSWD Unit can detect a failure of either 24 VDC source and use the operating one. PSWD Unit applies overvoltage protection for the voltages converted from the 24 VDC supplies. PSWD Unit provides diagnostics for power supply failures to the FPGA.

[[

]]<sup>a,c,e</sup>

Figure 6-34 provides the functional diagram of the PSWD.

[[

]]<sup>a,c,e</sup>

**Figure 6-34: Functional Diagram of PSWD Unit**

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[[

]]<sup>a,c,e</sup>

The Voltage Supervisor and Watchdog CPLD performs the following critical functions:

- [[

]]<sup>a,c,e</sup>

PSWD design feature ensures that the critical PSWD Unit functions can be performed independently of FPGA failures. Every RadICS Module has a PSWD Unit.

The RadICS Platform PSWD Unit supports the predictability and repeatability of the design, which satisfies the system integrity requirements of IEEE Std 603-1991 Section 5.5 and IEEE Std 7-4.3.2-2003 Section 5.5.1.

**6.9 Access Control Features**

The RadICS Platform has the following features to fulfill the access control requirements:

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- RadICS Platform Chassis and cabinets with access control keys and alarm features
- Using unique identifiers for RadICS Modules to prevent substitution by malicious intention or by mistake

The keyswitches associated with a RadICS Chassis are shown in Figure 6-35. These contribute to preventing and detecting failures and maintenance errors.

The TUNING keyswitch is typically mounted on the RadICS Chassis and is connected directly to a dedicated contact input on the LM. The ARMED Keyswitch operates a dry contact supplied by end user is used by the RadICS Platform. It may be driven by any secure means (e.g., keyswitch). The dry contact is used to indicate that the end user downstream safety logic is secured in safe state. The ARMED key contact is connected to a designated input on LM. The keyswitches can be mounted anywhere that is convenient to the end user and consistent with their functions.

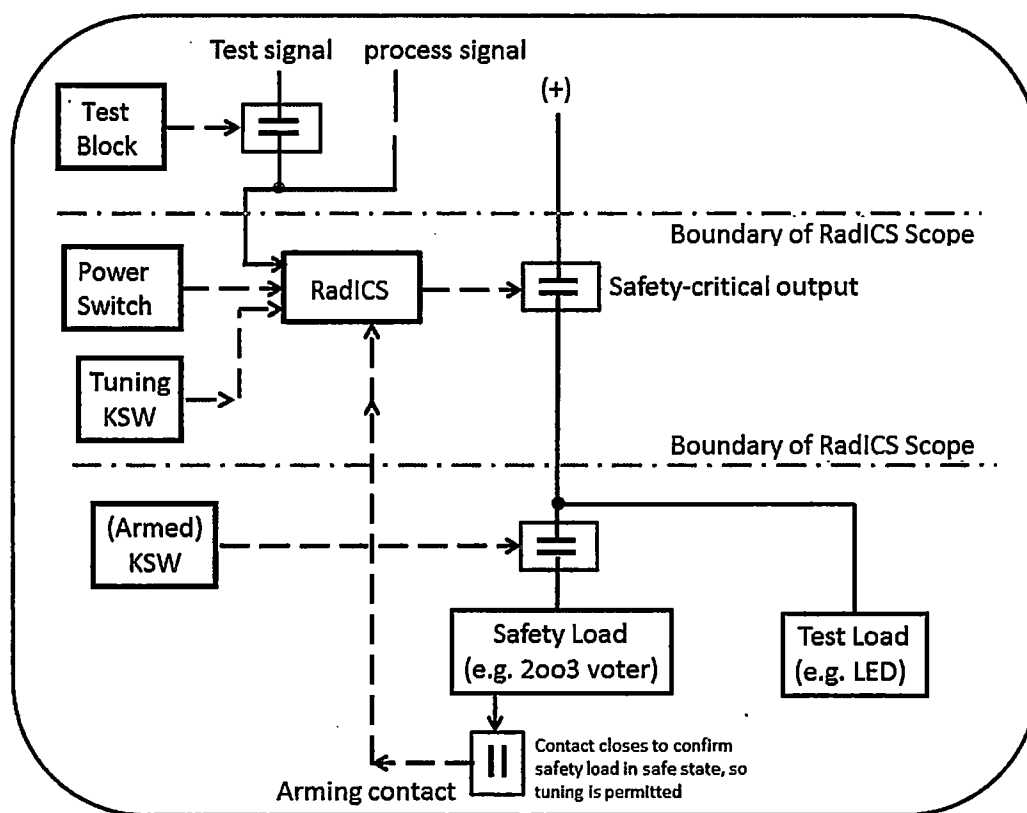


Figure 6-35: RadICS Keyswitch Access Control Features

The TUNING keyswitch is typically controlled by the control room staff. This keyswitch must be present and turned to the “tune” position for the RadICS Module to provide power internally to the designated



tuning port used to connect the MATS Tuning PC. The RadICS Platform logic reads this port only when the keyswitch is in the "tune" position. The tuning activity is signaled to the MATS in the control room.

The ARMED keyswitch is used to permit complete testing of single or multiple safety functions within the RadICS Platform system. The keyswitch is used to force all safety field outputs of the RadICS Platform to the safe state regardless of the state of the RadICS Platform outputs. A contact from this logic is provided to the RadICS Platform to indicate the safety load is in the safe state. The end user uses the ARMED keyswitch to place the RadICS Platform field outputs in the safe state whenever tuning the RadICS Platform Application ED and to test the effects of the tuning changes before putting the RadICS Platform channel back online. The ARMED keyswitch circuit allows for complete testing by varying the input parameters through their complete range from non-trip conditions into trip conditions while the plant equipment is in the safe state.

To enable the vendor to configure the RadICS Platform (i.e., to define the Application Logic to be implemented in the Module ED), there is an additional JTAG connector interface at the LM PCB. This interface is inaccessible when the Module is installed in a Chassis and it only allows configuration of the Application ED in an off-line mode. Removal of the Module from the Chassis will cause the RadICS Platform to drive all safety outputs to the safe state. Since the JTAG connector is the only means to change the Application ED configuration of the Module, the system is protected from such errors whether accidental or intentional.

The software used in configuring process of the RadICS Platform contains password protection features, as well as functions to check the successful completion of the configuration process.

The RadICS Platform control of access features satisfy the control of access requirements of IEEE Std 603-1991 Section 5.9.

## 6.10 Timing Diagrams and Working Cycles

The RadICS Platform performs initialization when the Chassis transitions from POWERED-OFF mode to STARTUP mode. Initialization time should take not more than  $[[ \quad ]]$ <sup>a,c,e</sup>. After initialization, Work Cycles are performed cyclically. During a Work Cycle, all functions of the RadICS Platform are performed. A Work Cycle duration is  $[[ \quad ]]$ <sup>a,c,e</sup>.

A RadICS Platform Work Cycle consists of the following Phases:

Input Data Receive (IDR)	Receive input data from the I/O Modules for the current Work Cycle and perform application test logic code.
Application Logic Processing and Configuration (AppLPrc and CFG)	Application Logic processing and generation of I/O Module data packets
Output Data Transmission (ODT)	Transmission of Application Logic processing results to the output Modules.
Switch Time (ST)	Switching time for the output Modules.



The timing allocations provided for each Phase are:

- [[ ]] <sup>a,c,e</sup> is allocated to receive and transmit the data from the input Modules (i.e., AIM and DIM) to the LM. This time is allocated to implement a full cycle of input data processing (i.e., hardware operation, data processing, and transmission to LM). Application test logic code is performed during this time.
- [[ ]] <sup>a,c,e</sup> are allocated for Application Logic processing in the LM. This time is allocated to execute Application ED (i.e., process input data and form output data).
- [[ ]] <sup>a,c,e</sup> is allocated to transmit the results of Application Logic processing from LM to the output Modules (i.e., AOM, DOM, and OCM). This time is allocated to read the results of Application Logic processing from the LM output memory and transmit the data to the output Modules.
- [[ ]] <sup>a,c,e</sup> is allocated for output Module switching. This time is allocated for switching of the output elements of the output Modules (e.g., field-effect transistors, relay, etc.).

The AFBL SD testing described in Section 6.4.4.3 is performed in all Phases except the Application Logic Processing and Configuration Phase.

The Work Cycle time parameters are different for each I/O Module because of differences in Module hardware and functionality, as shown in Table 6-7.

**Table 6-7: Timing Requirements for RadICS I/O Modules**

Module	Time Allocation	Parameters
AIM and WAIM	[[ ]]	<sup>a,c,e</sup>
DIM	[[ ]]	<sup>a,c,e</sup>
AOM	[[ ]]	<sup>a,c,e</sup>
DOM	[[ ]]	



Module	Time Allocation	Parameters
		]]a,c,e
OCM	[[	]]a,c,e
TIM	[[	
RIM	[[	
		]]a,c,e

The operation timing diagram of a single RadICS Platform Chassis is shown in Figure 6-36.

[[

]]a,c,e

Figure 6-36: Operation Timing Diagram of a Single RadICS Chassis



The operation timing diagram for communication between two RadICS Platform Chassis is shown in Figure 6-37.

[[

]]<sup>a,c,e</sup>

**Figure 6-37: Operation Timing Diagram for Two RadICS Chassis**

Figure 6-37 demonstrates that one OCM-OCM communication between Chassis adds to response time up to 5 milliseconds. If a signal passes through more than two Chassis, then the timing can be calculated individually by keeping in mind that an OCM receives data from the LM in the ODT Phase and transmits data to the LM during the IDR phase.

The RadICS Chassis operate asynchronously with each other. Because of small variations in the platform clocks, it is possible that data from the sending Chassis may not be updated for the next Work Cycle of the receiving Chassis. This case can occur if the receiving Chassis is running slightly faster than the sending Chassis. In this case, the receiving Chassis may still have the old input data, which is outdated. It will take a second Work Cycle until updated (valid) data are processed. Consequently, the [[

]]<sup>a,c,e</sup>

The RadICS Platform Work Cycle features support the predictability and repeatability of the design and satisfy the system integrity requirements of IEEE Std 603-1991 Section 5.5 and IEEE Std 7-4.3.2-2003 Section 5.5.1. The Work Cycle features also address the BTP 7-21 review guidance regarding allocation of system timing requirements to the digital computer portion of the system.

## **6.11 Periodic Testing**

The RadICS Platform has extensive self-diagnostic testing features. These tests can be supplemented with application specific engineered test features and engineered end-point equipment actuation tests that are performed as a series of overlapping tests to satisfy the requirements of IEEE 603-1991 Section 5.7. The self-diagnostic testing is performed continuously during operation of the RadICS Platform. Most other surveillance tests can be engineered to be semi-automated (i.e., features design to assist maintenance or operators in the task) for completion during power operation. [[

]]<sup>a,c,e</sup>

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The testing features for the RadICS Platform are described in the context of the typical surveillance tests required by plant Technical Specifications (Reference 6-10):

- Channel Check
- Channel Calibration
- Channel Operational Test
- Actuation Logic Test
- Response Time Test

The RadICS Platform performs a large portion of these tests automatically during operation without the need for human interaction either through inherent platform self-diagnostics or engineered solutions. For testing that must be performed manually or during refueling outages, the RadICS Platform offers solutions that can automate aspects of the testing process to reduce human error and reduce the time required to perform the tests. Figure 6-38 shows the series of overlapping surveillance tests that are used to verify the performance and operability of a RadICS Platform.





[[

]]<sup>a,c,e</sup>

**Figure 6-38: RadICS System Periodic Surveillance Test Coverage**

### **6.11.1 Channel Check**

A Channel Check, required by plant Technical Specifications, is a qualitative assessment of channel behavior during plant operation. The determination includes the comparison of indication and status of independent instrument channels measuring the same parameter. On existing systems, the parameter comparisons are typically performed manually channel by channel once per shift by plant operators. The RadICS Platform can provide engineered solutions to perform the Channel Checks automatically on a continuous basis and provide notification to the operators when ranges or deviations between channels exceed the established acceptance criteria.

[[

]]<sup>a,c,e</sup>

Automation of the Channel Checks using the RadICS Platform features can be used to replace the manual Channel Checks performed once per shift by plant operators. Automation of the Channel Checks can improve detection of sensor problems and better focus operator response to instrument channel failures or sensor calibration drift that may impact system and plant performance.

### 6.11.2 Channel Calibration

A Channel Calibration required by plant Technical Specifications is the adjustment, as necessary, of a channel output such that it responds within the necessary range and accuracy to known values of the parameter that the channel monitors. [[

]]<sup>a,c,e</sup> As required, channels being calibrated may be placed in bypass during testing to prevent influence of the safety function or actuation of system outputs.

### 6.11.3 Channel Operational Test

The Channel Operational (or Functional) Test required by plant Technical Specifications is a test of all required logic components to verify channel operability, including required alarm, interlock, display, and trip functions, and channel failure trips. This test includes verifications, as necessary, such that the setpoints are within the necessary range and accuracy. The Channel Operational Test may be performed by means of any series of sequential, overlapping, or total channel steps so that the entire channel is tested.

For a RadICS Platform based system, the Channel Operational Test is accomplished by a series of overlapping tests that ensure the operability of the entire system. [[

]]<sup>a,c,e</sup>

The Module self-diagnostic and communication interface testing is performed continuously during operation of the RadICS Platform. Automation of the Channel Operational Tests using the RadICS Platform features can be used to replace the manual Channel Operational Tests performed by plant maintenance technicians. These features simplify the required maintenance support necessary and increase the amount of diagnostic testing performed during operation while minimizing the potential for plant transients caused by maintenance or testing errors during plant operation. [[

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]]<sup>a,c,e</sup>

#### **6.11.3.1 Input Operability Test**

The Input Operability Tests verify the operability of discrete/binary input channels of each input channel to an installed RadICS Platform-based system (complementary to Channel Calibration). This test is an engineered solution that considers the required surveillance period and whether testing during power operation is required or if testing can instead be completed during refueling outages. The general concept is as follows:

- Input channels are tested by injection of test signals in the input circuits. This testing may be performed via existing plant signal injection methods or by a test cart designed to automate the task.
- Correct operation of the input circuits may be verified automatically using a test cart interface or by signals monitored by the MATS.
- As required, input signals/channels may be placed in bypass during testing to prevent influence of the safety function or actuation of system outputs.

#### **6.11.3.2 Continuous Self-Diagnostic Tests**

The RadICS Platform self-diagnostic and test features continuously perform the surveillance activities that are required during power operation to verify setpoints and the protection system trip actuation capability. The RadICS Platform self-testing features are an integral part of each Module design, as described in Section 6.4. [[

]]<sup>a,c,e</sup>

The correctness of self-diagnostic and test features has been verified during the V&V activities described in Section 7.4.

#### **6.11.3.3 Communication Monitoring and Diagnostics**

Communication Monitoring and Diagnostics are a subset of the overall module self-diagnostic and test features. Much like the continuous self-testing of the ED trip functions, communications within channels and between channels are continuously monitored during operation to detect incorrect behavior and unsafe conditions, as described in Section 6.4. [[

]]<sup>a,c,e</sup>

The correctness of Communication Monitoring and Diagnostics features has been verified during the V&V activities described in Section 7.4.

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#### 6.11.4 Actuation Logic Test

Actuation Logic Test required by plant Technical Specifications is the application of various simulated or actual input combinations in conjunction with each possible interlock logic state required for operability of a logic circuit and the verification of the required logic output. The Actuation Logic Test includes a check of output devices.

The automated tests can be engineered to be overlapping to the extent required by plant surveillance requirements, required surveillance times, and impact on plant status while the plant is operational. The Actuation Logic Test can be completed in two overlapping segments:

- Output Circuit Test - The application of various simulated or actual input combinations to determine the operability of an output logic circuit pathway (the output module, interposing relays, and check-back circuits as applicable) without actuating the end component.
- End Component Test - Verification of the operability by actuation of the end devices.

##### 6.11.4.1 Output Circuit Testing

Tests of the RadICS Platform-based system output logic pathways may be determined to be necessary during plant operations to support surveillance timeframes. In some cases, the end devices must not be actuated during power operation of the plant. Either through simulated inputs or designed output test logic, the RadICS Platform-based safety system can support or even automate a test of these output circuit pathways, while ensuring the end component is not actuated. Typically, this involves test up to the interposing relay between the RadICS Platform equipment and the end component actuation circuits. These output circuits can include checkback logic to help to automate the Output Circuit Testing.

The very fast cycling capability of the of DOs in the DOM Module support partial valve stroke testing. Valves are tested to move off their full open or full closed parked position and this action is timed. The operation is terminated fast enough to not disturb the process.

##### 6.11.4.2 End Component Testing

To complete the testing of any system, it is necessary to actuate and verify the operability of the end components. This test may be completed online if plant conditions allow for the test to be completed without causing an unsafe condition in the plant. These tests are performed in accordance with plant Technical Specifications.

#### 6.11.5 Response Time Tests

The Response Time Test verifies the time interval from when a monitored parameter exceeds its trip setpoint until the required safety action is completed. Technical Specifications allow for verification of response times in lieu of measurement for selected components provided that the components and methodology for verification have been previously reviewed and approved by the NRC.

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The RadICS Platform has a deterministic behavior. The Work Cycle for each Module is fixed and the maximum response time for system architecture is established using the maximum response time of each LM and communication links. This deterministic behavior guarantees that safety outputs will always be delivered within the computed maximum response time limit. See Section 6.10 for further details on Work Cycles and response times. The execution of each Module Work Cycle is continuously monitored by the PSWD Unit located on each Module, as described in Sections 6.2.5.2.2, 6.2.5.2.7, and 6.8.

## 6.12 Download Station

The DLS is physically a RadICS Platform Chassis that is identical to the in-service RadICS Platform Chassis that is installed as part of the safety-related I&C system. The DLS is used for:

- CPLD and FPGA (Platform ED) configuration
- Downloading FPGA Application Logic ED, Hardware Configuration, Service Data, and Tunable values to the LM
- Calibrating an AIM, WAIM, TIM, RIM, and AOM

[[

]]<sup>a,c,e</sup>

The DLS would then be used to configure the Configuration, Tuning, and Application Netlist EEPROMs. This configuration is performed using a proprietary Radiy configuration device and may be performed by either Radiy or the end user.

The DLS also contains an LM to interface with other Modules inserted into the DLS. This arrangement supports the calibration functions of the AIM and AOM modules, as needed, for the in-service system. The calibration of the AIM and AOM modules may also be performed by the in-service system rather than using the DLS. See Appendix A for more information on the calibration checking functions of the RadICS Platform.

The RadICS Platform DLS satisfies the test and calibration requirements of IEEE Std 603-1991 Section 5.7.

## 6.13 Chapter 6 References

- 1 IEEE Std 1012-2004, "IEEE Standard for Software Verification and Validation Plans"
- 2 IEEE Std 603-1991, "Criteria for Safety Systems for Nuclear Power Generating Stations"

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- 3 IEEE Std 7-4.3.2-2003, "Standard Criteria for Digital Computers in Safety Systems of Nuclear Power Generating Stations"
- 4 IEC 61508-2010, "Functional Safety of Electrical/Electronic/Programmable Electronic Safety-related Systems," International Electrotechnical Commission
- 5 IEC 61784-3:2010, "Industrial communication networks - Profiles - Part 3: Functional safety fieldbuses - General rules and profile definitions"
- 6 IEEE Std 379-2000, "Application of the Single-Failure Criterion to Nuclear Power Generating Station Safety Systems"
- 7 Regulatory Guide 1.53, Revision 2, "Application of the Single-Failure Criterion to Safety Systems"
- 8 Regulatory Guide 1.75, Revision 3, "Criteria for Independence of Electrical Safety Systems"
- 9 IEEE Std 384-1992, "Standard Criteria for Independence of Class 1E Equipment and Circuits"
- 10 NUREG-1431, Volume 1, Revision 4.0, "Standard Technical Specifications - Westinghouse Plants"



## 7 RadICS Platform Development Process

### 7.1 Overview of Safety Standards Used for RadICS Platform Development Process

RPC Radiy used development standards from three main international organizations for the development of the equipment dedicated as the RadICS Platform: IAEA, IEC, and IEEE.

The IAEA Safety Standards reflect international consensus on what constitutes a robust level of safety and form the basis for the IAEA safety review services and assistance. They are intended for use by all organizations involved in the nuclear industry, including operating organizations, regulatory bodies, designers, and suppliers. Safety Guide IAEA NS-G-1.3, *Instrumentation and Control systems important to safety in nuclear power plants*, provides guidance on the design of I&C systems important to safety in NPPs, including all I&C components, from sensors to actuators and final elements, operator interfaces, and auxiliary equipment (Reference 7-1). This guide supplements Safety Standards Series No. NS-R-1, *Safety of Nuclear Power Plants: Design*, which establishes the design requirements for ensuring the safety of NPPs (Reference 7-2).

Safety Guide IAEA NS-G-1.1, *Software for Computer Based Systems Important to Safety in Nuclear Power Plants*, provides guidance on the collection of evidence and preparation of documentation to be used in the safety demonstration for the software for computer-based systems important to safety in NPPs, for all phases of the system life cycle (Reference 7-3).

The IEC uses IAEA safety guides (mainly NS-R-1, NS-G-1.3, and NS-G-1.1) as guidelines for development of I&C systems important to safety. IEC standards provide guidance for the implementation in the design of basic safety principles.

IEC 61508, *Functional safety of electrical/electronic/programmable electronic safety-related systems*, (Reference 7-4) outlines industry best practices to be followed during the entire lifecycle of programmable electronic systems to reduce the risk of systematic failures to an acceptable level. IEC 61508:2010 addresses all aspects of the lifecycle of electrical/electronic/programmable devices in safety-related applications, regardless of the technology (FPGA or other).

IEC 61513:2001, *Nuclear power plants – Instrumentation and control systems important to safety – General requirements for systems*, (Reference 7-5) establishes the relationship between NPP safety objectives, requirements for the overall architecture of I&C systems, and requirements of the individual systems important to safety. This standard uses the main principles of IEC 61508:2010 to introduce requirements applicable to computer-based I&C systems and equipment that are used to perform functions important to NPP safety.

IEC 60880, *Nuclear power plants – Instrumentation and control systems important to safety – Software aspects for computer-based systems performing category A functions*, (Reference 7-6) addresses computer-based I&C software. IEC 60880:2006 addresses the following topics:

- Introduces the concept of software lifecycle and details the concept of system safety lifecycle of digital systems given in IEC 61513 to the software portion of the I&C system

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- Recommends good practices related to activities, such as: development of safety applications software, software verification processes, software modification, qualification and configuration control procedures, and tools application requirements
- Prescribes the adoption of I&C software development principles, such as: top-down design methods; the "V" model for software development; modularity; verification of each phase and clear and unambiguous documentation contents
- Details the I&C validation stage in IEC 61513:2001 to the software portion of the system and introduces software-specific issues to the validation process

IEC 60987:2007, *Nuclear power plants – Instrumentation and control important to safety – Hardware design requirements for computer-based systems*, (Reference 7-7) sets out the general requirements for the hardware development life-cycle of computer-based systems. IEC 60987:2007 addresses the following topics:

- establishes requirements for the I&C systems hardware and aims at ensuring consistency between system and hardware requirements
- establishes requirements for hardware development, including V&V

Taken together, IEC 61508, IEC 61513, IEC 60880, and IEC 60987 include requirements for the whole lifecycle of digital I&C systems and products. These standards are not I&C technology specific and are suitable for identification of requirements as applicable to FPGA based I&C systems at a general level.

Considering the growing trend of programmable devices in the nuclear industry, in 2006, IEC subcommittee 45A dealing with I&C for nuclear facilities, decided to create a new standard to establish requirements for the development processes to be applied to FPGA-based I&C systems performing Category A functions (equivalent to the U.S. safety-related functions). The first edition of IEC 62566, *Nuclear power plants – Instruments and control important to safety – Development of HDL-programmed integrated circuits for systems performing category A functions*, (Reference 7-8) was issued in 2011. IEC 62566:2011 addresses the following topics:

- Establishes requirements for each stage of the HPD lifecycle (requirements specification, design, implementation, verification, integration and validation) to develop highly reliable HPDs for use in I&C systems of NPPs performing safety category A functions
- Describes activities and guidelines to be followed in addition to requirements in IEC 61513:2001, for the system integration and validation of HPDs
- Adapts the basic safety principles from IEC 61508:2010 for the development of HDL-Programmed Devices
- Clarifies IEC 60880:2006 requirements considering FPGA specific features

Before IEC 62566 was published, RPC Radiy was already using many of the requirements in the development of the equipment dedicated as the RadICS Platform. RPC Radiy designers have analyzed and used many good practices that have been successfully applied in other safety critical domains (e.g., aerospace). These goods practices are described in RTCA/DO 254, *Design Assurance Guidance for Airborne Electronic Hardware*, (Reference 7-9) an aerospace standard that highlights the processes and other non-technical aspects specific to FPGA-based systems.

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Adherence to the above standards and the adoption of the best practices in the industry enables RPC Radiy to develop modern, safe, and reliable digital I&C systems.

The Radics LLC QAPD and procedures are in line with the requirements and recommendations found in international and domestic regulatory documents and the Radics LLC staff is fully trained to follow them throughout the product life cycles, as described in Chapter 3.

## **7.2 Standard Requirements in the RadICS Life Cycle**

All regulatory documents requirements and recommendations can be divided into two categories:

- Process oriented requirements: These describe processes, organizations, documentation, and concepts to be followed to achieve the desired safety levels and provide recommendations on how to avoid common mistakes and meet all established requirements.
- Mandatory safety and functional requirements: These are the main I&C safety and functional requirements that define the way the I&C system will operate and describe the NPP I&C mandatory features.

Between 1995 and 2011, RPC Radiy modernized their existing digital safety I&C technology, as described in Chapter 2. The equipment dedicated as the RadICS Platform is the third generation of nuclear I&C equipment developed by RPC Radiy. The RadICS Platform development life cycle defined in this chapter was designed to comply with international engineering practice for software for nuclear safety applications.

The following equipment, electronic designs, and software were developed for the RadICS Platform:

- Standardized Class 1E hardware Modules based on FPGA technology. The LM performs input module data acquisition, executes Application ED, and drives the output modules and process diagnostic data from all I/O Modules installed in the chassis. The I/O Modules provide interfaces with other devices (e.g., detectors, sensors, actuators, signalization devices). The functionality of each Module is driven by the ED implemented in the onboard FPGA(s).
- Standardized Class 1E EDs (i.e., programmable logic) for the FPGAs that perform the standardized functionality of the RadICS Modules
- A Class 1E FBL is used to standardize design activities, minimize the potential for human errors, and reduce the design time and cost of a RadICS Platform system while maintaining high quality. The FBL consists of pre-developed functional blocks used in the implementation of functions of a wide complexity range. Functional Blocks are written in VHDL. The FBL consists of two parts:
  - The RadICS PFBL that includes functional blocks used for the ED of the RadICS Modules (e.g., transceivers, diagnostic elements, etc.)
  - The RadICS AFBL that includes functional blocks used in the Application ED (e.g., logical, mathematical functions, time functions, etc.)
- A non-Class 1E set of tools integrated in a software development environment called RPCT. This tool can be used to configure EDs for various applications using the AFBL.

All ED associated with the RadICS Platform was developed or procured according to the RPC Radiy QMS. The RadICS Platform Class 1E ED originally was developed under the life cycle process that was established based on the guidance of the IEC 61508:2010. As described in Chapter 4, the generic RadICS

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Platform is being commercially dedicated demonstrating how the RadICS Platform ED life cycle processes comply with U.S. nuclear safety requirements. As described in Chapter 3, the dedications of the generic RadICS Platform are now maintained under a QA program that complies with 10 CFR Part 50 Appendix B.

The RPCT tools were developed by RPC Radiy. Radics LLC also uses commercial off-the-shelf tools, as discussed in Section 8.3.

### 7.3 RadICS Platform Development Process

The RadICS Platform development process consists of three stages: high-level system/platform design, Module ED development and implementation, and system integration and validation (including EQ for the RadICS Platform development).

The RadICS Platform safety life cycle model is described in Section 7.3.1. The RadICS Platform high-level design stage is described in Section 7.3.2. The Module ED and implementation stage is described in Section 7.3.3. The system integration and validation stage is described in Section 7.3.4. The RadICS Platform project-specific system high-level design stage is described in Section 7.3.5.

The RadICS Platform EQ process is described in Chapter 9.

#### 7.3.1 RadICS Safety Life Cycle

The RadICS Platform safety life cycle is based on the development model used in the IEC standards. The IEC model covers the complete cradle-to-grave life of a safety product or a safety system, as shown in Figure 7-1. The shaded parts apply to the design of a product, such as the RadICS Platform, that will be used in NPP safety-related systems.

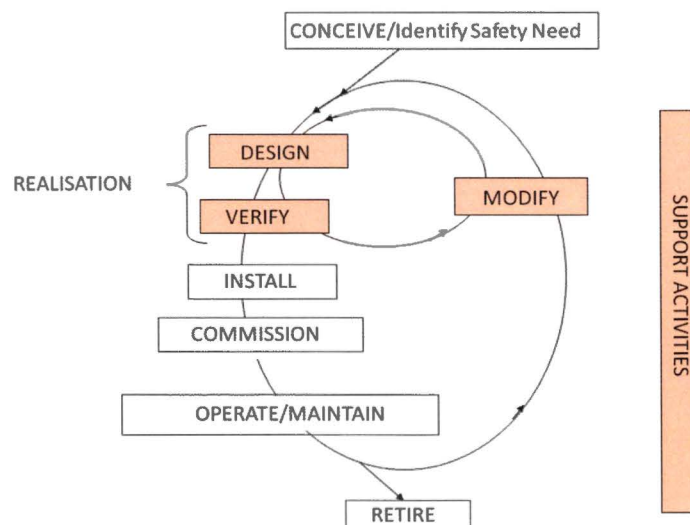


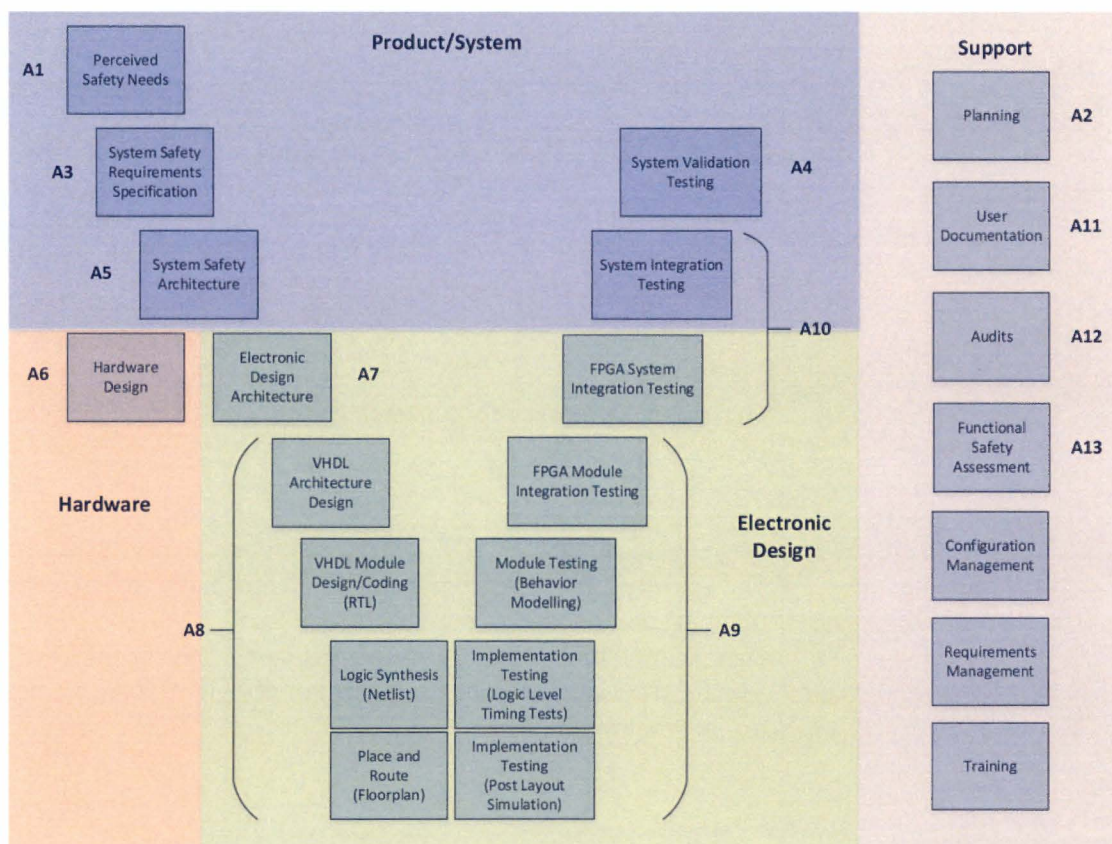
Figure 7-1: IEC Safety Life Cycle Concept





The RadICS Platform safety life cycle expands the design and verify phases to better define the pairing of design activities with the V&V activities for all the levels of design. It should be recognized that the V-model representation does not show well parallelism in the design process and looping required by V&V results. The overall RadICS Platform development lifecycle is shown in Figure 7-2. The figure also provides an overall context for the RadICS Platform development tasks. The product/system portion of the life cycle highlights the tasks that are largely independent of the use of FPGA technology. Similarly, the hardware portion of the life cycle recognizes that the RadICS Platform is built from hardware that has many design aspects that are unrelated to the use of FPGA technology. The Electronic Design portion of the lifecycle captures the development activities that are directly related to the use of FPGA technology. Support activities are activities and support services that must be available for the complete life cycle and are not associated with any individual life cycle phase.

The activities in the RadICS Platform safety life cycle may not necessarily be continuous. For example, A4 starts early with planning of the all V&V activities, as documented in the Overall V&V Plan. After the Safety Requirements Specification (SRS) is written, the Validation Test Plan and Specification are prepared. The Test Specification may have to be modified after the Product Architecture Document (PAD) is issued. The Validation Test Report must wait until almost the end of the project.



**Figure 7-2: RadICS Safety Life Cycle**

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The RadICS Platform development activities tagged with the A label in the figure are described in Table 7-1. The RadICS Platform V&V process is described in Section 7.4. The RadICS Platform configuration management process is described in Section 7.5. The RadICS Platform requirements management process is described in Section 7.6. The use of quality metrics for RadICS projects is described in Section 7.7. The Radics LLC training activities are described in Section 7.8.

The process controls for the RadICS FBL development are described in Chapter 8.

### Table 7-1: Summary of RadICS Life Cycle Development Activities

Label	Title	Description
A1	Perceived Safety Needs	This Activity identifies the safety needs of the target or market industries and clients and describes the RadICS Platform product that will meet those needs and which RPC Radiy is willing to provide. The [[  ]] <sup>a,c,e</sup>
A2	Planning	This Activity plans the work activities, the documentation required, configuration management, training, resourcing, and all the other support activities that must be present from [[  ]] <sup>a,c,e</sup>
A3	System Safety Requirements Specification	This Activity starts the formal engineering work of designing the product. [[  ]] <sup>a,c,e</sup> Validation is based on these requirements.
A4	Validation Planning and Validation	This Activity is executed in two parts: planning and testing. The planning part generates the Validation Test Plan and the Test Specification from the SRS. The testing part produces the Test Specification and the Validation Test Report near the end of the project realization phase. [[



Label	Title	Description
		<p>]]<sup>a,c,e</sup> The Overall V&amp;V Plan serves as the umbrella “Test Plan” for all other Test Plans and numerous Test Specifications. The Overall V&amp;V Plan [[</p> <p>]]<sup>a,c,e</sup></p>
A5	System Safety Architecture Design	<p>This Activity implements the requirements from A3. [[</p> <p>]]<sup>a,c,e</sup></p> <p>High-level integration (and testing) is based on the details of the architecture. [[</p> <p>]]<sup>a,c,e</sup></p> <p>Note: Software is used here in the sense of VHDL.</p>
A6	Hardware Design	<p>In this Activity, the architecture requirements for hardware, from A5, are applied to design and build the chassis and to design and populate PCBs [[</p> <p>]]<sup>a,c,e</sup></p>
A7	Electronic Design Architecture	<p>In Activity A5, the FPGA ED Safety Requirements Specifications and FPGA ED Safety Design are developed. [[</p>





Label	Title	Description
		<p>]]<sup>a,c,e</sup></p> <p>This information is included in the ED Detailed Description (DD) document. Activity A7 is performed following the FPGA Electronic Design Development Procedure.</p>
A8	Detailed Design and Coding	<p>A8 involves VHDL Detailed Design and VHDL module design and coding. [[</p> <p>]]<sup>a,c,e</sup></p> <p>Activity A8 is performed following the FPGA Electronic Design Development Procedure.</p> <p>Note: For VHDL design and test purposes, a “component” is a module or low-level integration of related modules</p>
A9	Electronic Design Functional Tests	<p>A9 is the lowest level of ED testing and includes [[</p> <p>]]<sup>a,c,e</sup></p> <p>Activity A9 is performed following the FPGA Electronic Design Development Procedure.</p>
A10	Integration Testing	<p>During A10, integration tests [[</p> <p>]]<sup>a,c,e</sup></p>
A11	User Documentation	<p>The prime output of A11 is the Product Safety Manual.</p> <p>[[</p> <p>]]<sup>a,c,e</sup></p>
A12	Audits	<p>This “phase” is an on-going support activity that is intended to verify at suitable intervals in the process, as defined in the [[</p> <p>]]<sup>a,c,e</sup></p>





Label	Title	Description
A13	Functional Safety Assessment	This phase is conducted by [[  ]] <sup>a,c,e</sup>

### 7.3.2 High-Level Platform Design

A set of high-level design documents are produced during the RadICS Platform design process.

The Product Concept Document (PCD) is prepared by a multi-disciplinary team. It defines what product looks like, how it is to be used, and how it is positioned in the market.

The SRS is prepared by the safety and design teams. It applies integrity requirements from IEC 61508 and high-level functional requirements. It is developed as a black-box requirements document. The SRS is reviewed by personnel with the appropriate qualifications using safety requirements checklist to ensure the consistency and completeness of the document review. The checklist is used as a verification step for completeness and is maintained as a project record. The SRS is reviewed by a multi-discipline team. The results of the team review are documented in meeting minutes and all action items are tracked to closure.

The PAD defines the modularization of the design. It defines all interfaces and how possible failures are detected and mitigated. It documents how the SRS requirements are met. This RadICS Platform PAD describes architecture of RadICS Platform. As specified in RadICS Platform FSMP, PAD implements high-level requirements presented in RadICS Platform PCD and RadICS Platform SRS. While PCD and SRS are the black-box documents, PAD is white-box and defines the internal structure of the product, providing design solutions for the requirements, and allocating the parts of the solution to the hardware, software, and FPGA/VHDL subsystems of the product.

The architectural design defines all functional blocks and their interfaces, as well as other information required for the detailed design development process. Reliability, traceability, and design verifiability requirements are defined at this stage.

The RadICS Platform PAD identifies the overall system architecture in sufficient detail to illuminate potential failure modes and their impact on the safety of the system, and to document the requirements for counter-measures such as high-effectiveness diagnostics, and preventative design measures. It also identifies known safety integrity measures that can help to mitigate the impact of any dangerous failure modes and their effectiveness. It provides a top-level view of the architecture on a qualitative basis.

The PAD is verified by conducting a System FMEA and the FMEDA once the detailed designs of the RadICS Modules have been developed. An FMEDA is one of the analyses that are performed to achieve functional safety certification of a device per IEC 61508. The FMEDA generates failure rates and the safe failure fraction. The FMEDA is maintained throughout the RadICS Platform lifecycle to reflect changes

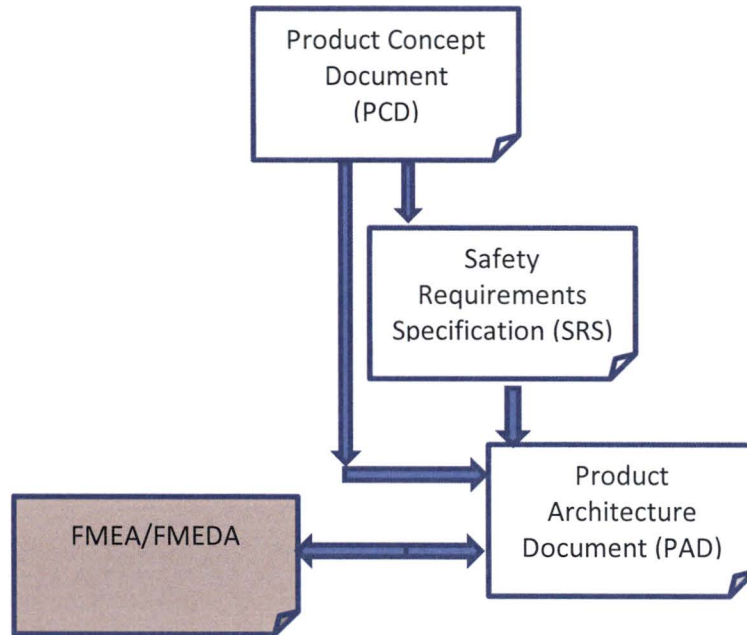


that come from downstream review or design changes. The FMEDA is used in the development of validation test cases, as described in Section 7.4.3.

The output of the architectural design requirements definition process is the textual or graphical description of the design partitioning of the above requirements among the system components. Upon completion of this design activity, a design review is performed, which may result in creating a modified design partitioning or correction of the initial requirements.

The PAD also provides electronic design safety functional and electronic design safety integrity requirements required to implement the safety concept. The identification of separate hardware and software requirements is required by IEC 61508. The separation of requirements allows for separation of the hardware and ED white box testing.

The interrelation between these system documents is shown in Figure 7-3.



**Figure 7-3: High-Level RadICS Platform Requirements Documents**

### 7.3.3 RadICS Module Electronic Design and Implementation

Radics LLC develops I&C systems based on the pre-qualified RadICS Modules. The development cycle complies with requirements of IEC 62566:2011. IEC 62566 uses the term “HDL-Programmed Device (HPD)” for integrated circuit configured via HDLs.

The ED for the FPGAs on the standard RadICS Modules are developed using the “V cycle” model described in the IEC standards, as shown in Figure 7-2.

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The electronic design development and V&V processes are two important processes in the lifecycle of FPGA-based I&C systems. The development process can be further divided into the design phase and the implementation phase. The result of these two phases is FPGA electronic design integration. V&V supports the whole development process and is applied to the output of each development step with appropriate checks, comparisons, and analysis. The high-level documents are reviewed and approved before considering the subsystem or component levels.

The initial and the most critical step of the overall development process is the design process, which includes a preliminary (or architectural) design and detailed design. The preliminary design defines all functional blocks (performing functions such as voting or simple mathematical operations), their interfaces and connections, and other information required in the next phase. At this step, such criteria as reliability, design traceability, and design verifiability are defined. The output of the preliminary design process is the textual or graphical description (diagrams) of design partitioning and other design requirements. Upon completion of this design activity, a design review is performed, which may result in creating a modified design partitioning or correction of the initial requirements.

[[

]]<sup>a,c,e</sup>

These rules may support and assure different safety aspects of the design.

For the verification of detailed design outputs, [[  
]]<sup>a,c,e</sup>

The next major step is implementation, [[  
]]<sup>a,c,e</sup>. The appropriate procedures of V&V relate to each activity of the implementation phase.

[[



]]<sup>a,c,e</sup>

Integration testing is intended to demonstrate that the electronic design implemented in the FPGA chip performs according to its specification and system architecture. This testing complements the integration testing accomplished by the ED Functional Testing (i.e., simulation). For the integration testing, the FPGA chip, which now has the integrated electronic design, is installed on the board for which it was developed. The inputs of the board are connected to a special test bench, which feeds

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them with input signals in accordance with testing stimuli. The outputs of the board are connected to a data acquisition system that collects the response of the board on input stimuli.

Output signals (response) are analyzed in accordance with pass/fail criteria.

The development tasks and output documents for the Platform EDs for the RadICS Modules are summarized in Table 7-2.



Table 7-2: Generic RadICS ED Task Descriptions

HPD Lifecycle Stage	Task Description	Task Results	Standards Requirements
Life cycle and other general requirements for HPD projects	To develop planning document including: <ul style="list-style-type: none"> <li>- FSMP</li> <li>- Configuration Management Plan</li> <li>- Overall V&amp;V Plan</li> <li>- Document Plan</li> </ul> Personnel Management Plan	FSMP and a set of supporting plans	IEC 62566 (2) IEC 61513 (5, 6.3) IEC 60880 (5) IEC 60987 (4)
[[			
]] <sup>a,c,e</sup>			
HPD Requirements Specification	Based on system requirements a set of requirements for HPD Electronic Design is defined, including: <ul style="list-style-type: none"> <li>- functions to be provided by the HPD, modes (such as POWERED-OFF, STARTUP, RUN (SAFE) mode, etc.) and transitions between these modes</li> <li>- I/Os, external interfaces requirements</li> <li>- parameters that can be modified during operation</li> <li>- performance requirements and restrictions</li> <li>- assumptions regarding the HPD environment</li> <li>- fault detection and diagnostics requirements</li> </ul>	Safety Requirements Specification Product Architecture Document	IEC 62566 (6.1 - 6.4) IEC 61513 (6.2.2, 6.2.3, 6.4.2, 6.4.3) IEC 60880 (6) IEC 60987 (5)
HPD Requirements Specification Review	Completeness and compliance of HPD requirements with system requirements are verified after HPD requirements specification phase.	SRS Review Report PAD Review Report	IEC 62566 (6.6) IEC 61513 (6.4.2.3, 6.4.3.3) IEC 60880 (software aspects)







HPD Lifecycle Stage	Task Description	Task Results	Standards Requirements
HPD Verification	To implement systematic V&V process for each of the stage of HPD life cycle	Overall V&V Plan VHDL Static Code Analysis / Code Review Reports VHDL Functional Test Plans and Specifications VHDL Functional Test Reports ED Logic Level Simulation and Timing Test Reports ED Static Timing Analysis Test Reports	IEC 62566 (9) IEC 61513 (6.3.2.2) IEC 60880 (8.1, 8.2.1, 8.2.3) IEC 60987 (7.1-7.7)
HPD System Integration	System integration involves all the activities necessary to ensure that the programmable and non-programmable components work together as a system.	Integration Test Plan	IEC 62566 (10.1 – 10.3) IEC 61513 (6.2.5, 6.4.5) IEC 60880 (9.1, 9.2, 9.4) IEC 60987 (7.8)
HPD Integration Testing	Integration testing is performed to check internal and external system interfaces, as well as system functions.	Fault Insertion Test Plan, Specification and Report Integration Test Plan, Specification, and Report	IEC 62566 (10.4 - 10.6) IEC 61513 (6.4.5.3) IEC 60880 (9.3, 9.5)



HPD Lifecycle Stage	Task Description	Task Results	Standards Requirements
System Validation	Validation is performed to check compliance of complete system with initial system requirements specification. This is mainly a black box type of test.	Validation Test Plan, Specification, and Report	IEC 62566 (11) IEC 61513 (6.2.6, 6.4.6) IEC 60880 (10) IEC 60987 (7.9)



### 7.3.4 RadICS System Integration and Validation

System integration involves all the activities necessary to ensure that the programmable and non-programmable components work together as a system. Integration testing is performed to check internal and external system interfaces, as well as system functions. Validation is performed to check compliance of the complete system with initial system requirements specification. Validation is mainly a black box type of test.

### 7.3.5 Project-Specific Application Process

Project-specific applications are developed using the RadICS Platform components and consists of configuring the RadICS Modules, Chassis, and Cabinets to perform the required system functions. The hardware design is reduced to choosing the required amount and type of cabinets, chassis, and modules in accordance with the system requirements specification.

A set of high-level design documents are produced to develop a project-specific I&C system using the standard RadICS Modules. Before starting FPGA electronic design development, the following documents are prepared and reviewed:

- Technical Requirement Specification describes the overall objectives of the system development as determined by the technical, functional, customer, and commercial goals and requirements.
- Safety Requirements Specification identifies all safety related requirements imposed of the final system, including requirements from appropriate nuclear standards and basic safety standards, such as IEC 61508, and from the specific safety requirements of the given application.
- System Architecture Description provides an overview of the intended system architecture and allocates specific requirements to the various subsystems, such as hardware, application logic, and diagnostic logic.

These can also be combined into a single document based on end user documentation requirements.

At this point, the same process described in Sections 7.3.3 and 7.3.4 is used to complete the project-specific system development. The RPCT can be used to configure EDs for various applications using the AFBL. The project-specific testing focuses on the functional requirements for the system design (i.e., system architecture connections and LM Application ED). The generic RadICS Platform testing of the RadICS Modules and associated Platform EDs is not repeated for a specific project.

The development process for project-specific applications developed using the RadICS Platform technology described in this topical report are intended to be implemented by Radics LLC or authorized partners using the same development process.

The following constraints are applied to the development of Application ED:

- []

]]<sup>a,c,e</sup>

The RadICS Platform Application Guide presented in Appendix A provides requirements for applying the RadICS Platform in NPP I&C systems classified as safety-related and is used in conjunction with other user documentation provided by Radics LLC for application of the RadICS Platform.

#### **7.4 RadICS Platform Verification and Validation**

Given the criticality of nuclear safety system applications using RadICS Platform technology, implementation of a rigorous approach to V&V in compliance with widely recognized standards is necessary to ensure that RadICS Platform systems developed for NPPs are high quality products that meet customer and regulatory requirements. The following V&V methods are used:

- Document review and comments
- Distinct types of analysis, including Static Code Analysis, FMEDA etc.;
- Modeling with the use of simulators

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- Diverse types of testing, including functional testing, fault insertion testing, load and validation testing, with the use of automated facilities

Proven V&V tools are used whenever possible over manual methods to eliminate human error. The above tools are purchased only from well-established vendors with a good track record of configuration management, V&V, problem notification and resolution, and support and training materials.

The RPC Radiy QMS prescribes that all commercial software-based tools used for V&V should be tested and evaluated with the issuance of relevant evaluation reports. In addition to commercial software-based tools, RPC Radiy uses custom software-based and hardware-based tools for V&V activities that have been developed for use with the RadICS Platform. Examples of such tools are VHDL-based Test Benches for code verification.

RPC Radiy V&V capabilities are provided by a department that is technically, administratively, and financially independent from the Design departments. Personnel performing V&V activities have strong theoretical background and practical experience on design and testing of software and FPGA ED. The RPC Radiy practices are in line with those followed by other organizations involved in the design of FPGA-based safety and non-safety I&C solutions for NPPs, as described in EPRI document 1022983 (Reference 7-10). RPC Radiy methods are consistent with U.S. and international standards. Radics LLC V&V personnel also participate in the RadICS Platform V&V activities.

#### 7.4.1 Roles and Responsibilities

The Project Verification Manager coordinates the Verification Team that provides independent internal verification of the design team outputs. The Project Verification Manager is also responsible for preparation of the Overall V&V Plan and its subsidiary plans to ensure compliance of the safety planning measures, including all design and V&V activities, with the applicable national and international nuclear standards.

The Verification Team is independent from design teams because of compliance with the following principles:

- [[

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An independent organization (**exida** LLC) reviewed the Overall V&V Plan, the Radics LLC V&V process, RadICS Platform results, and corresponding documents. They also performed the FMEA and FMEDA for the RadICS Platform.

The V&V process is closely connected with project management, quality assurance, configuration management, and the change control processes. The overall project management process is supervised by the Project Manager. Safety management activities are supervised by Project and Functional Safety Coordinator. The Quality Assurance Team is responsible for quality of all RadICS Platform life cycle processes, including V&V.

All changes of RadICS Platform components arisen by defects discovered during V&V activities are performed under change control procedure in accordance with established procedures. The Change Control Board is responsible for approving changes to the RadICS Platform and managing the implementation of the approved changes, including V&V results and feedback implementation.

The responsibilities for V&V activities are defined in the Overall V&V Plan. The qualifications of the V&V Team and Qualification Testing Team members' competence are defined in the Project Personnel Plan, which includes competencies for knowledge of product domain, functional safety, analysis techniques, and safety concepts. Training records are kept up to date and maintained by the RPC Radiy Human Resource department.

## 7.4.2 Methods and Tools

At each stage of the RadICS Platform safety life cycle, the design outputs (e.g., a specification, description, or code) is verified. This verification may be done by review, inspection, analysis and/or testing (listed in increasing order of preference). These methods and the resulting output are described below:

- Review and comment (R&C) is a recorded check of a document's content and correctness that does not follow an analytic process or use a tool, except that it includes the use of a checklists. The resulting output is a completed checklist that becomes a necessary part of each of the documents or a main part of a Code Review Report.
- Document Inspection (DI) is a detailed formal process of verifying a document, according to a defined procedure. The resulting output is a Review Report (RR).
- Analysis involves a discipline analysis or use of a special tool. Examples of these analyses are FMEDA and Static Code Analysis. The resulting output document is a report (e.g., FMEDA report).
- Testing involves preparation of a test procedure and a test report, as defined by the corresponding plan and specification. The resulting output document is a test report. Distinct types of testing are performed for integrated RadICS Platform and for parts of the RadICS Platform, including ED/FBL Functional Testing (FT), ED Netlist File Logic Level Simulation and Timing Simulation, ED Floor Plan File Static Timing Analyses, Module Fault Insertion Testing (FIT) (as described in Section 7.4.2.1), Software Tool FIT (as described in Section 7.4.2.2), RadICS Platform Integration Testing, RadICS Platform Validation Testing, RadICS Platform EQ Testing.



At the final stages of RadICS Platform design, all outputs that resulted in RadICS Platform hardware (i.e., several types of RadICS Modules with the associated ED and a completed chassis) are validated during Integration Testing and Validation Testing using corresponding testing procedures. The test results are thoroughly analyzed to ensure that all requirements have been met.

V&V activities are performed at every life cycle phase and for every activity. As shown in Section 7.3.1, the RadICS Platform safety life cycle is broken down into activities (A1 through A11). For each activity, the inputs, design outputs, and V&V outputs, as well as, the method of V&V for each document are defined in the Overall V&V Plan. The V&V tasks are shown graphically in Section 7.3.1. The major V&V documents (i.e., analysis reports and test reports) are each identified as specific document types, and as individual documents in the Project Document Plan.

Tools used for V&V are discussed in Section 8.3.

#### **7.4.2.1     *Module Fault Insertion Testing***

RadICS Module FIT demonstrates that the RadICS Modules detect, report, and perform appropriate actions in accordance with three fault types, as required by RadICS Platform FSMP. This testing demonstrates that all Module Hardware Units are covered by the Module diagnostic subsystem. This testing is part of the validation activities performed as part of the RadICS Platform Overall V&V Plan and Safety Validation Test Plan, as required for product certification to IEC 61508 requirements. The RadICS Module FIT cases were developed using the FMEDA for each Module. See Section 9.2.1 for more information on the FMEDA.

#### **7.4.2.2     *Software Tool Fault Insertion Testing***

The FIT was extended to address the use of T3 tools related to the development of Application Logic, to meet the requirements of IEC 61508. The Software Tool FIT demonstrates that the tool performs its required functions modes and the proper handling of any identified failure modes (intentional or through failure) and to validate the mitigation measures used to counter the identified vulnerabilities. The Software Tool FIT cases were developed using the FMEDA analysis for each tool.

Two T3 tools were identified and included in the Software Tool FIT.

- RPCT
- Application Tuning Station

See Section 8.3 for more information on tool classification.

RPCT is the integrated development environment used to design the Application Logic for RadICS Platform-based system. RPCT is used to specify the hardware configuration in RadICS Chassis, assign I/O signals, define tunable parameters, and develop Application Logic using the AFBL. See Section 8.4 for more information on RPCT.

The following critical components of the RPCT were included in the Software FIT:

- UAL Configuration Input Modules
- Build Module

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- UpLoader Module

The RPCT FIT ensures that the LM detects errors in configuration data uploaded into the RadICS Modules using diagnostics subsystem and appropriate actions are performed in accordance with error types. The RPCT FIT validated that the RPCT Output Verification Tool detects and reports errors in configuration data during Application Logic build verification before uploading configuration data into the LM. The RPCT Output Verification Tool tests were completed by a static analysis of the tool to ensure that it detected injected faults.

The Application Tuning Station is used to modify the values of the tunable parameters. FIT was conducted on the Application Tuning Station software to ensure that in the event of a failure that the LM properly handles the tuning modification functions properly and that the mitigation actions are appropriate to detect unintended tuning values.

### 7.4.3 Implementation Activities

The RadICS Platform has several identifiable components, each requiring its own testing, integration testing, followed by overall RadICS Platform integration and validation testing. In addition to integrated overall V&V activities, V&V is performed for three types of RadICS Platform components:

- Hardware modules
- Module FPGA Electronic Designs (including PFBL and AFBL)
- RPCT (as a part of custom tools)

The V&V tasks discussed below correlate to the V&V tasks shown in Figure 7-4.

Integrated RadICS Platform V&V activities include:

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Hardware Module verification includes:  
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[]<sup>a,c,e</sup>

EDs (including FBL) verification includes:  
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[]<sup>a,c,e</sup>

RPCT and Application Logic/AFBL includes:  
[]



]]<sup>a,c,e</sup>

The RadICS Platform development lifecycle activities (including V&V) is shown in Figure 7-4.



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**Figure 7-4: RadICS Platform Development Activities (including V&V)**

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#### **7.4.4 V&V Administrative Requirements**

V&V processes are performed under control of Project FSMP and Overall V&V Plan requirements.

##### **7.4.4.1 Anomaly Resolution and Reporting**

All anomalies found are identified, reported, and analyzed by the responsible V&V Team in appropriate V&V reports.

A decision on resolution of anomalies is ultimately a responsibility of the Change Control Board in the cases when impact analysis, which is performed by the responsible V&V Team member, identifies that anomaly resolution could have an impact on the previous stage/stages of the design life cycle. Anomaly resolutions and decisions for changes for a product are completed by the responsible Development Team.

The responsible V&V Team members repeat the applicable part of V&V activity(s) to prove the anomaly resolution was effective. The appropriate records about anomaly findings, analysis, and resolution are included in the appropriate V&V reports.

##### **7.4.4.2 Task Iteration Policy**

The Validation Test Report for activity V17, Qualification Test Report for activity V18, as well as FMEDA Reports for activity V5, is approved by the Project Manager. All other V&V documents are approved by Project and Functional Safety Coordinator. The Project Manager and Project and Functional Safety Coordinator are decision makers for formal completion of appropriate V&V activities and for transition to the next product development stage. Such transition is allowed only after resolution of all identified anomalies.

##### **7.4.4.3 Deviation policy**

Any deviation from the Overall V&V Plan is documented as the next revision of the Overall V&V Plan. The information required for deviations includes task identification, rationale, and impact analysis. Project Manager is responsible for approving deviations from the Overall V&V Plan.

#### **7.4.5 V&V Documentation Requirements**

The Project Document Plan specifies the requirements for documents to be produced under the Project FSMP and the Overall V&V Plan. The standardized document requirements are intended to facilitate traceability, modification, and translation of documentation.

##### **7.4.5.1 V&V Reporting**

The following types of reports are produced as the result of V&V activities:

- Review Reports for activities V1-V4, V5 (Hardware design review), V6, V7, and V10
- FMEDA Reports for activity V5

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- Test Reports for activities V9, V12-V18, and V21
- Static Code Analysis / Code Review Reports for activities V8, V11, and V22

Detailed requirements for the reports for each of the V&V activities are specified in the Overall V&V Plan. All V&V activities findings are documented in the corresponding reports.

All V&V outputs are Configuration Items and all Configuration Management and Change Control activities are applied for V&V outputs in accordance with the Project Configuration Management Plan, as described in Section 7.5.

#### **7.4.5.2 V&V Test Documentation**

V&V activities V9, V12-V18, and V21 are based on testing methods including:  
[[

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The Overall V&V Plan specifies the content of the specific Test Plan for which Test Specification/Test Procedure and Test Report are required. [[

]]<sup>a,c,e</sup> The specific plans that the Overall V&V Plan covers

are:

- FIT Plan and Specifications:
  - [[

]]<sup>a,c,e</sup>

- Integration Test Plan:
  - The primary aim of the Integration Test Plan is to identify and plan integration tests or other verification methods (if testing is inappropriate) for the requirements from PAD to prove that RadICS Platform meets these requirements:
    - [[

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]]<sup>a,c,e</sup>

- Validation Test Plan:
  - The primary aim of the Validation Test Plan is to identify and plan validation tests or other verification methods (if testing is inappropriate) for the requirements from SRS and Overall V&V Plan to prove that RadICS Platform meets these requirements:
    - [[

]]<sup>a,c,e</sup>

- Qualification Test Plans (Qualification Testing Team responsibility):
  - Testing of the entire product:
    - [[

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- Functional Test Plan and Specification (that combines both component (i.e., unit) testing and integrated ED testing):
  - [[

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#### 7.4.5.2.1 Test Plans

Test Plans are prepared based on the Overall V&V Plan and the part of the RadICS Platform architecture they cover. They address the same subjects as the Overall V&V Plan, but they focus on their specific scope of the RadICS Platform product. Test Plans can serve as the first revision of the corresponding Test Specification and Test Procedure. Test Plans will document:

- What RadICS Platform equipment or components and what functions are to be tested

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- The method of verification or validation (test (wherever possible) or analysis) for each requirement in the scope of the plan
- Detailed acceptance (pass/fail) criteria for each type of tests/analysis or for each of the verified/validated initial requirements
- The testing equipment needed and degree of automation of the tests
- Other resources needed for the tests (e.g., who should be present)
- The general approach to performing the tests

#### 7.4.5.2.2 Test Specifications

Test Specifications are prepared from each Test Plan. A Test Specification is usually the first draft of a Test Procedure and includes test case descriptions. The developed test procedure may remain part of the Test Specification document, as specified in the Test Specification. It is produced before the procedure to provide a high-level perspective for the tests. The Test Specification usually provides the basis for tracing the testing of requirements for V&V. It shall:

- Define the test objectives:
  - Information to Record Before and After the Tests
  - Identification of Test Cases
  - Specifically identify what equipment/components and what functions are to be tested
- Define how the components and functions will be tested, expanding this to the level where the tests cover the requirements completely and are in sufficient step by step detail that they are repeatable or automatable
- Define acceptance criteria for each component, requirement, or function test
- State any assumptions
- Define which test environment is to be used for what tests
- Ensure coverage of all operating modes and a full range of operating conditions in each mode for IT/VT only

If the Test Specification is in sufficient detail that it ensures repeatability, then it essentially includes the Procedure and a separate procedure document is not needed.

#### 7.4.5.2.3 Test Procedures

A Test Procedure document can expand the Test Specification down to repeatable detailed procedural steps, including the detailed pass/fail acceptance criteria where needed to ensure that tests are repeatable, and where it is not practical to include that level of detail in the Test Specification. A separate Test Procedure document is not required if the Test Specification is sufficiently detailed.

Test Procedures are usually formatted to facilitate recording of step-by-step test results. They include:

- Expansion to detailed, repeatable steps of every test specified in the Test Specification
- Provision for recording the test results step by step and review check-off at key milestones

A separate Test Procedure document is used for complicated tests. Test Procedures are generally used only for EQ testing.

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#### 7.4.5.2.4 Test Reports

The Test Report consists of a summary portion and a detailed portion. The summary portion summarizes:

- Precisely what was tested (hardware/firmware/software versions, etc.)
- The versions of the design documentation that correspond to the RadICS Platform Hardware, ED, and software under test
- What equipment was used for the test (the test environment and configuration, calibration sheets of test equipment)
- Who performed the test (signatures of testers)
- A summary and analysis of all test anomalies
- A summary of all changes to the Configuration Items under test
- A summary of any re-testing performed and the impact analysis to support the degree of regression testing (if any were required – else statement that none were required)
- A summary of the results and open items (if any)

The detailed portion consists of the marked up detailed test procedure.

#### 7.4.5.2.5 Test Coverage and Pass/Fail Criteria

Test Plans are traceable to design documents and traceability to Test Specifications and Test Reports. Each Test Specification includes the basis for the selection and detailing of Test Cases to ensure full test coverage. Typical test case approaches are:

- Functional and black box testing to demonstrate requirements coverage
- White box testing to ensure full code structure coverage, using modified condition/decision coverage
- Interface testing using test cases deduced from boundary value analysis or equivalence classes
- Performance/stress testing (such as combinations of variables at extreme values, tests with a fully-loaded system)
- Error guessing
- Full coverage of all functions defined in the corresponding user manuals

Appropriate test cases developed from these principles are applied during:

- Unit testing of VHDL on test-benches
- Integration testing
- Validation testing

The planning of test coverage is dynamic and continues as the design proceeds. A chart of tests is generated and the assignment of tests to various test specification documents is maintained (i.e., allocation of various kinds of tests to Fault Insertion Tests, Integration Tests and Validation Tests) to ensure complete test coverage. It is not possible to test for all hardware or functional configurations in certain cases (e.g., all permutations of RadICS Modules in rack locations). In these cases, a basic set of configurations are tested that collectively provide test coverage of the full set of configurations.

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Each test step of the test specifications/procedure is written so that they form step-by-steps instructions and provide the tolerance criterion for pass or failure of the test step. The tolerance criterion may be stated for each step, sequence of steps or larger part of a test specification/procedure, and there may be difference tolerances for various kinds of readings. Tolerance criteria are established in the Overall V&V Plan, but if different criteria are required, then the specific Plan document for the tests in question (e.g., the Integration Test Plan for integration tests) specifies them. In general, qualitative criteria are to be avoided if possible, but are unavoidable for the following examples:

- Display color: colors that clearly distinguishable are to be used, and the acceptance criterion is that the specified color is recognized by a tester whose color vision is accepted by the V&V Manager as accurate.
- Timing: time of response is normally treated as a quantitative measure (e.g., when testing how long the RadICS Platform component takes to change an output state in response to a stimulus).

For the Static Code Analysis Test, the VHDL-code Static Code Analysis/Code Review is successfully completed if all identified violations and/or defects have been resolved or adequate reasons for all unresolved violations have been documented with corresponding justifications. The decision on the admissibility of such justifications is taken jointly and agreed to by the Project Verification Manager and Electronic Design Development Team Leader.

The Static Timing Analysis is successfully completed if the ED Netlist files are free of timing violations against the predefined timing constraints defined by the ED Development Team in the Project Design Constraints Document. Logic Level Simulation and Timing Simulation testing is successfully completed if the test results consider the maximum and minimum possible delays of the signal propagation in the selected FPGA chip model and they confirm the positive results obtained during the ED Functional Testing.

To simplify the Logic Level Simulation and Timing Simulation test efforts, the same ED Test Benches used in Functional Testing are utilized.

## **7.5 RadICS Configuration Management Process**

The RadICS Platform configuration management process applies throughout the lifecycle of the RadICS Platform and project-specific applications. According to IEC 61513, a configuration management process must be established to document and control the functional and physical attributes of all components, to record and report all changes and to verify their compliance with requirements. Configuration management of the RadICS Platform and its applications is performed according to requirements as outlined in IEC 60880:2006 and IEC 62566.

According to Radics LLC practices and requirements under IEC 61508-2 and IEC 61508-3 (6.2.10, 7.16), all project activities shall be subject to a configuration management plan, which defines the tools, procedures to be used, activities to be performed, their sequence and timing within the product lifecycle and responsibilities for their execution.

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### 7.5.1 Roles and Responsibilities

Configuration management process utilizes the following participants:

- Configuration Management Board (CMB)
- Change Control Board (CCB)

The CMB and CCB are formed at the planning stage for a RadICS Platform-based project (either Platform or project-specific application). CMB and CCB memberships are determined by the Radics LLC Personnel Plan for the project.

The CMB implements the following activities:

- [[

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The CCB implements the following activities in compliance with established procedures:

- [[

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The primary structure of each change implementation board or development team involved in the configuration management process, as well as the personnel assignments to such boards (or teams), is given in Radics LLC Personnel Plan for the project.

### 7.5.2 Process Controls

The Configuration Management Plan implementing procedure identifies the generic Configuration Items for a RadICS Platform-based project. It identifies the Configuration Items generated by RPC Radiy (e.g., hardware, documents, electronic designs, and software elements), as well as, the externally supplied Configuration Items such as development and V&V tools.

The list of the controlled RadICS Platform Configuration Items is a multilevel hierarchical structure. The top level specifies the following Configuration Items:

- Hardware
- PFBL
- AFBL

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- FPGA ED
- Tools
- Documents
- Work Instructions and Guides

The hierarchy of the controlled RadICS Platform Configuration Items is given in Figure 7-5.

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**Figure 7-5: Hierarchy of the Controlled RadICS Configuration Items**

**7.5.2.1 Configuration Items**

Naming Configuration Items includes system of:

- Identifiers for RadICS Platform items and item versions, providing unique identifier for each of the items
- Marking of the items and their versions

Identifiers for all specific RadICS Platform Configuration Items are developed based on the Radics LLC Document Plan for the project.

The acquisition of Configuration Items is performed after the identification and naming of Configuration Items is completed. The acquisition process is implemented in this order to effectively control the RadICS Platform Configuration Items. After each Configuration Item is created and named, it is transferred under the control of the configuration management tool to implement version control.

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Only a single version of tools for a RadICS Platform-based project is installed on the development computers used for the specific Radics LLC project. The version and status of each Configuration Item is checked using the configuration management tool, before a development activity is executed.

Configuration documents and work instructions (in the form of electronic copies) are stored in two separate locations under control of the configuration management tool. The stored copies can be on the same or different media.

Each optical disc is assigned a unique identifier along with a date and time stamp for the disc creation, as specified in the Radics LLC project Document Plan for the project. Data storage identifiers are recorded in the configuration management tool.

### **7.5.2.2 Configuration Baselines**

A Baseline is a RadICS Platform configuration version, related to a specific life cycle stage, which is verified and approved. The Baseline is the basis for implementation of further life cycle stages.

Once a Baseline for a set of Configuration Items is established, implementation of changes into those Configuration Items is controlled by a formal change control process. The change implementation process for the items of any of established baseline is regulated by the change control procedures for RadICS Platform components and RadICS Platform-based applications.

Baselines in RadICS Platform life cycle include specific RadICS Platform Configuration Items relevant to the appropriate RadICS Platform life cycle process.

The RadICS Platform life cycle has the following baselines:

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The complete actual list of Configuration Items for each of the baselines is presented in the Document Plan for the specific project.

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In addition to the Configuration Items specified within each of the baselines, there are the following baseline-independent Configuration Items, which are under control of the configuration management tool:

- Documents
- Tools
- Work Instructions and Guides

### 7.5.3 Implementation Activities

The main configuration management implementation activities are: change control, configuration status accounting, and configuration auditing. Each of these implementation activities is described below.

#### 7.5.3.1 *Change Control*

For each of the identified Configuration Items, change control is performed in accordance with established procedures for RadICS Platform components and RadICS Platform-based applications.

The change control activities consist of implementation of the approved changes, including preparation of change requests, performing an impact analysis, and obtaining approval/rejection. Approved changes are implemented with appropriate documentation, verification, validation, as well as required notifications. Reasons for the necessity to implement changes are regulated by the change control procedure for RadICS Platform components and RadICS Platform-based applications.

Configuration changes are managed to ensure that all needed changes are made and unnecessary (and possibly damaging) changes are not made. Needed changes may arise from field feedback from customers, from internal testing, or from approved product upgrades. An impact analysis is performed to support the approval decision and to help determine the extent of retesting that will be needed. Finally, every time a RadICS Module is modified, it is entered into the configuration management system. These aspects of managing change are illustrated in Figure 7-6.





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]]<sup>a,c,e</sup>**Figure 7-6: Change Control Work Flow**

The Product Safety Manual provides end users and system integrators with instructions on how to report problems with the RadICS Platform.

When a report concerning a possible problem with the RadICS Platform or a delivered system is received from an end user or system integrator that is or could possibly be associated with a possible hazardous event, a Change Request is always initiated. This Change Request is processed to completion with a high

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priority. The Functional Safety Coordinator is responsible for ensuring that the change request is promptly processed to completion.

#### **7.5.3.2 Configuration Status Accounting**

Configuration status accounting is realized after the establishment of the Requirements Baseline and proceeds during the entire RadICS Platform life cycle. Configuration Item status accounting consists of monitoring, documenting, and notification regarding any changes in RadICS Platform configuration. Configuration Items status accounting is performed using configuration management tool(s).

The following information is used for configuration status accounting:

- List of items, which are traced and included into RadICS Platform configuration versions and/or baselines and into change control, represented in configuration audit reports
- Reports on RadICS Platform configuration status accounting (including versions of items, status of change requests, and data concerning approved changes) are generated after each lifecycle stage using a configuration management tool

The configuration audit reports are available to the project personnel. The configuration management tool can generate the following reports at any time:

- RadICS Configuration Items allocation report: reflects allocation of all items in the RadICS Platform (i.e., list of items, their description, and location)
- Report on established RadICS Platform baseline: a list of all Configuration Items of the given RadICS Platform-based project baseline with identification of appropriate attributes for each of the items

The Release Baseline configuration is verified with the actual configuration, approved in the corresponding documents prior to release to the customer. V&V results are presented in the acceptance testing reports.

#### **7.5.3.3 Configuration Auditing**

After release of each of the established baselines, a baseline configuration audit is performed. Interrelationship of these audits with the RadICS Platform life cycle is shown in Figure 7-7. Each Configuration Audit is directed towards check of correctness of the RadICS Platform Configuration Items functional and physical features implementation for the specific project.



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]]<sup>a,c,e</sup>**Figure 7-7: RadICS Baseline Configuration Audits**

A Configuration audit is performed to confirm compliance of RadICS Platform configuration hardware, electronic designs, and software items implementation with their technical documents. Compliance identification process consists in review of design documents, electronic design VHDL files, as well as user documents, and is directed towards check of the fact that:

- Each established RadICS Platform baseline includes correct versions of items
- All documents are issued, approved and correspond to RadICS Platform configuration

The configuration audit results are documented in the configuration audit reports for each stage. A Configuration Audit shall be performed after establishing of each baseline within the RadICS platform-based project. There are [[ ]]<sup>a,c,e</sup> configuration audits corresponding to appropriate baselines in RadICS Platform-based project to be performed:

- [[



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The output from each of the Configuration Audits is documented as each audit is performed. The audit reports include the appropriate checklists to ensure consistent reviews. After performance of the configuration audit, there may be findings. Such findings are resolved and re-audited following the same process to verify that the findings were completely resolved.

## 7.6 Requirements for the RadICS Platform and Applications

Platform Functional requirements are divided into the following groups:

- Safety requirements
- Performance requirements
- Qualification requirements

The high-level safety, performance, and qualification requirements are illustrated in Figure 7-8.

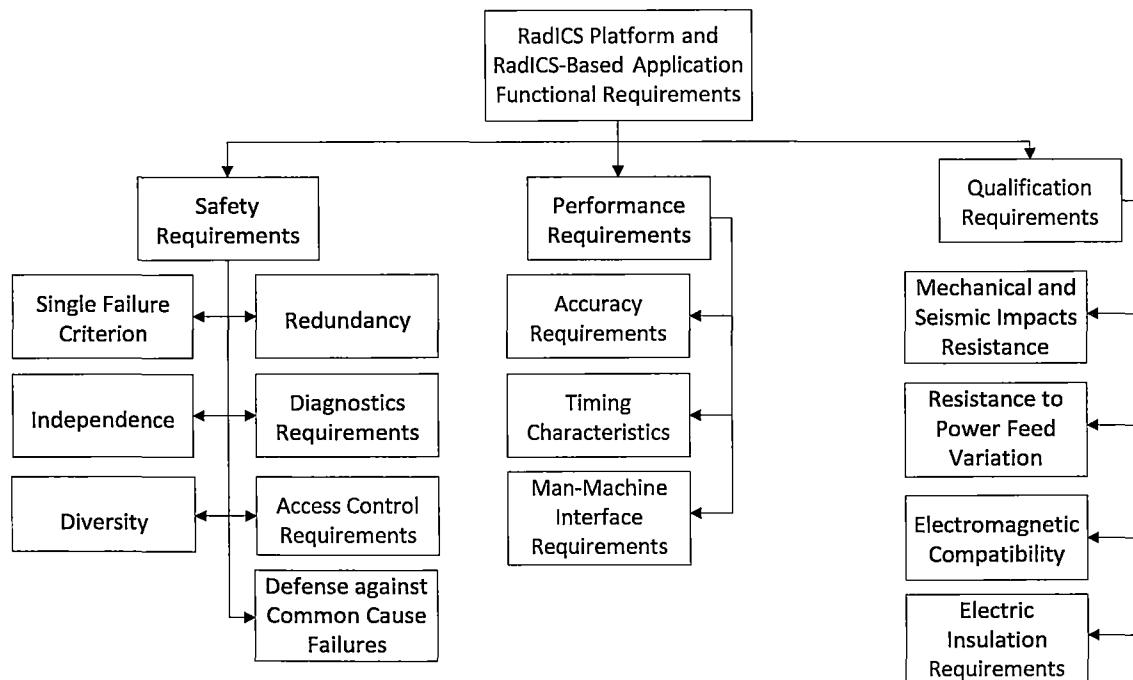


Figure 7-8: RadICS Platform and Applications Requirements



### 7.6.1 Allocation of Requirements

The allocation of RadICS Platform requirements has up to three dimensions:

- Modules to which they apply (MA = module allocation)
- Means of meeting the requirement (IA = implementation allocation)
- Means of V&V (by testing) (TA = test allocation)

Module Allocation is used for requirements that apply to or are implemented by one or more Module(s). The module allocations used for the RadICS Platform are:

Symbol	Meaning	Description
ALL	All Modules	The requirement applies to all Modules.
I/O	All I/O Modules	The requirement applies to all I/O Modules (AIM, RIM, TIM, WAIM, DIM, DOM, AOM, and OCM).
AIM, etc.	Named Modules only	The requirement applies to all named Modules (LM, AIM, RIM, TIM, WAIM, DIM, DOM, AOM, and OCM), and no others.

Implementation Allocation is used for requirements that are implemented via conventional electronic hardware, via ED (i.e., VHDL), or a combination of both. The implementation allocations used for RadICS Platform are:

Symbol	Meaning	Description
ED	Electronic Design	The design child documents are the architecture design of the functionality of the VHDL design, followed by detailed design and coding.
HW	Hardware	Conventional components (e.g., timers, FETs, varistors, etc.) are required to meet some requirements. Because the design tools produce only graphic objects, the next level of design document verifiable from examination of anything textual is the hardware design review report.
PSM	Product Safety Manual	The requirement is for statements in the User Safety Manual, not for something to be implemented in the product.



Testing Allocation starts with understanding the environment needed to execute and test a requirement. For this reason, the SRS and PAD provide preliminary allocations of what level of test will be used for verifying requirement implementation. The allocation is designed to both identify every requirement to be tested and to identify tests to completely cover the requirement. These allocations need not be final, since the requirements tracing tool is updated throughout the development process and will record which test plan or specification covers the requirement. The test allocations used for RadICS Platform are:

Symbol	Meaning	Description
FIT	Fault Insertion Test	FIT tests are 'negative' tests, designed to test the integrity requirements. If separately determined based on the FMEDA that credits the claimed fault detection functions described in the PAD, these do not have to be repeated
FT	Functional Test	These are the 'positive' tests of the intended functionality of the RadICS Platform, and may be conducted at any reasonable test level (e.g., module, integration, validation)
NT	No test needed	Justifiable when a requirement is just a collector and simply points to (requires) other requirements that are tested.
VT	Validation Test	Test that should be conducted as part of Validation testing.

### 7.6.2 Documentation of Design Requirements

The RadICS Platform SRS specifies the functionality and properties of the RadICS Platform as a black box (i.e., no content describing the internal modularization of the RadICS Platform).

The RadICS Platform PAD describes the hardware components and the principles of operation, including required diagnostics.

The PAD also includes separate requirements for hardware and electronic design, as required by IEC 61508. The PAD allocates the functional specification from the SRS to the specific Modules, operational modes of modules, and the use and operation of hardware units (from which modules are built). It describes their operation and specifies the design for inter-module communications.

### 7.6.3 Maintainability and User Friendliness Requirements

Design features that enhance maintainability and user friendliness of the RadICS Platform are described in Table 7-3. The checklist items below are taken from Part 7 of IEC 61508.

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### Table 7-3: Maintainability and User Friendliness Requirements

[illegible]



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Clause	Checklist Items from IEC 61508/7-B.4	How this Recommendation is Met
B.4.4	Considerations for limiting operational possibilities	
	limiting the operation within special operating modes, for example by key switches	The use of keyswitches is explained in Section 6.9
	limiting the number of operating elements	[[  ]] <sup>a,c,e</sup>
	limiting the number of generally possible operating modes	[[       ]] <sup>a,c,e</sup>
B.4.5	Operation only by skilled operators	
	Training is commensurate with the SIL level and complexity of the maintenance activities	[[     ]] <sup>a,c,e</sup>
	Training includes understanding of the process hazards	[[  ]] <sup>a,c,e</sup>
B.4.6	Protection against operator mistakes	
	Wrong inputs (value, time, etc.) are detected via plausibility checks or monitoring of the EUC	[[    ]] <sup>a,c,e</sup>

#### 7.6.4 Requirements Tracing Tool

The implementation status of the RadICS Platform safety requirements is documented in a Requirements Traceability Matrix. The requirements tracing tool has the following capabilities:

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- Capable of capturing requirements, design and implementation statements (solutions), as well as analysis and test procedures and reports, and identify them by a unique ID
- Capable of linking the requirements, design solutions, analyses, and tests

As a minimum, the tracing information is given by means of a cross-reference list between requirement and allocation to component(s) and related design and verification documents and paragraph. The cross-reference allows for forward and backward tracing. Any additional safety requirements identified during the Architectural Design and Verification (derived requirement) are also entered into the Requirements Traceability Matrix.

All design and test specifications are reviewed to verify that they implement the requirements allotted to them.

The requirements tracing tool may be adapted or modified for a RadICS Platform-based project based on customer requirements.

## **7.7 Development Process Metrics**

Quality metrics are used throughout the RadICS Platform life cycle to assess the effectiveness of the QA program for electronic design. The metric approach discussed below is used to conform to the requirements in IEEE Std 7-4.3.2-2003 clause 5.3.1.1 (Reference 7-11), as endorsed by RG 1.152 (Reference 7-12).

### **7.7.1 Electronic Design Quality Metrics Based on Anomaly Reports**

The FSMP and the Overall V&V Plan define the anomaly reporting and resolution process used during the RadICS Platform development process. All electronic design review and test reports include a discussion of the anomalies found and their resolution. These electronic design and other design anomalies are recorded as open issues in the Radics LLC action tracking system during each phase of development.

### **7.7.2 Electronic Design Quality Metrics Based on V&V Open Issues**

The FSMP and the Overall V&V Plan require the use of an action tracking process for all stages of electronic design development and V&V. The open issues are assessed using the following indicators:

- Total number of V&V open issues in the open issues backlog as a function of calendar time
- Number of project open issues discovered by V&V team compared to the total number of open issues
- Severity statistics associated with anomalies and open issues discovered during V&V activities
- Number of anomalies discovered by V&V team during review and testing



### 7.7.3 Electronic Design Quality Metrics Based on Test Coverage

The V&V plans defines quality metrics based on test coverage calculation. Requirements coverage is a required metric that is defined as the fraction of requirements specified in the top-down design documents that are traceable into test plan and specifications. A comprehensive 100% functional coverage is required. It is recognized that some requirements may not be testable; therefore, alternate analytical verification means are defined. The coverage is recalculated by crediting approved means of alternative verification. Code structure coverage metrics are defined as the fractions of code components that are covered during testing. Radics LLC use the following coverage metrics to approve VHDL 100% code coverage with tests:

- 100% statement coverage
- 100% branch coverage
- 100% modified condition/decision coverage

The V&V reports provide evidence that 100% requirements test coverage as well as 100% code structure test coverage is achieved.

## 7.8 Development Process Training

All persons assigned responsibilities for a RadICS Platform-based project are be informed of their responsibilities, as specified in the Project FSMP. All persons assigned to the project are technically qualified in terms of formal education, specific product training, specific training on quality procedures (including the Project FSMP), and relevant professional experience.

The Project Personnel Plan lists the current incumbents for each role, the competence requirements for the roles, and the compliance of the incumbent for each role. Where each design team (software, electronic design, hardware, mechanical) consists of more than just the development manager (i.e., the team leader), the rest of the team should collectively have the same competency as the team development manager. Each member of the team is required to have the technical education and specific training required to execute the assigned responsibilities. Each team is assessed for its combined competencies and shown to cover all required competencies for the work performed by the team.

The Technical Director performs a training needs analysis based on the matrix of competencies for the various job functions and develops an annual training plan in accordance with the Project Training procedure. Training is conducted in accordance with the training plan by both in-house and external training resources. Training records include the training material, participant lists, feedback forms, and training results. Training records for each employee are maintained by the Human Resources organization. The training instructor is responsible for determining if the training objectives were met for each student.

All personnel playing a significant role on a Radics LLC project will received IEC 61508 training and will indicate that they understand their responsibilities.

If performance weaknesses are disclosed, they are addressed by documenting planned corrective action, such as training.

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## 7.9 Chapter 7 References

- 1 Safety Guide IAEA NS-G-1.3, "Instrumentation and Control systems important to safety in nuclear power plants"
- 2 Safety Standards Series No. NS-R-1, "Safety of Nuclear Power Plants: Design"
- 3 Safety Guide IAEA NS-G-1.1, "Software for Computer Based Systems Important to Safety in Nuclear Power Plants"
- 4 IEC 61508:2010, "Functional Safety of Electrical/Electronic/Programmable Electronic Safety-related Systems"
- 5 IEC 61513:2001, "Nuclear power plants – Instrumentation and control systems important to safety – General requirements for systems"
- 6 IEC 60880:2006, "Nuclear power plants – Instrumentation and control systems important to safety – Software aspects for computer-based systems performing category A functions"
- 7 IEC 60987:2007, "Nuclear power plants – Instrumentation and control important to safety – Hardware design requirements for computer-based systems"
- 8 IEC 62566:2011, "Nuclear power plants – Instruments and control important to safety – Development of HDL-programmed integrated circuits for systems performing category A functions"
- 9 RTCA/DO 254, "Design Assurance Guidance for Airborne Electronic Hardware"
- 10 Electric Power Research Institute, "Recommended Approaches and Design Criteria for Application of Field Programmable Gate Arrays (FPGAs) in Nuclear Power Plant I&C Systems," 1022983, 2011
- 11 IEEE Std 7-4.3.2-2003, "Standard Criteria for Digital Computers in Safety Systems of Nuclear Power Generating Stations"
- 12 Regulatory Guide 1.152, Revision 3, "Criteria for Use of Computers in Safety Systems of Nuclear Power Plants"



## 8 Electronic Design Development

The RPC Radiy Electronic Design Development Team was responsible for the development of the ED for RadICS Modules and the RadICS FBL. ED is a set of FPGA configuration files that are installed (loaded) into the RadICS Modules. RPC Radiy used a defined and controlled process to develop the RadICS Platform ED that complies with the requirements of IEC 61508:2010 (Reference 8-1).

When developing RadICS Platform safety applications, RPC Radiy and Radics LLC use tools and components (i.e., FPGA chips) manufactured by Altera using the FPGA design flow defined in the Altera user manuals. The chipsets and related tools are part of the Altera Functional Safety Data Package, that was certified to IEC SIL 3 (reference TÜV Rheinland Certificate No. 968/EL 693.00/10). Tools are used for development and/or V&V efforts. These tools are described in Section 8.3.

### 8.1 RadICS Electronic Design Process

Development of the RadICS Module ED is a step-by-step process translating the RadICS Platform requirements into ready-to-use electronic modules as bitstream files.

The RadICS Module ED development process is defined in procedures and is accomplished in eight phases:

- Development of Electronic Design Architecture Description (ED AD)
- Development of FBL Detailed Description
- Development of FBL Code
- Development of ED DD
- Development of ED Code
- Synthesis
- Place and Route
- Bitstream generation

A set of documents and files is generated during each ED phase, which is used as input to the subsequent phases of development ED or is part of the outcome of ED development.

Figure 8-1 shows the relationship of the phases of the RadICS Platform ED development life-cycle and the documents produced.



[[

]]<sup>a,c,e</sup>

**Figure 8-1: RadICS ED Development Lifecycle and Documents**

Chapter 8 only describes the ED stages of development for the RadICS Modules and FBL with a summary of the V&V methods for each ED phase. The complete RadICS Platform V&V methods are described in Section 7.4.

The following sections contain a description of each of the ED development stages, including:

- Input data
- Implementation details
- Outputs
- Methods of Verification

The ED phases are implemented independently for each RadICS Module.

Inputs and outputs are the documents (RPC Radiy or vendor) and/or files and artifacts created for the project.

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### 8.1.1 Development of Electronic Design Architecture Description

The inputs for the ED Architecture Description phase are:

- RadICS Platform PAD
- [[ ]]<sup>a,c,e</sup>

At this stage, an ED AD is developed for each RadICS Module and documented in an ED DD.

[[ ]]

[[ ]]<sup>a,c,e</sup>, the ED AD development may begin. The ED AD is developed for each of the RadICS Modules and all on-board components (e.g., ED AD for the PSWD CPLD). Any common components are developed once and used in all Modules across the platform.

The ED AD contains the following information:

- Top-level architecture requirements, including:
  - [[ ]]

[[ ]]<sup>a,c,e</sup>

- ED diagnostic architecture

[[ ]]

[[ ]]<sup>a,c,e</sup> This information is utilized in the

Synthesis and Place and Route stages.

The outputs of the ED Architecture Description phase are:

- ED DD for each RadICS Module and an [[ ]]<sup>a,c,e</sup>

All output documents from this stage are reviewed and verified for completeness and implementation of all input requirements. [[ ]]

[[ ]]<sup>a,c,e</sup>

### 8.1.2 Development of Function Block Library Detailed Description

The FBL development steps described here apply to both the PFBL and the AFBL development and V&V activities. The PFBL and AFBL are two separate entities. Some additional steps are taken and separate AFBL documents are produced both for design and V&V to ensure the AFBL is properly documented and structured for use in safety-related applications. The inputs, outputs, and additional development steps for the AFBL are described in Section 8.2.

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The inputs for the FBL Detailed Description phase are:

- ED DD for each RadICS Module and an [[ ]]<sup>a,c,e</sup>

At this stage, the RadICS FBL Detailed Description document is developed, which contains the detailed requirements for PFBL). During the PFBL development, the following elements are detailed:

- Scope and Purpose
- [[ ]]<sup>a,c,e</sup>
- Platform requirements for each of the Units, including:
  - [[ ]]

]]<sup>a,c,e</sup>

The output of the FBL Detail Description phase is:

- FBL Detailed Description

The outputs of this phase are verified by two methods:

- [[ ]]

]]<sup>a,c,e</sup>

The RadICS FBL is uniquely developed by RPC Radiy for the RadICS Platform. [[ ]]

]]<sup>a,c,e</sup>

8.1.3 Development of Function Block Library Code

The steps described here apply to both the PFBL and AFBL development and V&V activities. The PFBL and AFBL are designed together as one library; however, additional steps are taken and separate documents are produced both for design and V&V to ensure the AFBL is properly documented and structured for use in safety-related applications. The outputs and additional development steps for the AFBL are described in Section 8.2.



The inputs for the FBL Code phase are:

- FBL Detailed Description
- [[ ]]<sup>a,c,e</sup>

At this stage, the FBL VHDL Code document is developed by implementing the functions that are defined in the FBL Detail Description document. [[ ]]

]]<sup>a,c,e</sup>

The outputs of the FBL Code phase are:

- FBL VHDL Code
- FBTB Test Report

The outputs of this phase are verified by [[ ]]<sup>a,c,e</sup>:

- [[ ]]

]]<sup>a,c,e</sup>

### 8.1.4 Development of Electronic Design Detailed Description

The inputs for the Electronic Design Detailed Description phase are:

- ED AD for each RadICS Module
- FBL Detailed Description

At this stage, the ED DD document is developed for each RadICS Module. These documents contain the detailed requirements for all FPGA components on each RadICS Module. The ED DD development includes the following elements:

- Scope and Purpose of the Document
- [[ ]]

]]<sup>a,c,e</sup>

The output of the Electronic Design Detailed Description phase is:

- ED DD for each RadICS Module

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The outputs of this phase are verified by two methods:

- [[

]]<sup>a,c,e</sup>

**8.1.5 Development of Electronic Design Code**

The inputs for the Electronic Design Code phase are:

- FBL VHDL Code
- ED DD for each RadICS Module

At this stage, the functions defined for each ED are implemented using the VHDL language. This coding represents the formal representation of the hardware description language (VHDL Design Files). It uses a structural decomposition and top-down design.

[[

]]<sup>a,c,e</sup>

When performing the VHDL language coding, developers are guided by the [[

]]<sup>a,c,e</sup>

The outputs of the Electronic Design Code phase are:

- ED VHDL Code for each RadICS Module
- [[

]]<sup>a,c,e</sup>

The outputs of this phase are verified by two methods:

- [[

]]<sup>a,c,e</sup>



### 8.1.6 Synthesis

The inputs for the Synthesis phase are:

- ED VHDL Code for each RadICS Module
- [[ ]]<sup>a,c,e</sup>

At this stage, the ED VHDL Code is automatically synthesized into logical view cells fitting the corresponding FPGA chip. [[ ]]

]]<sup>a,c,e</sup>

The outputs of the Synthesis phase are:

- Generated synthesis reports consisting of builds for each RadICS Module
- [[ ]]
- RadICS Module ED Synthesis Results Review Reports

]]<sup>a,c,e</sup>

[[ ]]

]]<sup>a,c,e</sup>

### 8.1.7 Place and Route

The inputs for the Place and Route phase are:

- Synthesis Database [[ ]]

]]<sup>a,c,e</sup>

At this stage, a Netlist is automatically created and is presented in the Place and Route format with the specific location of each logical cell, the links between them, and other resources of the FPGA. [[ ]]

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]]<sup>a,c,e</sup>

The outputs of the Place and Route phase are:

- Generated performance Place and Route reports consisting of builds
- [[ ]]<sup>a,c,e</sup>
- ED Place and Route Results Review Reports for each RadICS Module

[[

]]<sup>a,c,e</sup>

**8.1.8 Bitstream Generation**

The inputs for the Bitstream phase are as follows:

- Place and Route Database [[ ]]<sup>a,c,e</sup>

The purpose of this step is to create a programming file for implementation into the RadICS Module, (i.e., used for configuring logical cells on the FPGA chip by using the onboard programmer). [[

]]<sup>a,c,e</sup>

The outputs of the Bitstream phase are:

- Programming files for each RadICS Module and generated reports on the implementation of the bitstream generation consisting of builds
- Modules ED Bitstream Generation Results Review Reports.

[[

]]<sup>a,c,e</sup>



After completion of the ED, the Bitstream files are implemented in the RadICS Modules. Module tests are carried out in phases (i.e., Fault Insertion Testing, Integration Testing, and Validation Testing).

## **8.2 Application Function Block Library Electronic Design Development**

The AFBL is designed to provide a fully validated and qualified function block language that is sufficiently rich in the capabilities of the blocks that RadICS Application ED can be designed entirely using only the AFBL blocks. Several activities, in addition to the steps described in Sections 8.1.2 and 8.1.3, are taken to further document and verify the AFBL.

### **8.2.1 AFBL Design Activities**

The inputs for the RadICS AFBL and associated user documents are the RadICS Platform PAD and RadICS AFBL/Application Logic Detailed Requirements Specification.

The outputs for the RadICS AFBL user documents are:

- RadICS AFBL Function Block Reference Manual
- RadICS Application Logic User Manual

The AFBL Function Block Reference Manual defines the Application Function Blocks that are available in the AFBL for the design engineer to create Application Logic for safety-related RadICS Platform-based projects.

The Application Logic User Manual is provided to inform the application designer about the AFBL structure and constraints; Function Block list; and a Function Block description (e.g., purpose, parameters, functional requirements, and usage examples). This document also describes the process of Application ED creation (using the Quartus-based approach).

All RadICS AFBL blocks are designed for safety applications and the following rules are applied:

- All blocks test Application Logic inputs and tuning parameters, as well as intermediate results to ensure that no error condition can result in computational exceptions (e.g., due to divide-by-zero, underflow, overflow or any other error condition). The blocks also ensure that there is no violation of the fundamental assumptions behind the calculation algorithm used within the block.
- Where overflows are possible, internal calculations are performed to higher precision than SINT16 (signed 16-bit integer format) and then truncated to SINT16.
- All blocks that could be subject to either of the foregoing conditions provide appropriate diagnostic output signals that are used in the Application ED for error management.

In addition to checking that input data do not cause problems, the RadICS AFBL blocks protect their operational integrity by ensuring that the tuning parameters, singly and in concert, are consistent with the requirements of the computational algorithm used inside the block. Integrity defenses include:

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- All AFBL blocks perform validation of the tuning values and their inputs to ensure that the values are consistent with the concept of the block. Each tunable block outputs a tunable parameter status signal set to TRUE if tuning parameter validation succeeds, and FALSE if it fails.
- If a tuning parameter of a block, alone or in concert with any other tuning parameters, fails the validation tests, the SOR will be set by the Application Logic. This action will drive all safety-function outputs on RadICS Modules to the safe state. Some RadICS Module outputs may be designed during configuration to be used for non-safety-critical functions (e.g., alarms) and will remain functional. The SOR will not be reset until the tuning validation succeeds and an operator then activates the SOR reset button.

The AFBL Function Block Reference Manual and the RadICS Platform Application Logic User Manual are used together to produce Application ED for a RadICS Platform-based project. This Reference Manual defines the AFBL blocks. The User Manual is used to familiarize the user with the AFBL structure and constraints, the functional blocks list, and their description (i.e., purpose, parameters, functional requirements, and usage examples). This document also describes the process of Application ED creation using Quartus-based approach.

### 8.2.2 AFBL Methods of Verification and Validation

The V&V activities for the AFBL are conducted in an equivalent manner as for the PFBL described in Section 8.1.2 and 8.1.3; however, a separate set of phase activities and documents are produced. The V&V engineers perform reviews of the AFBL design documents and produce review reports in addition to performing functional testing.

The outputs of AFBL development are verified by three methods:

- Verification of AFBL design documents and issuance of the Application Logic User Manual Review Report to verify the completeness of each document and ensure that they are aligned with the phase inputs
- Static analysis review of the VHDL code and issuance of the AFBL Static Code Analysis / Code Review Report
- Functional testing of the VHDL code based on the AFBL Functional Test Plan and Specification and issuance of the AFBL Functional Test Report

The AFBL development is not considered complete if the verification and validation effort reveals deficiencies. If deficiencies are detected, the AFBL is refined and verified until all deficiencies are resolved.

### 8.3 FBL and Module Electronic Design and V&V Tools

The RadICS Platform development process uses several commercial tools to produce the FBL and the ED for the RadICS Modules. The tool types used for ED development are:

- VHDL Tool Suite for VHDL code development
- Static analysis tool
- VHDL simulation tool
- Test coverage analysis tool

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- Test automation tool
- Compiling tool
- Integrated development environment

Proven tools are preferred over manual methods. Software-based tools are purchased only from long-established vendors with a good track record of configuration management, V&V, problem notification and resolution, product support, and training material. A Project Tool Selection and Evaluation Report are prepared for all commercially available tools to be used that specifies each tool by function, name, manufacturer, and version number. RPC Radiy has a policy in place for tool upgrades, in which the revised tool is used to regenerate an existing application, which is then tested for errors.

Each tool used for RadICS Platform ED and FBL development is classified according to its application. The tools are classified as defined in IEC 61508:2010. Software-based tools are divided into the following classes:

- T1 – generates no outputs that can directly or indirectly contribute to the executable code (including data) of the safety related system (e.g., a text editor or a requirements or design support tool with no automatic code generation capabilities; configuration control tools). These tools are not discussed in this Topical Report.
- T2 – supports the test or verification of the design or executable code, where errors in the tool can fail to reveal defects but cannot directly create errors in the executable software (e.g., a test harness generator; a test coverage measurement tool; a static analysis tool).
- T3 – generates outputs that can directly or indirectly contribute to the executable code of the safety related system (e.g., a tool to change set-points during system operation; an optimizing compiler where the relationship between the source code program and the generated object code is not obvious; a compiler that incorporates an executable run-time package into the executable code).

Note: executable code is used here in the sense of electronic designs.

The tools are evaluated based on a standard set of criteria, as shown in Table 8-1.

**Table 8-1: RadICS Tool Evaluation Criteria**

Evaluation Criterion	Tool Class		
	T1	T2	T3
[[			



Evaluation Criterion	Tool Class		
	T1	T2	T3
			]] <sup>a,c,e</sup>

All tools used for a RadICS Platform-based project are controlled within the scope of Configuration Management repository, as required by the Project Configuration Management Plan

Table 8-2 outlines the commercial tool profile used for ED development in RadICS Platform-based projects.



Table 8-2: RadICS Commercial Development Tools

Tool Name	Tool Function	Tool Supplier	Tool Classification	Configuration Items Generated
Quartus II	[[ ]] <sup>a,c,e</sup>	Altera	[[	]] <sup>a,c,e</sup>
HDL Designer	[[ ]] <sup>a,c,e</sup>	Mentor Graphics	[[	]] <sup>a,c,e</sup>
Understand	[[ ]] <sup>a,c,e</sup>	Scientific Toolworks, Inc.	[[	]] <sup>a,c,e</sup>
ModelSim	[[ ]] <sup>a,c,e</sup>	Mentor Graphics	[[	]] <sup>a,c,e</sup>
LabView	[[ ]] <sup>a,c,e</sup>	National Instruments Corp.	[[	]] <sup>a,c,e</sup>
TestComplete	[[ ]] <sup>a,c,e</sup>	SmartBear	[[	]] <sup>a,c,e</sup>
TopJTAG Probe	[[ ]] <sup>a,c,e</sup>	TopJTAG	[[	]] <sup>a,c,e</sup>
Visual Studio	[[ ]] <sup>a,c,e</sup>	Microsoft	[[	]] <sup>a,c,e</sup>
PostgreSQL	[[ ]] <sup>a,c,e</sup>	PostgreSQL Global Development Group	[[	]] <sup>a,c,e</sup>



Tool Name	Tool Function	Tool Supplier	Tool Classification	Configuration Items Generated
Qt Creator	[  ]	Qt Company	[	]] <sup>a,c,e</sup>
GNU Compiler Collection	[ ] ]] <sup>a,c,e</sup>	The GNU Project	[	]] <sup>a,c,e</sup>

There are custom software-based and hardware-based tools for some V&V activities like Test Benches that are used as tools for RadICS Platform V&V (including ED and FBL verification and integration and validation testing). The details for the use of such Test Benches in V&V activities are defined in the RadICS FBL Functional Testing Plan and Specification, the RadICS Module FPGA ED Functional Testing Plans and Specifications, the RadICS Platform Integration Testing Plan, and the RadICS Platform Validation Testing Plan.

The work flow for RadICS Platform ED development is shown in Figure 8-2.

[[

11a,c,e

**Figure 8-2: Work Flow of Tools for FBL and ED Development**

### 8.3.1 Quartus II

Quartus II is an integrated system-level design tool that is used to support RadICS Module ED and FBL VHDL design. It integrates design, synthesis, place and route, and verification into a single development environment. Quartus II has features that facilitate the design process:

- incremental compilation to reduce the design cycle time
- system-on-a-programmable-chip Builder for system-level design

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- power analysis tools to meet stringent power requirements
- memory compiler function to easily use embedded memory

Altera has a closed loop quality and reliability system that conforms to the requirements of ISO 9001:2008 (Reference 8-2), MIL-I-45208 (Reference 8-3), and various Joint Electron Device Engineering Council standards. [[

]]<sup>a,c,e</sup>

### 8.3.2 HDL Designer

HDL Designer is used for [[

]]<sup>a,c,e</sup>. HDL Designer is an advanced design rule checking tool designed to detect problems early in the development cycle without behavioral simulation, including poor coding styles, improper clock and reset management, simulation and synthesis problems, poor testability, and electronic design VHDL issues. HDL Designer includes the DesignChecker feature, which enables Radics LLC development and V&V teams to view and manage the results of the linting session. Violation reports can be exported into a file for analysis.

[[

]]<sup>a,c,e</sup>

HDL Designer is widely used in many industries with a wide global presence.

### 8.3.3 Understand

Understand is used for [[

]]<sup>a,c,e</sup>. The Understand tool includes several useful features:

- Information Browser, which can display various kinds of information about entities (e.g., source files, classes, members, functions, types, methods, packages, interfaces, etc.). Information that is hierarchical in nature (such as a call relationship) can be expanded multiple levels.
- Architecture Browser, which shows a list of all the defined architectures in the database and provides a way to navigate individual architectures.
- Graphical Views, which presents information from internal database containing information about the entities and the relationships between entities in a convenient form. Two kinds of graphical views are available: hierarchy (shows relations between entities, from the starting entity through its children and successors) and structure (shows the structure of any entity that added to the structure of the code).

Understand is used in many industries in several countries. [[

]]<sup>a,c,e</sup>

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### 8.3.4 ModelSim

The ModelSim tool is used at the [[

]]<sup>a,c,e</sup>

ModelSim supports Altera gate-level libraries and includes behavioral simulation, HDL test benches, and tool command language scripting. ModelSim implementation and quality assurance practices are guided by IEEE standards.

ModelSim is widely used in many industries and is favored by many military and aerospace sector companies. [[

]]<sup>a,c,e</sup>

### 8.3.5 LabView

The LabView tool is used at the [[

]]<sup>a,c,e</sup>.

LabView is a system design software package that provides engineers with the tools they need to create any testing or measurement systems. It has the highest bandwidth vector signal analyzers and digitizers. A key benefit of LabView over other development environments is the extensive capability for accessing instrumentation hardware. It had drivers and abstraction layers for distinct types of instruments and buses that are represented as graphical nodes. The graphical nature makes it effective for test and measurement, automation, instrument control, data acquisition, and data analysis applications.

LabView is widely used in many industries.

### 8.3.6 TestComplete

TestComplete is used for [[

]]<sup>a,c,e</sup>

Over 4 million software professionals and 25,000 organizations across 194 countries use SmartBear tools. Among them more than 5000 companies use TestComplete: Cisco, J.P. Morgan, McAfee, Intuit and Boeing are in this list.

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### 8.3.7 TopJTAG Probe

The TopJTAG Probe is [[

]]<sup>a,c,e</sup>

### 8.3.8 Visual Studio

Visual Studio is an integrated development environment that includes code editor, debugger, compiler that supports the following programming languages: C, C++, C#. The Visual Studio Integrated development environment is used to perform compilation of the RPCT source code into Windows executable binary file. The RPCT is the multicomponent software-based platform that allows user to configure a complete RadICS Platform-based system and associated MATS. Visual Studio is used to support design process of the RPCT Output Verification Tool. RPCT Output Verification Tool is a software-based application that allows user to verify compliance between RPCT outputs and RadICS Chassis application layer design specification. RPCT Output Verification Tool does not generate outputs that can directly or indirectly contribute to the executable code of the safety related system.

Visual Studio is one of the leading integrated development environments used worldwide for software development in C/C++/C# and is used by many different companies for development of desktop software in different fields by different companies. Visual Studio compiler was successfully assessed by *exida* for SIL 3 capable applications. [[

]]<sup>a,c,e</sup>

### 8.3.9 PostgreSQL

PostgreSQL is an object-relational database management system used to implement the RPCT Application Project Database. RPCT Application Project Database is intended to store RPCT design data (i.e., RadICS Platform hardware configuration, Application Logic design, and MATS configuration) and to allow for retrieval at the request of the various RPCT software components.

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PostgreSQL is cross-platform, free and open-source software and is used in different fields by different companies.

### **8.3.10 Qt Creator**

Qt Creator is a cross-platform C++, JavaScript, and Qt Modeling Language integrated development environment. Qt Creator integrated development environment is used to support design process of the RPCT. RPCT is the multicomponent software-based platform that allows the user to configure a complete RadICS Platform-based system and associated MATS.

Qt Creator has been used in various systems requiring certification.

### **8.3.11 GNU Compiler Collection**

The GNU Compiler Collection is used for compiling RPCT source code into Linux executable file. GCC performs full compilation sequence:

- preprocessing
- compilation
- assembly
- linking

The GNU Compiler Collection parses source code and creates an abstract syntax tree. It then transforms it to RTL, optimizes it, and translates it into assembler language.

The GNU Compiler Collection is the most popular C/C++ compilation tool for UNIX-based OS for the last 30 years. It has open-source status and a very wide community of users. Most of safety-critical UNIX-based projects are using the GNU Compiler Collection as the C/C++ compiler.

## **8.4 Application Electronic Design Tool**

The AFBEL described in Section 8.2 is utilized to create the Application ED that implements the required safety system logic. RPCT is the tool used for this design process and was developed for the RadICS Platform.

The RPCT is an integrated development environment, which enables a system designer to completely configure the:

- Overall architecture of the RadICS Platform-based I&C system that includes one or more RadICS Chassis
- Detailed hardware configuration of each RadICS Chassis,
- Application ED to operate in each RadICS LM
- Tuning parameters in the Application ED for each LM
- Application Signals that will be monitored via MATS
- Architecture of the monitoring system that allows plant technicians and operators to perform their tasks





The Application ED is designed on logic schemas using the RPCT. The designer selects function blocks for each schema and links the blocks together to define the required signal flow. The blocks are selected from the AFBL via a simple dialog menu and inter-connected using icons and simple mouse operations. The inter-block signal values on a schema are internal to the schema and thus inaccessible outside the schema, except where connections are made via INPUT or OUTPUT blocks. The INPUT and OUTPUT blocks expand the signal connectivity to any number of logic schemas, to the hardware signal ports, and to external monitoring via the MATS. The RPCT User Manual explains the use of RPCT and is a resource manual for RadICS Platform-based system designers.

The RPCT is used for the design process to configure the entire system. The RPCT is used to download the completed set of configuration files to the RadICS LMs. The LM to be configured are removed from the RadICS Chassis and installed in the DLS for this operation. The RPCT is not used for any online activities.

## **8.5 Chapter 8 References**

- 1 IEC 61508:2010, "Functional Safety of Electrical/Electronic/Programmable Electronic Safety-related Systems"
- 2 ISO 9001:2008, "Quality management systems – Requirements"
- 3 MIL-I-45208, "Inspection System"
- 4 TÜV Rheinland Certificate No. 968/EL 850.00/12



## 9 Equipment Qualification and Analysis

### 9.1 Equipment Qualification

Environmental qualification testing of the RadICS Platform Qualification Test Specimen (QTS) and Supplemental QTS (SQTS) has been performed in accordance with the requirements of NRC RG 1.209 (Reference 9-1) and requirements of IEEE Std 323-2003 (Reference 9-2). The environmental qualification testing of the RadICS Platform QTS and SQTS is also performed in accordance with the requirements for qualifying digital computers IEEE Std 7-4.3.2-2003 (Reference 9-3) and RG 1.152 (Reference 9-4).

Seismic qualification testing has been performed in accordance with RG 1.100 (Reference 9-5), IEEE Std 344-2004 (Reference 9-6), and the generic seismic spectra provided in EPRI TR-107330 (Reference 9-7).

Electromagnetic compatibility (EMC) qualification testing has been performed in accordance with the guidance provided in RG 1.180 (Reference 9-8).

EPRI TR-107330 also describes an approach for generically qualifying commercial Programmable Logic Controllers for safety-related applications. This approach was found acceptable by the NRC (Reference 9-9). The generic qualification approach for the RadICS Platform uses guidance from EPRI TR-107330, as applicable, to meet the requirements of IEEE Std 323-2003 and other NRC guidance.

#### 9.1.1 Equipment to be Tested

The equipment to be tested is the RadICS Platform QTS and SQTS. In accordance with EPRI TR-107330, a representative sampling of the RadICS Platform components is identified for evaluation and qualification testing. The assembled components of the RadICS Platform QTS and SQTS include the following types of hardware modules and components:

- Chassis and Backplane
- Logic Modules
- Analog Inputs Modules
- Discrete Inputs Modules
- Wide Range Analog Inputs Modules
- Thermocouple Inputs Modules
- Resistance Temperature Detector Inputs Module
- Analog Outputs Modules
- Discrete Outputs Modules
- Optical Communication Modules
- Interface Protection Modules for External Interfaces
- Fan Cooling Hardware
- Cable Assemblies for Chassis and Module Connections

The RadICS Platform QTS and SQTS were exercised during qualification testing by a test system comprised of an industrial-grade data acquisition system (DAS) and a test specimen application program

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(TSAP). This test system is a non-qualified system whose purposes are to: (1) generate a series of known inputs to the RadICS Platform QTS and SQTS, and (2) monitor the corresponding outputs of the QTS and SQTS. Correct correspondence between input and output before, during, and after qualification tests and lack of spurious behavior are the key results that will demonstrate the predictable behavior of RadICS Platform hardware during normal and abnormal plant operating conditions.

Detailed descriptions of the RadICS Platform QTS and SQTS and the test system are provided in the QTS Specification (Reference 9-10) and SQTS Specification (Reference 9-11). QTS, SQTS, and DAS system arrangement and wiring drawings were prepared to provide additional hardware configuration information. A master configuration list was prepared to provide detailed RadICS Platform QTS and SQTS configuration information such as component serial numbers and electronic design version numbers (References 9-12 and 9-13).

## **9.1.2 Equipment Qualification Testing**

The RadICS Platform Equipment Qualification Plans (References 9-14 and 9-15) define the scope of testing to be performed and provides a test plan for each of the individual qualification tests. The basic qualification test sequence is shown in Figure 9-1 and the individual tests are described briefly below.

### **9.1.2.1 Factory Acceptance Testing**

Factory Acceptance Testing was performed at the end of the manufacturing and assembly phase to demonstrate compliance of the RadICS Platform QTS and SQTS and Test System with the QTS or SQTS Specification, as applicable. During Factory Acceptance Testing, the RadICS Platform QTS and SQTS were powered with the input/output I/O modules operating under control of the TSAP and the connected test system simulation devices. The I/O field circuits was configured with loads representative of the types intended for connection to the corresponding I/O module points, and other devices required for monitoring of the circuit operations. Burn-In Testing was performed by RPC Radiy as part of the manufacturing process.

### **9.1.2.2 Pre-Qualification Acceptance Testing**

The objective of Pre-Qualification Acceptance Testing was performed to demonstrate that the RadICS Platform QTS and SQTS operate as intended prior to start of qualification testing, and to provide baseline acceptance data for qualification testing implementation of the Operability and Prudency Tests. Section 5.2 of EPRI TR 107330 provides guidance for implementation of pre-qualification acceptance testing. The RadICS Pre-Qualification Acceptance Testing includes System Setup and Checkout Testing, Operability Testing, and Prudency Testing. The RadICS Pre-Qualification Acceptance Testing can be performed with the RadICS Platform QTS and SQTS in the environmental test chamber.



MANUFACTURING

Test Specimen and Test System  
Manufacture and Assembly

FACTORY ACCEPTANCE TESTING

Test Specimen and Test System Factory Acceptance Testing

PRE-QUALIFICATION ACCEPTANCE TESTING

Pre-Qualification Testing  
System Setup and Checkout Testing

Pre-Qualification Testing  
Operability Testing

Pre-Qualification Testing  
Prudency Testing

QUALIFICATION TESTING

Environmental Testing  
With Operability Testing at High Temp/RH, Low Temp/RH and ambient Temp/RH  
With Prudency Testing at High Temp/RH

Seismic Testing  
System Setup and Checkout Testing

Seismic Testing

Post-Seismic  
Operability Testing

Post-Seismic  
Prudency Testing

EMI/RFI Testing  
System Setup and Checkout Testing

EMI/RFI Emission Testing

EMI/RFI Susceptibility  
Testing

Electrical Fast Transient  
Testing

Electrostatic Discharge Testing

Surge Withstand Testing

Post-EMI/RFI, Electrical Fast Transient,  
Surge Withstand, Electrostatic Discharge  
Operability Testing

Post-EMI/RFI, Electrical Fast Transient,  
Surge Withstand, Electrostatic Discharge  
Prudency Testing

Class 1E to Non-1E Isolation Testing  
System Setup and Checkout Testing

Class 1E to Non-1E Isolation Testing

PERFORMANCE PROOF TESTING

Performance Proof Testing  
System Setup and Checkout Testing

Performance Proof Testing  
Operability Testing

Performance Proof Testing  
Prudency Testing

Figure 9-1: RadICS QTS and SQTS Qualification Testing Sequence



### **9.1.2.3 Environmental Testing**

The environmental testing demonstrated that the RadICS Platform QTS and SQTS did not experience failures due to abnormal service conditions of temperature and humidity as required by RG 1.209 and IEEE Std 323-2003. Section 4.3.6 of EPRI TR 107330 defines the recommended normal and abnormal temperature and humidity exposure levels the test specimen must withstand (i.e., the test specimen must continue to meet the manufacturer specified performance levels). The environmental testing sequence was:

- Assemble the RadICS Platform QTS and SQTS in the environmental test chamber
- Perform the Pre-Qualification Acceptance Testing
- Expose the RadICS Platform QTS and SQTS to varying temperature and humidity conditions according to the Environmental Testing procedures
- Perform Environmental Testing Operability and Prudence Testing at the times identified in the Environmental Testing procedures
- Remove the RadICS Platform QTS and SQTS from the Environmental Test chamber

The Environmental Test acceptance criteria are based on Section 4.3.6 of EPRI TR-107330.

### **9.1.2.4 Seismic Testing**

Seismic testing demonstrated the suitability of the RadICS Platform for qualification as a Category 1 seismic device based on seismic withstand testing performed on the RadICS Platform QTS and SQTS in accordance with RG 1.100 and IEEE Std 344-2004. Section 4.3.9 of EPRI TR 107330 (EPRI website version) defines the seismic test levels to which the test specimen was exposed, while the test specimen continues to meet the manufacturer specified performance levels. The seismic test acceptance criteria are based on Section 4.3.9 of EPRI TR-107330 (EPRI website version). The seismic testing can be performed in any order after completion of the environmental testing. The seismic testing sequence is:

- Setup the RadICS Platform QTS and SQTS on the Seismic Test table
- Perform the Pre-Seismic Testing System Setup and Checkout Test
- Perform Resonance Search testing on the RadICS Platform QTS and SQTS components
- Perform five seismic tests to the specified Operating Basis Earthquake (OBE) test levels
- Perform one seismic test to the specified Safe Shutdown Earthquake (SSE) test level
- Perform Post-Seismic Testing Operability and Prudence Testing
- Remove the RadICS Platform QTS and SQTS from the Seismic Test table

### **9.1.2.5 Electromagnetic Interference/Radio Frequency Interference Testing**

The objective of EMI/RFI testing was to demonstrate the suitability of the RadICS Platform for qualification as a safety-related device with respect to EMI/RFI emissions and susceptibility levels. EMI/RFI testing of the RadICS Platform QTS and SQTS were performed in accordance with RG 1.180, Revision 1, using additional guidance from EPRI TR-107330, as applicable. Grounding and shielding of the RadICS Platform is in accordance with IEEE Std 1050-1996 (Reference 9-16). Since the RadICS QTS and SQTS do not include the 120 V level power supplies, certain AC power-related tests are not applicable. The specific EMI/RFI tests performed include:

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- EMI/RFI Emissions Tests

MIL-STD-461E, CE101 (Reference 9-17)	Conducted Emissions, Low Frequency, AC and DC Power Leads
MIL-STD-461E, CE102 (Reference 9-17)	Conducted Emissions, High Frequency, AC and DC Power Leads
MIL-STD-461E, RE101 (Reference 9-17)	Radiated Emissions, Magnetic Field, QTS Surfaces and Leads
MIL-STD-461E, RE102 (Reference 9-17)	Radiated Emissions, Electric Field, Antenna Measurement

- EMI/RFI Susceptibility Tests

IEC 61000-4-6 (Reference 9-18)	Conducted Susceptibility, Induced RF Fields, Power/Signal Leads
IEC 61000-4-16 (Reference 9-19)	Conducted Susceptibility, Common Mode Disturbance, Power/Signal Leads
IEC 61000-4-8 (Reference 9-20)	Radiated Susceptibility, Magnetic Field, Helmholtz Coil Exposure
IEC 61000-4-9 (Reference 9-21)	Radiated Susceptibility, Magnetic Field, Pulsed
IEC 61000-4-10 (Reference 9-22)	Radiated Susceptibility, Magnetic Field, Damped Oscillatory
IEC 61000-4-3 (Reference 9-23)	Radiated Susceptibility, High Frequency, Antenna Exposure
MIL-STD-461 E, RS103 (Reference 9-17)	Radiated Susceptibility, High Frequency, Antenna Exposure [[ <sup>a,c,f</sup> ]]

The testing specified in IEC 61000-4-13 (Reference 9-24) is not applicable to the RadICS QTS or SQTs scope.

The EMI/RFI test acceptance criteria are based on Section 4.3.7 of EPRI TR-107330 and RG 1.180. The EMI/RFI testing can be performed in any order after completion of the environmental testing. The EMI/RFI testing sequence was:

- Setup the RadICS Platform QTS and SQTs in the EMI/RFI test chamber
- Perform the Pre-EMI/RFI Testing System Setup and Checkout Test
- Perform EMI/RFI Emissions Testing



- Perform EMI/RFI Susceptibility Testing
- Perform EMI/RFI Testing Operability and Prudency Testing

The electrical-related tests in described in Sections 9.1.2.5 through 9.1.2.9 are typically performed as a set. The EMI/RFI Testing Operability and Prudency Tests can be performed once at the end of the electrical-related tests as the Performance Proof Testing described in Section 9.1.2.10.

#### **9.1.2.6 Electrical Fast Transient Testing**

The objective of electrical fast transient (EFT) testing was to demonstrate the suitability of the RadICS Platform for qualification as a safety-related device with respect to EFT susceptibility levels. EFT testing of the RadICS Platform QTS and SQTs was performed in accordance with RG 1.180 using additional guidance from EPRI TR-107330, as applicable. The specific EFT test to be performed is IEC 61000-4-4, (Reference 9-25). The EFT testing can be performed in any order after completion of the environmental testing. The EFT acceptance criteria are based on Sections 4.6.2 and 4.3.7 of EPRI TR-107330 and RG 1.180. The EFT addresses the review guidance in BTP 7-11 (Reference 9-26).

#### **9.1.2.7 Surge Withstand Testing**

The objective of surge withstand testing was to demonstrate the suitability of the RadICS Platform for qualification as a safety-related device with respect to surge withstand levels. Surge withstand testing of the RadICS Platform QTS and SQTs was performed in accordance with RG 1.180, using additional guidance from EPRI TR-107330 as applicable. The specific surge withstand tests performed included:

IEC 61000-4-5 (Reference 9-27)	Surge Immunity Test
IEC 61000-4-12 (Reference 9-28)	Oscillatory Waves Immunity Test

The surge withstand testing can be performed in any order after completion of the environmental testing. The surge withstand test acceptance criteria are based on Section 4.6.2 of EPRI TR-107330 and RG 1.180. The surge withstand testing addresses the review guidance in BTP 7-11.

#### **9.1.2.8 Electrostatic Discharge Testing**

The objective of electrostatic discharge (ESD) testing was to demonstrate the suitability of the RadICS Platform for qualification as a safety-related device with respect to ESD withstand levels. EPRI TR-107330, Section 4.3.8, requires that the test specimen under qualification be tested for ESD withstand capability in accordance with the requirements of EPRI TR-102323 (Reference 9-29). In accordance with EPRI TR-102323, the specific ESD Test to be performed is the Electrostatic Discharge Immunity Test in Part 4-2 of IEC 61000-4-2 (Reference 9-30). RG 1.180 provides no guidance for ESD Testing. The ESD Testing can be performed in any order after completion of the environmental testing. The ESD acceptance criteria are based on Sections 4.3.8 of EPRI TR-107330.



#### **9.1.2.9 Class 1E to Non-Class 1E Isolation Testing**

The objective of Class 1E to non-Class 1E isolation testing was to demonstrate the suitability of the RadICS Platform for qualification as a safety-related device with respect to providing electrical isolation at non-Class 1E field connections, as required by IEEE Std 384-1992 (Reference 9-31). EPRI TR-107330, Section 6.3.6, requires that the test specimen under qualification be tested for Class 1E to non-Class 1E isolation capability in accordance with the requirements of EPRI TR-107330, Section 4.6.4.

The non-1E isolation testing can be performed in any order after completion of the environmental testing. The Class 1E to non-Class 1E isolation testing acceptance criteria are based on Sections 4.6.4 of EPRI TR-107330. The Class 1E to non-Class 1E isolation testing addresses the review guidance in BTP 7-11.

#### **9.1.2.10 Performance Proof Testing**

The objective of Performance Proof Testing was to demonstrate the continuing acceptable operation and performance of the RadICS Platform QTS and SQTs following completion of all hardware qualification testing. EPRI TR-107330, Section 5.5 requires a final performance of the Operability Test procedure on completion of qualification testing. As an alternative to this requirement, Performance Proof Testing will include a final performance of the System Setup and Checkout, Operability, and Prudency test procedures following completion of all hardware qualification testing, and comparison of the test results to the results for all previous performances of the Operability and Prudency test procedures. Acceptance criteria for performance monitoring of the RadICS Platform QTS and SQTs during Performance Proof Testing was specified separately in the System Setup and Checkout, Operability, and Prudency Test procedures. In addition, comparison of the Performance Proof Operability and Prudency Test data to all other Operability and Prudency test data shall not indicate an unacceptable change in performance of the RadICS Platform QTS or SQTs hardware.

#### **9.1.2.11 Operability Testing**

The objective of Operability Testing was to demonstrate the continuing correct function and performance of the RadICS Platform QTS and SQTs throughout qualification testing. Section 5.3 of EPRI TR-107330 describes the specific functional and performance tests to be performed as part of Operability Testing. These tests were implemented in the RadICS Platform QTS and SQTs Operability Test procedures as they are applicable to the RadICS Platform QTS or SQTs design. Section 5.5 of EPRI TR-107330 identifies the points at which the Operability Tests should be performed during hardware qualification testing.

Operability testing was performed at the following times during hardware qualification testing:

- With Pre-Qualification Acceptance Testing
- At the completion of the high temperature, high humidity phase of Environmental Testing
- At the completion of the low temperature and low humidity phases of Environmental Testing  
(Note: If the specified relative humidity cannot be achieved for the specified temperature, then separate tests can be performed after the lowest relative humidity has been achieved at the

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specified temperature followed by running the test at the lowest temperature that can be achieved the specified relative humidity.)

- At the completion of Environmental Testing
- At the completion of the Seismic Testing
- At the completion of the EMI/RFI, EFT, Surge Withstand, and ESD Testing
- With Performance Proof Testing

The operability tests satisfy the computer system testing requirements in IEEE Std 7-4.3.2-2003 Section 5.4.1.

#### **9.1.2.12 Prudency Testing**

The objective of Prudency Testing is to demonstrate the continuing correct function and performance of the RadICS Platform QTS and SQTS throughout qualification testing. Section 5.4 of EPRI TR-107330 describes the specific functional and performance tests to be performed as part of Prudency Testing. These tests were implemented in the RadICS Platform QTS and SQTS Prudency Test procedures as they are applicable to the RadICS Platform QTS or SQTS design. Section 5.5 of EPRI TR-107330 identifies the points at which the Prudency Tests should be performed during hardware qualification testing.

Prudency Testing was performed at the following times during hardware qualification testing.

- With Pre-Qualification Acceptance Testing
- At the completion of the high temperature, high humidity phase of Environmental Testing
- At the completion of the Seismic Testing
- At the completion of the EMI/RFI, EFT, Surge Withstand, and ESD Testing
- With Performance Proof Testing

The prudency tests satisfy the computer system testing requirements in IEEE Std 7-4.3.2-2003 Section 5.4.1.

#### **9.1.3 Generic Qualification Envelope**

The results of the RadICS Platform EQ testing were described in the Equipment Qualification Test Summary Report (Reference 9-32) and Supplemental Equipment Qualification Test Summary Report (Reference 9-33. Successful execution of the RadICS Platform EQ Plan qualified the generic RadICS Platform for the qualification envelope summarized in Table 9-1.

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Table 9-1: Generic Qualification Envelope for the RadICS Digital Safety I&amp;C Platform

Equipment Qualification Category	Regulatory Requirements	Source of Qualification Test Specification	Qualification Envelope and Test Levels	Qualification Test Acceptance Criteria	Qualification Status
Radiation Exposure	RG 1.209 and IEEE Std 323-2003	Section 4.3.6 of EPRI TR-107330	Qual. envelope: 1000 Rad Test level: 1000 Rad (by analysis)	Section 4.3.6 of EPRI TR-107330	Qualified by analysis.
Environmental (Temperature and Humidity)	RG 1.209 and IEEE Std 323-2003	Section 4.3.6 of EPRI TR-107330	Qualification envelope: 40 °F (4.4 °C) to 140 °F (60 °C) and 10 percent to 90 percent Relative Humidity (non-condensing) Test levels: 34.9 °F (1.6 °C) to 148.5 °F (64.7 °C) and 5 percent to 95 percent Relative Humidity (non-condensing)	Section 4.3.6 of EPRI TR-107330 Qualification envelope: 40 °F (4.4 °C) to 120 °F (48.9 °C) and 10 percent to 95 percent Relative Humidity (non-condensing) Figure 4.4 of EPRI TR-107330 Test Envelope: 40 °F (4.4 °C) to 140 °F (60 °C) and 5 percent to 90 percent Relative Humidity (non-condensing)	Qualification sequence successfully completed.
Seismic	RG 1.100 and IEEE Std 344-2004	Section 4.3.9 of EPRI TR-107330 (EPRI website version). The OBE and SSE tests shall follow the Required Response Spectrum (RRS) curve given as Figure 4-5 in EPRI TR-107330 within the limits	Resonance search as described in Section 7.1.4 of IEEE Std 344-2004	Section 4.3.9 of EPRI TR-107330	Some resonances in frame between 33 Hz and 100 Hz. Non-consequential because frame still considered rigid.



Equipment Qualification Category	Regulatory Requirements	Source of Qualification Test Specification	Qualification Envelope and Test Levels	Qualification Test Acceptance Criteria	Qualification Status
		of the seismic test table, with the proviso that the peak acceleration and minimum Zero Period Acceleration (ZPA) requirements are met. Note: The EPRI TR-107330 version in NRC Legacy ADAMS (not publicly available) has a Figure 4-5 that shows the OBE and SSE peak accelerations between 3 and 16 Hz.	Five triaxial OBEs tests with an RRS curve given as Figure 4-5 in EPRI TR-107330 with a peak acceleration of 9.8 g between 4.5 and 16 Hz and minimum ZPA of 4.9 g		Five OBE tests successfully completed. Test levels exceeded OBE levels in Figure 4-5 of EPRI TR-107330 for all frequencies between 1 Hz and 100 Hz.
			One triaxial SSE test with an RRS curve given as Figure 4-5 in EPRI TR-107330 with a peak acceleration of 14 g between 4.5 and 16 Hz and minimum ZPA of 7 g		SSE tests successfully completed. Test levels exceeded OBE levels in Figure 4-5 of EPRI TR-107330 for all frequencies between 1 Hz and 100 Hz.
EMI/RFI	RG 1.180	EMI/RFI Emissions Tests			
		MIL-STD-461E, CE101 Conducted Emissions, Low Frequency, AC and DC Power Leads	30 Hz to 10 kHz Applicable for 24 VDC leads Not applicable for 120 VAC leads	Section 4.3.7 of EPRI TR-107330 and RG 1.180 Emission limit: RG 1.180, Figure 3-1 DC Power Curve	Conducted emissions test sequence successfully completed.
		MIL-STD-461E, CE102: Conducted Emissions, High Frequency, AC and DC Power Leads	10 kHz to 2 MHz Applicable for 24 VDC leads Not applicable for 120 VAC leads	Section 4.3.7 of EPRI TR-107330 and RG 1.180 Emission limit: RG 1.180 Figure 3-2 28V Power Curve	Conducted emissions test sequence successfully completed.
		MIL-STD-461E, RE101: Radiated Emissions, Magnetic Field, QTS Surfaces and Leads	30 Hz to 100 kHz	Section 4.3.7 of EPRI TR-107330 and RG 1.180	Radiated emissions test sequence



Equipment Qualification Category	Regulatory Requirements	Source of Qualification Test Specification	Qualification Envelope and Test Levels	Qualification Test Acceptance Criteria	Qualification Status
				Emission limit: RG 1.180 Figure 3-3 RE101 Operating Envelope	successfully completed.
		MIL-STD-461E, RE102: Radiated Emissions, Electric Field, Antenna Measurement	2 MHz to 1 GHz	Section 4.3.7 of EPRI TR-107330 and RG 1.180 Emission limit: RG 1.180 Figure 3-4 RE102 Operating Envelope	Radiated emissions test sequence successfully completed.
		EMI/RFI Susceptibility Tests			
		IEC 61000-4-6: Conducted Susceptibility, Induced RF Fields, Power/Signal Leads	150 kHz to 80 MHz Section 4.3.7 of EPRI TR-107330 and RG 1.180 Susceptibility test level for power leads Not applicable for 120 VAC leads	Section 4.3.7 of EPRI TR-107330, RG 1.180, and IEC 61000-4-6 Susceptibility test level - signal and 24 VDC power leads: 126 dB $\mu$ V	Conducted susceptibility test sequence successfully completed at 140 dB $\mu$ V at 10 V.
		IEC 61000-4-16: Conducted Susceptibility, Common Mode Disturbance, Power/Signal Leads	15 Hz to 150 kHz and DC portion on Digital Inputs	Section 4.3.7 of EPRI TR-107330 and RG 1.180 Susceptibility test level - power leads: RG 1.180 Table 11 (Level 3)	Conducted susceptibility test sequence successfully completed at: 0.1 V <sub>rms</sub> (15–150 Hz) 1 V <sub>rms</sub> (150–1.5 kHz) 1–10 V <sub>rms</sub> (1.5–15 kHz) 10 V <sub>rms</sub> (15–150 kHz).
				Section 4.3.7 of EPRI TR-107330 and RG 1.180	Conducted susceptibility test



Equipment Qualification Category	Regulatory Requirements	Source of Qualification Test Specification	Qualification Envelope and Test Levels	Qualification Test Acceptance Criteria	Qualification Status
				Susceptibility test level - signal leads: RG 1.180 Table 15 (Level 2)	sequence successfully completed at: 0.03 V <sub>rms</sub> (15–150 Hz) 0.3 V <sub>rms</sub> (150–1.5 kHz) 0.3–3 V <sub>rms</sub> (1.5–15 kHz) 3 V <sub>rms</sub> (15–150 kHz).
		IEC 61000-4-8: Radiated Susceptibility, Magnetic Field, Helmholtz Coil Exposure	60 Hz	Section 4.3.7 of EPRI TR-107330 and RG 1.180 Susceptibility test level - continuous: 30 A/m	Radiated susceptibility test sequence successfully completed with continuous pulses at: 30 A/m (152 dBpT).
				Section 4.3.7 of EPRI TR-107330 and RG 1.180 Susceptibility test level - short duration: 300 A/m	Radiated susceptibility test sequence successfully completed with short duration pulses at: 300 A/m (172 dBpT).
		IEC 61000-4-9: Radiated Susceptibility, Magnetic Field, Pulsed	60 Hz	Section 4.3.7 of EPRI TR-107330 and RG 1.180 Susceptibility test level: 300 A/m	Radiated susceptibility test sequence successfully completed at 300 A/m (172 dBpT).
		IEC 61000-4-10: Radiated Susceptibility, Magnetic Field, Damped Oscillatory	100 kHz and 1 MHz	Section 4.3.7 of EPRI TR-107330 and RG 1.180 Susceptibility test level: 30 A/m	Radiated susceptibility test sequence successfully completed at 30 A/m (152 dBpT).



Equipment Qualification Category	Regulatory Requirements	Source of Qualification Test Specification	Qualification Envelope and Test Levels	Qualification Test Acceptance Criteria	Qualification Status
		IEC 61000-4-3: Radiated Susceptibility, High Frequency, Antenna Exposure	26 MHz to 1 GHz	Section 4.3.7 of EPRI TR-107330 and RG 1.180 Susceptibility test level: 10 V/m	Radiated susceptibility test sequence successfully completed at 10 V/m.
		MIL-STD-461E, RS103: Radiated Susceptibility, High Frequency, Antenna Exposure	1 GHz to 10 GHz	Section 4.3.7 of EPRI TR-107330 and RG 1.180 Susceptibility test level: 10 V/m	Radiated susceptibility test sequence successfully completed at 10 V/m.
Electrical Fast Transient	RG 1.180	IEC 61000-4-4	Power Leads (24 VDC), Test Voltage Level: 2 kV Signal Leads, Test Voltage Level: 1 kV	Sections 4.6.2 and 4.3.7 of EPRI TR-107330 and RG 1.180	Surge withstand test sequence successfully completed at 2 kV for power leads and 1 kV for signal leads.
Surge Withstand	RG 1.180	Table 22 of RG 1.180 defines the IEC 61000-4-12 Ring Wave and IEC 61000 4-5 Combination Wave surge withstand levels for power supplies installed in Category B locations with surge waveform Low Exposure levels	For 24 VDC power leads, the corresponding Ring Wave surge withstand level is 1 kV and the corresponding Combination Wave surge withstand level is 1 kV open circuit and 0.5 kA short circuit. The RadICS Platform will typically be connected to an external 120 VAC power supply provided by the end user.		Surge withstand test sequence for power supplies successfully completed at 2 kV for line to ground and 1 kV line to line.
		Table 15 of RG 1.180 defines the IEC 61000-4-12 Ring Wave and IEC 61000 4-5 Combination Wave surge withstand levels for signal leads in Low Exposure locations with Level 2 surge waveforms			Surge withstand test sequence successfully completed for signal leads at 2 kV for line to ground and 1 kV line to line.



Equipment Qualification Category	Regulatory Requirements	Source of Qualification Test Specification	Qualification Envelope and Test Levels	Qualification Test Acceptance Criteria	Qualification Status
		IEC 61000-4-5	For signal leads in Low Exposure locations with Level 2 surge waveforms, the corresponding Ring Wave surge withstand level is 1 kV and the corresponding Combination Wave surge withstand level is 1 kV open circuit and 0.5 kA short circuit.	Section 4.6.2 of EPRI TR-107330 and RG 1.180 The RadICS QTS and SQTS configurations corresponds to the Level 2 Switching configuration described in Table 4.7 from NUREG/CR-5609 (Reference 9-34).	Surge withstand test sequence successfully completed for signal leads at 1 kV open circuit test voltage and 0.5 kA short circuit.
		IEC 61000-4-12			Surge withstand test sequence successfully completed for ring wave at 1 kV test voltage.
Electrostatic Discharge	EPRI TR 107330, Section 4.3.8, requires that the test specimen under qualification be tested for ESD withstand capability in accordance with the requirements of EPRI TR-102323. RG 1.180 provides no guidance or requirements for ESD Testing.	IEC 61000-4-2	Maximum test levels of 15 kV for air discharges and 8 kV for contact discharges, corresponding to IEC 61000-4-2 Level 4. Testing to contact discharges will include the lower levels of 6 kV, 4 kV, and 2 kV. Testing to air discharges will include the lower levels of 8 kV, 4 kV, and 2 kV.	Sections 4.3.8 of EPRI TR-107330	Contact discharge test successfully completed at 2 kV, 4 kV, 6 kV, and 8 kV. Air Discharge test successfully completed at 2 kV, 4 kV, 6 kV, 8 kV, and 15 kV.



Equipment Qualification Category	Regulatory Requirements	Source of Qualification Test Specification	Qualification Envelope and Test Levels	Qualification Test Acceptance Criteria	Qualification Status
Class 1E to Non-Class 1E Isolation	IEEE Std 384-1992. EPRI TR 107330, Section 6.3.6, requires that the test specimen under qualification be tested for Class 1E to non-Class 1E isolation capability in accordance with the requirements of EPRI TR-107330, Section 4.6.4.	Sections 4.6.4 of EPRI TR-107330	Class 1E to Non-1E isolation points are tested for a maximum isolation capability of 250 VAC and 250 VDC applied for 30 seconds.	Sections 4.6.4 of EPRI TR-107330	Class 1E to Non-1E isolation test successfully completed at 250 VAC ( $\pm 10$ VAC) at 60 Hz or 250 VDC ( $\pm 10$ VDC) applied for $\geq 30$ seconds.





#### 9.1.4 Maintenance of Generic Qualification

Hardware type tests were performed on a specific version of the RadICS Platform. However, the specific version of the RadICS Platform supplied for nuclear plant applications may be a later version. If later versions are supplied for nuclear safety-related applications, the qualification basis described in the RadICS Platform Equipment Qualification Report will be augmented with technical evaluations or additional testing, based on the requirements established in Section 6.4 of IEEE Std 323-2003.

### 9.2 Equipment Analysis

This section describes the following generic analyses that have been performed to establish the foundations for future system-level analyses for project-specific RadICS Platform-based systems:

- Board/device-level predictive reliability and safety analyses, which includes an FMEDA
- Setpoint analysis support
- Limited life parts analysis
- Radiation susceptibility

#### 9.2.1 Failure Modes, Effects, and Diagnostic Analysis

##### 9.2.1.1 Objective

The objectives of the board/device-level predictive reliability and safety analyses are to provide generic FMEDA and reliability data for the RadICS Platform hardware boards/devices identified in Section 6.2. These generic results are intended to be used as input data to support a system-level FMEA and reliability analysis for an NPP-specific RadICS Platform-based system.

##### 9.2.1.2 Approach for the FMEDA

An FMEA is a systematic way to identify and evaluate the effects of different component failure modes, to determine what could eliminate or reduce the chance of failure, and to document the system in consideration. A FMEDA (Failure Mode Effect and Diagnostic Analysis) is an FMEA extension. It combines standard FMEA techniques with the extension to identify automatic diagnostic techniques and the failure modes relevant to safety instrumented system design. It is a technique recommended to generate failure rates for each important category (safe detected, safe undetected, dangerous detected, dangerous undetected, fail high, fail low, etc.) in the safety models. The format for the FMEDA is an extension of the standard FMEA format from MIL-STD-1629A (Reference 9-35). The FMEDAs are consistent with the FMEA guidance of IEEE Std 352-1987, Sections 4.1, 4.4, and 4.5 (Reference 9-36).

The failure rate data used for the FMEDAs are from the Electrical and Mechanical Component Reliability Handbook (Reference 9-37), which was derived using over ten billion unit operational hours of field failure data from multiple sources and failure data from various databases. The rates were chosen in a way that is appropriate for safety integrity level verification calculations. It is expected that the actual number of field failures due to random events will be less than the number predicted by these failure rates. For hardware assessment according to IEC 61508, only random equipment failures are of interest. It is assumed that the equipment has been properly selected for the application and is adequately

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commissioned such that early life failures (infant mortality) may be excluded from the analysis. The methods used to estimate the reliability of RadICS Modules that are installed in a rack are based on the Electrical and Mechanical Component Reliability Handbook instead of MIL-HDBK-217F, which is recommended in IEEE Std 352-1987. The Electrical and Mechanical Component Reliability Handbook provides more current data for modern electronic hardware than MIL-HDBK-217F.

The FMEDA for each RadICS Module considered the distinct groups of components that affected module functionality. The following groupings were evaluated:

Common	The portion of the RadICS Module that is always used.
Input	The portion of the RadICS Module used by one on-board input channel (designated DI and AI, respectively, for discrete and analog channels).
Output	The portion of the RadICS Module used by one on-board output channel (designated DO and AO, respectively, for discrete and analog channels).
LVDS	The portion of the LM providing communication to one I/O Module.

The following definitions for the failure of the device were considered to judge the failure behavior of the RadICS Modules.

Fail-Safe State	State where all discrete outputs are de-energized.
Fail Safe	Failure that causes the device to go to the defined fail-safe state without a demand from the process. (abbreviation: S)
Fail Safe Detected	Failure that is detected by automatic self-diagnostics, which causes the output signal to go to the predefined fail-safe state (i.e., AOMs and/or DOMs deenergized). (abbreviation: SD)
Fail Safe Undetected	Failure that is safe and that is not diagnosed by automatic self-diagnostics. (abbreviation: SU)
Fail Dangerous	Failure that does not respond to a demand from the process (i.e., being unable to go to the defined fail-safe state).
Analog Input	Failure that deviates the measured input value by more than 2% of span and leaves the value within active scale.
Fail Dangerous Detected	Failure that is dangerous but is detected by automatic diagnostics. (abbreviation: DD)
Fail Dangerous Undetected	Failure that is dangerous and that is not being diagnosed by automatic diagnostics. (abbreviation: DU)



Annunciation Detected	Failure that does not directly impact safety but does impact the ability to detect a future fault (e.g., a fault in a diagnostic circuit) and that is detected by internal diagnostics. A Fail Annunciation Detected failure leads to a false diagnostic alarm. This condition leads to maintenance, and if the safety channel is not shut down (put into the safe state) during this maintenance, the time must be accounted for in any system level reliability calculation. (abbreviation: AD)
Annunciation Undetected	Failure that does not directly impact safety but does impact the ability to detect a future fault (e.g., a fault in a diagnostic circuit) and that is not detected by internal diagnostics. AU failures are not counted for Safe Failure Fraction calculation. (abbreviation: AU)
Fail Dangerous Undetected after Surveillance Test	Failure that is dangerous and that is not being diagnosed by either automatic diagnostics or the periodic surveillance test. (abbreviation: DUPT)

The failure categories listed above expand on the categories listed in IEC 61508:2010, which are only safe and dangerous, both detected and undetected. Under IEC 61508, Edition 2010, the No Effect failures cannot contribute to the failure rate of the safety function.

The Annunciation failures are provided for those who wish to do reliability modeling more detailed than required by IEC 61508. It is assumed that the probability model will correctly account for the Annunciation failures; otherwise the Annunciation Undetected failures have to be classified as Dangerous Undetected failures according to IEC 61508 (worst-case assumption).

### 9.2.1.3 Results of the Board/Device-Level Reliability Analyses

A summary of the predicted reliability for each board/device is presented in Table 9-2. All results are reported in Failure in Time ( $1 \times 10^{-9}$  failures per hour) at sea level.

**Table 9-2: Summary of the Predicted Reliability of RadICS Modules**

Module	Portion	$\lambda_{SD}$	$\lambda_{SU}$	$\lambda_{DD}$	$\lambda_{DU}$	$\lambda_{AD}$	$\lambda_{AU}$	$\lambda_{DUaPT}$
II								

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### 9.2.2 Setpoint Analysis Support

EPRI TR-107330, Section 4.2.4 (recommends that the qualifier provide information about the qualified hardware to support a project-specific setpoint analysis. RG 1.105 (Reference 9-38) endorses ISA-S67.04-1994 (Reference 9-39), with qualifications, as the basis for performing a project-specific setpoint analysis.

- A. Calibrated accuracy, including hysteresis and non-linearity, of the analog inputs and outputs
- B. Repeatability of the analog inputs and outputs
- C. Temperature sensitivity of the analog inputs and outputs
- D. Drift with time of the analog inputs and outputs



- E. Power supply variation effects on the analog inputs and outputs
- F. Error contribution of any arithmetic operations needed to implement a setpoint. The accuracy is based on using two additions and one multiplication on an input value plus a comparison. The error contributions are provided for both integer and floating point calculations.
- G. In addition, EPRI recommends that the qualification process identify those components, if any, on analog I/O modules that are sensitive to the following:
  - Components where vibration could affect accuracy (e.g., potentiometers)
  - Components where radiation exposure could affect accuracy
  - Components where relative humidity could affect accuracy

The objective of the RadICS Setpoint Analysis Support Documents (References 9-40 and 9-41) is to provide a single, concise listing of the accuracy, drift, and other relevant specifications of the RadICS Platform. These specifications are intended to enable a licensee to calculate instrument measurement uncertainties and establish critical control setpoints for a project-specific RadICS Platform-based system based on ISA-S67.04-1994.

### **9.2.2.2 Approach**

The Setpoint Analysis Support document provides the data recommended in EPRI TR-107330 for the following RadICS Platform components:

- Analog Inputs Modules (i.e., AIM, WAIM, TIM, and RIM)
- Discrete Inputs Modules
- Analog Outputs Modules
- Discrete Outputs Modules

The accuracy specifications have been compiled from manufacturer's documentation and the results of qualification testing of the RadICS Platform QTS and SQTS.

### **9.2.3 Limited Life Parts Analysis**

EPRI TR-107330, Section 4.7.8.2 requires the qualifier to perform a component aging analysis on the qualified hardware based on the normal and abnormal environmental conditions to which it is exposed. The purpose of this analysis is to provide a "qualified life" for components associated with the digital I&C platform under qualification. The component aging analysis described in EPRI TR-107330, Section 4.7.8.2 is not required for the standard RadICS Platform hardware, which will be installed in a mild environment, where repair is possible after an accident. Aging analysis is required only where equipment is installed in a harsh environment, where repair is not possible after an accident. Radiy will not use the alternate guidance for aging of digital equipment in EPRI TR-107330, Section 4.7.8.2, for equipment located in mild environments.

Qualified life is a term not typically applied to digital I&C equipment intended for installation in a mild environment, because accelerated aging is not part of the EQ program. In addition, IEEE Std 323-2003, Section 4.1 states that, "A qualified life is not required for equipment located in a mild environment and which has no significant aging mechanisms." RG 1.209, Paragraph C.(1), states that, "The NRC does not

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consider the age conditioning (of IEEE Std 323-2003) to be applicable because of the absence of significant aging mechanisms on microprocessor-based modules.”

The types of electronic components that typically have life limits are batteries and electrolytic capacitors. The RadICS Platform equipment described in Section 6.2 does not use any batteries or electrolytic capacitors that require regular replacement.

Project-specific RadICS Platform-based systems will be examined during the design phase to confirm if any life limited components are introduced in the hardware for a specific application. If any such components are identified, appropriate measures will be identified in the Product Safety Manual to manage the life-limited component.

### 9.2.4 Radiation Susceptibility Analysis

The radiation exposure susceptibility analysis demonstrates that the RadICS Platform Modules will not experience failures or unacceptable degradation due to expected radiation exposure from normal and abnormal service conditions as required by RG 1.209 and EPRI TR-107330. Section 4.3.6 of EPRI TR 107330 defines the normal and abnormal radiation exposure levels the equipment must withstand and continue to meet the specified performance levels.

## 9.3 Chapter 9 References

- 1 Regulatory Guide 1.209, “Guidelines for Environmental Qualification of Safety-Related Computer-Based Instrumentation and Control Systems in Nuclear Power Plants,” March 2007
- 2 IEEE Std 323-2003, “Standard for Qualifying Class 1E Equipment for Nuclear Power Generating Stations”
- 3 IEEE Std 7-4.3.2-2003, “Standard Criteria for Digital Computers in Safety Systems of Nuclear Power Generating Stations”
- 4 Regulatory Guide 1.152, Revision 3, “Criteria for Use of Computers in Safety Systems of Nuclear Power Plants”
- 5 Regulatory Guide 1.100, Revision 3, “Seismic Qualification of Electric and Mechanical Equipment for Nuclear Power Plants,” September 2009
- 6 IEEE Std 344-2004, “Recommended Practice for Seismic Qualification of Class 1E Equipment for Nuclear Power Generating Stations”
- 7 EPRI TR-107330, “Generic Requirements Specification for Qualifying a Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants,” December 1996
- 8 Regulatory Guide 1.180, Revision 1, “Guidelines for Evaluating Electromagnetic and Radio-Frequency Interference in Safety-Related Instrumentation and Control System,” October 2003
- 9 NRC Letter dated July 30, 1998 to Mr. J. Naser (EPRI), “Safety Evaluation by the Office of Nuclear Reactor Regulation Electric Power Research Institute Topical Report, TR-107330, Final Report, Generic Requirements Specification for Qualifying a Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants”
- 10 NRC RadICS Test Specimen (RTS-001) System Requirements Specification, Document No. 2015-RTS001-SRS-009

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- 11 NRC Supplement RadICS Test Specimen (SRTS-003) System Requirements Specification, Document No. 2019-SRTS003-SRS-009
- 12 RadICS Platform Master Configuration List, Radics LLC Document No. 2016-RTS002-MCL-018
- 13 RadICS Platform Master Configuration List, Radics LLC Document No. 2019-SRTS004-MCL-018
- 14 RadICS Equipment Qualification Test Plan, Radics LLC Document No. 2016-RTS002-EQTP-004
- 15 RadICS Supplemental Equipment Qualification Test Plan, Radics LLC Document No. 2019-SRTS004-EQTP-004
- 16 IEEE Std 1050-1996, Guide for Instrumentation and Control Equipment Grounding in Generating Stations
- 17 Military Standard 461E, "Requirements for the Control of Electromagnetic Interference Characteristics of Subsystems and Equipment," August 20, 1999
- 18 IEC 61000-4-6, "Testing and Measurement Techniques, Immunity to Conducted Disturbances Induced by Radio-Frequency Fields," May 2006
- 19 IEC 61000-4-16, "Testing and Measurement Techniques, Tests for Immunity to Conducted, Common Mode Disturbances in the Frequency Range 0 Hz to 150 kHz," July 2002
- 20 IEC 61000-4-8, "Testing and Measurement Techniques, Power Frequency Magnetic Field Immunity Test," March 2001
- 21 IEC 61000-4-9, "Testing and Measurement Techniques, Pulse Magnetic Field Immunity Test," March 2001
- 22 IEC 61000-4-10, "Testing and Measurement Techniques, Damped Oscillatory Magnetic Field Immunity Test," March 2001
- 23 IEC 61000-4-3, "Testing and Measurement Techniques, Radiated, Radio-Frequency, Electromagnetic Field Immunity Test," February 2006
- 24 IEC 61000-4-13, "Testing and Measurement Techniques, Harmonics and Interharmonics Including Mains Signaling at AC Power Ports, Low Frequency Immunity Tests," March 2002
- 25 IEC 61000-4-4, "Testing and Measurement Techniques, Section 4: Electrical Fast Transient/Burst Immunity Test," July 2004
- 26 BTP 7-11, Revision 5, Guidance on Application and Qualification of Isolation Devices
- 27 IEC 61000-4-5, "Testing and Measurement Techniques, Section 5: Surge Immunity Test," November 2005
- 28 IEC 61000-4-12, "Testing and Measurement Techniques, Section 12: Oscillatory Waves Immunity Tests," September 2006
- 29 EPRI TR-102323, Revision 1, "Guidelines for Electromagnetic Interference Testing in Power Plants," January 1997
- 30 IEC 61000-4-2, "Testing and Measurement Techniques, Section 2: Electrostatic Discharge Immunity Test," April 2001
- 31 IEEE Std 384-1992, "Standard Criteria for Independence of Class 1E Equipment and Circuits"
- 32 RadICS Equipment Qualification Test Summary Report, Radics LLC Document No. 2016-RTS002-EQTSR-040
- 33 RadICS Supplemental Equipment Qualification Test Summary Report, Radics LLC Document No. 2019-SRTS004-EQTSR-040
- 34 NUREG/CR-5609, "Electromagnetic Compatibility Testing for Conducted Susceptibility Along Interconnecting Signal Lines," August 2003



- 35 MIL-STD-1629A, Military Standard: Procedures for Performing a Failure Mode, Effects, and Criticality Analysis, 1980
- 36 IEEE Std 352-1987, "Guide for General Principles of Reliability Analysis of Nuclear Power Generating Station Safety Systems"
- 37 **exida** LLC, Electrical & Mechanical Component Reliability Handbook, Second Edition, 2008, ISBN 978-0-9727234-6-6
- 38 Regulatory Guide 1.105, Revision 3, "Setpoints for Safety-Related Instrumentation", December 1999
- 39 ISA-S67.04-1994, "Methodologies for the Determination of Setpoints for Nuclear Safety-Related Instrumentation", Instrument Society of America
- 40 RadICS Setpoint Analysis Support, Radics LLC Document No. 2016-RTS002-SAS-003
- 41 RadICS Setpoint Analysis Support, Radics LLC Document No. 2019-SRTS004-SAS-003





## 10 Diversity and Defense-In-Depth

### 10.1 Overview

Digital I&C systems can be vulnerable to CCFs caused by software, firmware, or programmed logic errors, which could defeat the redundancy achieved by hardware architecture. CCFs are of particular interest for a digital I&C system designed to perform in nuclear safety-related projects like a Protection System (PS).

### 10.2 Digital Common Cause Failures

NRC considers CCFs in digital systems to be a beyond design basis event and specifies the special methods for providing the necessary protection for digital PS projects. These methods use a D3 assessment as the primary design tool. Defense-in-depth is a principle that ensures multiple layers of I&C systems exist to provide protection against a wide spectrum of anticipated operational occurrences and postulated accidents, both design basis and beyond design basis. Diversity is a principle that ensures digital I&C systems are protected against postulated CCFs, specifically in portions of a digital I&C system that are not fully testable (e.g., the software, firmware, or programmable logic).

Protection against CCF is primarily provided at the overall I&C architecture level by implementing different lines of defense and diversity. Regulatory guidance on performing D3 analyses is provided in two main documents: BTP 7-19 (Reference 10-1) and NUREG/CR-6303 (Reference 10-2). These guidance documents are tailored to a D3 assessment performed for a project-specific safety-related I&C system, so much of the guidance is not applicable to a generic platform qualification process.

### 10.3 Defense Against Common Cause Failures

Individual safety I&C systems are generally designed with identical equipment (same hardware and software) in redundant divisions, therefore raising a CCF issue at the system level.

To ensure defense against CCF at the system level, the RadICS Platform employs several defensive measures that together provide protection against and elimination of CCFs. These defensive measures are as follows:

- Electronic Design Development Process Quality
- Hardware Independence Principles
- Platform Diversity
- Defense-in-Depth

In combination, these measures work together to reduce the risks of CCF to acceptable levels within applications that utilize the RadICS Platform.

#### 10.3.1 Electronic Design Development Process Quality

As stated in IEC 60880-2006 (Reference 10-3), Section 13.2, "Design of software against Common Cause Failure":

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"The basic and most important defense against common cause failure due to software is to produce software of the highest quality (i.e., as error-free as possible)."

The following are measures taken by Radiy and RadICS LLC during the electronic design development process as a line of defense against electronic design CCFs (as described in Chapter 6):

- Program code volume reduction due to application of FPGA as programmable components
- Application of distributed electronic design and separation of safety-related functions (IEC 61266 category A functions) from those of lesser categories (i.e., IEC 61266 (Reference 10-4) Categories B and C functions) and non-safety functions
- Application of development methods and tools aimed to prevent introduction of faults into the electronic designs
- Self-diagnostic testing and fault tolerant design features (validated by FIT as described in Section 7.4.2.1)
- Defensive programming
- Fail-safe design features

The RadICS Module Electronic Designs are based on life cycle processes that guarantee achievement of a robust level of quality (see Chapters 7 and 8). It aims at avoiding errors by means of:

- Adherence to a strict and phased development process
- Re-use of proven components
- Use of simple and proven design principles based on clearly defined rules
- Avoidance of unnecessary complexity
- Use of proven tools for automated code generation as much as possible to reduce risk of human errors
- Eliminating errors as soon as possible
- Documents produced during a phase are formally verified and reviewed before starting the next phase
- V&V tasks are performed by an independent team
- Static verification is performed on all electronic design VHDL and parameters
- Unit tests, integration tests, validation tests, factory acceptance tests, and site tests are planned and performed

### 10.3.2 Hardware Independence Principles

The steps of defense against hardware CCFs realized for both the RadICS Platform and RadICS Platform-based projects include adherence to independence principle. Generally, adherence to independence principle means that the I&C system should preserve its capacity to execute prescribed functions necessary to ensure nuclear power plant safety under failure or deliberate inactivation of one redundant channel. Radiy best practices to implement this principle are the following:

- Screening and galvanic separation of input, output circuits and power circuits in each channel using electro-optical components
- Radial ("point-to-point") structure of connections between channels to preserve the possibility and accuracy of data exchange among the rest of channels in case one of them fails

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- Physical separation of redundant I&C system channels that are housed in separate cabinets and powered from different sources
- Application of technical solutions and components proven in nuclear power plant operation experience

The independence features of the RadICS Platform are described in Section 6.6.

### 10.3.3 RadICS Platform Diversity Assessment

As stated in NUREG/CR-6303, Section 2.6, "Diversity":

"Diversity is a principle in instrumentation systems of sensing different parameters, using different technologies, using different logic or algorithms, or using different actuation means to provide several ways of detecting and responding to a significant event. "

The RadICS Platform employs several internal diversity features to provide sufficient protection to address CCFs that may be introduced using digital FPGA technology within the RadICS Platform. To accomplish this, the RadICS Platform addresses the following CCF vulnerabilities that are inherent in FPGA design technology used in the RadICS Modules:

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The validation of the independent and diverse self-tests and diagnostics, Netlist self-tests, as well as, the CPLD watchdog functions are accomplished by the RadICS Module FITs. The Module FITs demonstrate that each RadICS Module detects, reports, and performs the appropriate actions in accordance with the three defined fault types. Module FIT demonstrates that all Module Hardware Unit failures are covered by the Module self-test and diagnostic logics and the CPLD watchdog functions accordingly to place the RadICS Platform in a safe state when required and allows for these functions to mitigate any CCF vulnerabilities. The Module FIT cases were developed using the summary of the self-tests credited in the FMEDA for each Module. The validation is performed by the V&V organization as described in Section 7.4.2.1 and 7.4.5.2.

Figure 10-1 shows the diverse measures inherent to the RadICS Platform that are used to mitigate CCF vulnerabilities. The combination of these diverse measures ensure protection against the postulated CCFs.

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**Figure 10-1: Diverse Measures to Mitigate CCF Vulnerabilities**

Human diversity is not specifically credited in the RadICS Platform for mitigating the potential for digital CCFs. The RadICS Platform meets requirements for having a design team and an independent verification and validation team; however, the RadICS Platform does not require an additional independent design or verification and validation team since it would provide minimal benefits in eliminating digital CCFs. The basis for not incorporating additional human diversity into the Electronic Design development process is consistent with the view that independently developed software is very likely to contain CCF modes, as discussed in a Massachusetts Institute of Technology research report on hazards analysis. It should be noted that there are additional diversity attributes (e.g., human, technological, and functional) that are implicit attributes of the FPGA and CPLD manufacturing



equipment, FPGA and CPLD chip designs, and configuration tools (e.g., Quartus II and RadICS Platform Configuration Tool); however, they are not explicitly defined nor verified for the RadICS Platform diversity strategy.

The RadICS Platform diversity strategy is based on insights drawn from recent Massachusetts Institute of Technology research report sponsored by NRC that independently developed software is very likely to still contain CCF modes (Reference 10-5). The research report noted that "almost all serious accidents caused by software have involved errors in the requirements, not in the implementation of those requirements in software code." The report noted that the software requirements have had missing cases or incorrect assumptions about the behavior of how the system operated. These problems were attributed to misunderstandings by the engineers of the requirements for safe behavior, such as an omission of what to do and circumstances that are not anticipated or considered. Software may be considered "correct" if it successfully implements its requirements, but the requirements may be unsafe in terms of the specified behavior in the surrounding system, the requirements may be incomplete, or the software may exhibit unintended (and unsafe) behavior beyond what is specified in the requirements. The report noted that redundancy or even multiple versions of the implementations of the requirements does not help in these cases.

The National Research Council was asked by the NRC to conduct a study on application of digital I&C technology to commercial nuclear power plant operations (Reference 10-6). The study has several conclusions and recommendations that are relevant to the application of diversity in the RadICS Platform design. With respect to common-mode software failure potential, the report concluded that use of different programming languages, different design approaches meeting the same functional requirements, different design teams, or different vendors' equipment used to perform the same function is not likely to be effective in achieving diversity (i.e., none of these methods is a proof of independence of failures). The report noted that there is no generally applicable, effective way to evaluate diversity between two pieces of software performing the same function. Superficial or surface (syntactic) differences do not imply failure independence, nor does the use of different algorithms to achieve the same functions.

A more effective means of addressing these types of errors is to use the appropriate system design development techniques that ensure the correctness and completeness of the system requirements (e.g., plant safety analyses, system FMEA, platform FMEDA, diversity and defense-in-depth analyses, and multidiscipline design reviews).

*N*-version software diversity has been proposed by some as a means of dealing with the uncertainties of design faults in a computer system implementation. One researcher looked at the question "does software diversity buy you more reliability?" (Reference 10-7) The research was motivated by the additional question from a system engineering viewpoint that there may be alternative design options at the systems engineering level that are more cost-effective. The paper noted that the Knight and Leveson experiment did a service to the computing community by showing that failure independence of design faults cannot be assumed. It further noted that from a theoretical standpoint, it has been shown that any variation in the degree of difficulty for particular inputs will result in failure dependency. The paper suggested that excessive reliance on software diversity may be a case of diminishing returns (i.e., high conformity to the wrong specification). As such, it might make more sense to utilize diversity at a higher level so that there is some defense-in-depth against faults in the requirements.

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The RadICS Platform defensive measures work to limit the effects of these failures and ensures placement into safe states. These added features address the additional CCF vulnerabilities associated with digital technology and add to the defense-in-depth approach provided by the NRC hardware qualification requirements, plant design features for other licensing basis CCF vulnerabilities (e.g., fire flood, extreme weather mitigation), and the existing signal and functional diversity incorporated in the plant PS design/licensing basis.

The diversity of a typical application using the RadICS Platform technology was evaluated using the methodology outlined in NUREG/CR-7007 (Reference 10-8) is presented in Appendix D.

### 10.3.4 Defense-in-Depth

The design principle of defense-in-depth is applied to safety-related I&C systems through the concept of echelons of defense. NUREG/CR-6303 defines four I&C echelons of defense: control system, RTS, ESFAS, and monitoring and indicator system. These four echelons are typically thought of as providing concentric barriers of protection.

The four echelons of defense described above are only conceptual and, except for the monitoring and indication echelon of defense (see Section B.1.4 in BTP 7-19), NRC regulations do not require nor does this guidance imply that RTS and ESFAS echelons of defense must be independent or diverse from each other with respect to a CCF. NRC accepts that the RTS and ESFAS echelons may be combined into a single digital I&C PS platform. However, plant responses to postulated CCF that could impair a safety function must be shown to meet the acceptance criteria defined in BTP 7-19 regardless of the echelons of defense that may be affected. The RadICS Platform diversity strategy is implemented at the Module level and is not dependent on the echelons of defense in the plant I&C architecture.

The RadICS Platform diversity solution is an acceptable regulatory solution for the digital CCF vulnerabilities present in the RadICS Platform. NRC BTP 7-19, Revision 6, states that there are two design attributes, either of which is sufficient to eliminate consideration of software based or software logic based CCF: diversity or testability. With respect to the diversity option, BTP 7-19 specifies that when sufficient diversity exists in the PS, then the potential for CCF within the channels can be considered to be appropriately addressed without further action.

The RadICS Platform can be used employ additional signal and functional diversity strategies. Signal diversity is defined as the use of different sensed parameters to initiate a protective action. Signal diversity is a plant-specific design decision that can be effectively implemented with the range of input module capabilities in the RadICS Platform. Two signal channels are functionally diverse if they perform different physical functions or employ different algorithms. Functional diversity is a plant-specific design decision that can be readily implemented by allocating functionally diverse channels to separate LMs in a RadICS Platform system. These strategies can be used together with the existing signal and functional diversity incorporated in the plant PS design/licensing basis to further increase the overall diversity in the PS. These options do not affect the generic RadICS Platform features (i.e., the hardware, Electronic Design, or communications features described in Chapter 6). Instead, these options only affect certain plant-specific system analysis.





## 10.4 RadICS Diversity Summary

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The RadICS Platform diversity solution is an acceptable regulatory solution for the digital CCF vulnerabilities present in the RadICS Platform. NRC BTP 7-19, Revision 6, states that there are two design attributes, either of which is sufficient to eliminate consideration of software based or software logic based CCF: diversity or testability. With respect to the diversity option, BTP 7-19 specifies that when sufficient diversity exists in the PS, then the potential for CCF within the channels can be considered to be appropriately addressed without further action.

The RadICS Platform diversity strategy represents a stronger diversity case (i.e., more diversity attributes) than others accepted by NRC for systems based on FPGA technology. The FPGA-based Electronic Design and CPLD-based PSWD provide CCF protection for every RadICS Module in a system. The functional diversity strategy employed for RadICS Module Electronic Designs has a greater degree of diversity than strategies that introduce functional diversity into FPGA electronic designs through the use of various degrees of development team diversity.

The RadICS Platform diversity approach provides other benefits by simplifying the overall I&C systems designs, since a separate diverse actuation system is not required to mitigate digital CCFs. The RadICS Platform diversity strategy leads to a simpler overall I&C architecture than other platform-based diverse technology solutions (e.g., addition of a separate diverse actuation system or different equipment configurations in redundant divisions in a system). The RadICS Platform diversity strategy eliminates the complex intersystem design coordination analysis of two actuation systems controlling safety components.

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## **10.5 Chapter 10 References**

- 1 Branch Technical Position 7-19, Revision 6, "Guidance for Evaluation of Diversity and Defense- in-Depth in Digital Computer-based Instrumentation and Control Systems"
- 2 NUREG/CR-6303, "Method for Performing Diversity and Defense-in-Depth Analyses of Reactor Protection Systems"
- 3 IEC 60880:2006, "Nuclear power plants - Instrumentation and control systems important to safety - Software aspects for computer-based systems performing category A functions"
- 4 IEC 61226:2009, "Nuclear power plants - Instrumentation and control important to safety - Classification of instrumentation and control functions"
- 5 John Thomas, Francisco Luiz de Lemos, and Nancy Leveson, Research Report: NRC-HQ-11-6-04-0060, Evaluating the Safety of Digital Instrumentation and Control Systems in Nuclear Power Plants, November 2012.
- 6 National Research Council, "Digital Instrumentation and Control Systems in Nuclear Power Plants: Safety and Reliability Issues, Final Report," Washington, DC, 1997.
- 7 Bishop, P. G., Adelard LLC, "Review of Software Design Diversity," December 1994.
- 8 NUREG/CR-7007, "Diversity Strategies for Nuclear Power Plant Instrumentation and Control Systems."



## 11 Secure Development and Operational Environment

This chapter discusses the RadICS Platform secure development environment, the RadICS Platform vulnerability assessment, and implementation of the secure development and operational environment controls.

RPC Radiy and Radics LLC have implemented a secure development and operational procedure that specifies the security controls for the RadICS Platform development and operational environment. The procedures provide guidance for designing digital systems (both hardware and electronic design) to ensure that they are free from vulnerabilities that could affect the reliability of the system.

The RadICS Platform secure development and operational environment is designed to meet the guidance in RG 1.152 (Reference 11-1) by providing (1) measures and controls taken to establish a secure environment for development of the digital safety system against undocumented, unneeded, and unwanted modifications and (2) protective actions taken against a predictable set of undesirable acts (e.g., inadvertent operator actions or the undesirable behavior of connected systems) that could challenge the integrity, reliability, or functionality of a digital safety system during operations.

### 11.1 Development Environment Vulnerability Assessment

RPC Radiy and Radics LLC conducted vulnerability assessments for the RadICS Platform development environment to identify security vulnerabilities and identify potential security measures to mitigate identified vulnerabilities. Radics LLC used RG 1.152 as basis for this assessment. Radics LLC also used RG 5.71 (Reference 11-2) to understand potential U.S. customer requirements.

The RadICS Platform development environment vulnerability assessment included:

- Analysis of potential hardware vulnerabilities for the development environment
- Analysis of potential electronic design and software-based tool vulnerabilities for the development environment
- Analysis of potential configuration vulnerabilities for the development environment
- Analysis of potential network vulnerabilities for the development environment

The hardware vulnerability analysis of the development environment assessed the following potential vulnerabilities:

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The electronic design and software-based tool vulnerability analysis of the development environment assessed the following potential vulnerabilities:

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The configuration vulnerability analysis of the development environment assessed the following potential vulnerabilities:

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The network vulnerability analysis of the development environment assessed the following potential vulnerabilities:

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A list of possible threats to the development environment was developed. Each potential development environment vulnerability was assessed against the possible threats. Appropriate security measures for each vulnerability and effective means to implement them were identified.

The results of the RadICS Platform development environment vulnerability assessment were documented in a vulnerability assessment report (Reference 11-3).



### ***11.2 RadICS Secure Development Environment***

RPC Radiy and Radics LLC have implemented a comprehensive set of security measures that are designed to eliminate credible vulnerabilities associated with company security management and the digital equipment development process. These security measures include:

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### ***11.3 Operating Environment Vulnerability Assessment***

RPC Radiy and Radics LLC conducted vulnerability assessments for the RadICS Platform operating environment to identify potential security vulnerabilities and identify security measures to mitigate identified vulnerabilities. Radics LLC used RG 1.152 as basis for this assessment. Radics LLC also used RG 5.71 to understand potential U.S. customer requirements.

The RadICS Platform vulnerability analysis assessed the following potential vulnerabilities:

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Each potential operating environment vulnerability for the RadICS Platform was assessed and appropriate security measures for each vulnerability were identified.

The results of the RadICS Platform operating environment vulnerability assessment were document in a vulnerability assessment report.

**11.4 RadICS Platform Secure Operational Environment**

RadICS Platform has a comprehensive set of security measures implemented that are designed to eliminate credible vulnerabilities associated with the integrity, reliability, or functionality of a digital safety system during operations. These security measures include:

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### **11.5 Technology Advantages for FPGAs and CPLDs**

FPGA and CPLD technologies provide additional inherent technology enhancements to a secure development and operational environment. These inherent security measures include:

- There are no known viruses or malware designed to attack HDL coded configurations; FPGA-based platforms have a simple and structured design, therefore the corresponding V&V processes performed at each stage of design are more likely detect the presence of potential threats and malicious design;
- FPGAs do not use operating systems which could be the target of potential cyber attacks
- FPGA programming and reprogramming can be done only through a special interface requiring physical access to the hardware. Additionally, it is impossible to connect common storage media or communication devices that could infect the control logic code.

FPGA-based systems that directly implement the required I&C functions (like the RadICS Platform) do not contain high-level, general-purpose components that can be easily diverted or hijacked for malicious purposes. Malicious functions must be introduced as complete designs, using technology-specific engineering tools. This aspect of FPGA designs raises the level of difficulty a would-be attacker would face in attempting to make malicious modifications.

### **11.6 Project-Specific Vulnerability Assessments**

The Radics LLC Secure Development and Operational Environment Procedure specifies that a project-specific vulnerability assessment be prepared that contain results of vulnerabilities assessment and appropriate phase-specific protective actions and controls. This document is intended for implementation at development environment to cover all the revealed vulnerabilities for the development stages, including:

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The security of electronic records is assured by two main methods:

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The RadICS Platform-based project-specific lifecycle security activities and documentation are shown in Figure 11-1.





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**Figure 11-1: RadICS Project-Specific Lifecycle Security Activities**

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**11.7 Chapter 11 References**

- 1 RG 1.152, Revision 3, "Criteria for Digital Computers in Safety Systems of Nuclear Power Plants," July 2011
- 2 RG 5.71, "Cyber Security Programs for Nuclear Facilities," January 2010
- 3 RPC Radiy Document D2.8, "RadICS Security Analysis Report"



## 12 Compliance Summary for Key Regulations, Codes, and Standards

A summary of the key NRC regulatory requirements and acceptance criteria for I&C systems important to safety identified in Chapter 5 is provided for the RadICS Platform and associated development processes. The discussion is organized into four sections: Quality Assurance, Technical Requirements, Electronic Design Development Processes, and Secure Development and Operating Environment.

### 12.1 Quality Assurance

The quality assurance requirements applicable to the RadICS Platform Topical Report review are found in NRC RG 1.28 (Reference 12-1) and RG 1.152 (Reference 12-2).

#### 12.1.1 Regulatory Guide 1.28

RG 1.28, Revision 4, endorses Part I and Part II requirements included in NQA-1-2008 and the NQA-1a-2009 Addenda (Reference 12-3) as providing an adequate basis for complying with the requirements of 10 CFR Part 50 Appendix B (Reference 12-4). Compliance with 10 CFR Part 50 Appendix B is an accepted method of satisfying 10 CFR Part 50 Appendix A (Reference 12-5) GDC 1.

Chapter 3 describes the Radics LLC QAP. The Radics LLC organization was described and the key organizational responsibilities for quality were identified.

The Radics LLC QAPD is the top-level QA document. It was developed to meet the requirements of NQA-1-2008/ NQA-1a-2009 Addenda. The Radics LLC QAPD is based on NEI 11-04A (Reference 12-6). The Radics LLC QAPD establishes the quality system document structure, which includes the following:

- Radics LLC QAPD is the upper tier quality requirements document
- Radics LLC Quality Procedures implement the QAPD requirements for programs and processes
- Radics LLC Quality Work Instructions provide standardized methods to accomplish quality-related work
- Radics LLC Forms and Records are used to create the implementation evident for quality-related work

All Radics LLC activities for the processes described in the RadICS Topical Report are performed in accordance with the Radics LLC QAP.

A complete set of procedures was developed to implement quality controls for all 18 criteria from 10 CFR Part 50 Appendix B. A comprehensive training program was prepared for Radics LLC personnel on the key elements of the QAPD-001 and implementing procedures. A qualification and training program was implemented for QA lead auditors and inspectors. The Radics LLC staff has been certified on the following topics:

- Internal/External Auditing topics and techniques
- Organization safety culture, root cause determination and problem-solving techniques
- Means to identify and deal with Counterfeit, Fraudulent, and Suspect Items

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- Commercial Grade Item Dedication

GQA completed a third-party evaluation in August 2016 (Reference 12-7). Evaluation QAP\_EVAL-2016 was performed to assess the adequacy of the Radics LLC Quality Assurance Program documents for meeting 10 CFR Part 50 Appendix B, 10 CFR Part 21, ASME NQA-1-1994, NQA-1-2008, and NQA-1a-2009. The evaluation was performed as a document audit of current policies and quality procedures to assess the Radics LLC QAPD for addressing applicable requirements for control over quality activities for supplying nuclear safety-related digital instrumentation and control equipment. The scope of the evaluation included the latest approved revisions of the Radics LLC QAPD, 42 Quality Procedures, and 3 significant Work Instructions.

The evaluation found that the Radics LLC QAPD was a comprehensive network of policies, procedures, instructions, and forms that address the nuclear quality assurance requirements in detail. The Radics LLC QAPD also reflect recent regulatory developments, provisions and guidance of impact to nuclear licensees and their suppliers. GQA concluded that the Radics LLC QAPD is comprehensively documented and compliant with stated requirements. Three evaluation comments were submitted for corrective action in accordance with the Radics LLC QAPD.

The Radics LLC QAPD satisfies the quality assurance requirements of IEEE Std 603-1991 (Reference 12-8) Section 5.3.

### 12.1.2 Regulatory Guide 1.152

NRC RG 1.152, Revision 3, endorses IEEE Std 7-4.3.2-2003 (Reference 12-9) as an acceptable method for satisfying NRC regulations with respect to high functional reliability and design requirements for computers used in the safety systems of nuclear power plants.

IEEE Std 7-4.3.2-2003 Section 5.3 identifies additional requirements that are necessary to satisfy the requirements of IEEE Std 603 for digital systems for the following topics:

- Software development (Section 5.3.1)
- Use of software tools (Section 5.3.2)
- Verification and validation (Sections 5.3.3 and 5.3.4)
- Configuration management (Section 5.3.5)
- Risk Management (Section 5.3.6)
- Qualification of existing commercial computers (Section 5.4.2)

The electronic design development process described in Chapters 7 and 8 satisfy the requirements of IEEE Std 7-4.3.2-2003 Section 5.3.1.

The use of software-based tools described in Chapter 8 satisfies the requirements of IEEE Std 7-4.3.2-2003 Section 5.3.2.

The V&V activities described in Chapters 7 and 8 satisfy the requirements of IEEE Std 7-4.3.2-2003 Section 5.3.3. Compliance with IEEE Std 1012-2004 (Reference 12-10) is discussed in Section 12.3.

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The organizational independence of the organizations performing V&V activities for the RadICS Platform described in Chapter 3 satisfy the requirements of IEEE Std 7-4.3.2-2003 Section 5.3.4.

The electronic design configuration management process described in Chapter 7 satisfies the requirements of IEEE Std 7-4.3.2-2003 Section 5.3.5. Compliance with IEEE Std 828-2005 is discussed in Section 12.3.

The use of the FSMP described in Section 3.2.2.3 satisfies the risk management requirements of IEEE Std 7-4.3.2-2003 Section 5.3.6.

The commercial grade dedication process described in Chapter 4 satisfies the commercial grade dedication process requirements of IEEE Std 7-4.3.2-2003 Section 5.4.2. The RadICS Platform commercial grade dedication process described in Chapter 4 also addresses the review guidance in BTP 7-18 (Reference 12-11).

## **12.2 Technical Requirements**

The technical requirements applicable to the RadICS Platform Topical Report review are found in RG 1.153 (Reference 12-12), RG 1.152, Revision 3, DI&C-ISG-04 (Reference 12-13), and NUREG/CR 6082 (Reference 12-14).

### **12.2.1 Regulatory Guide 1.153**

RG 1.153, Revision 1, endorses IEEE Std 603-1991 as an acceptable method for satisfying NRC regulations with respect to the design, reliability, qualification, and testability of the power, instrumentation, and control portions of the safety systems of nuclear power plants. 10 CFR 50.55a(h)(2) incorporates IEEE Std 603-1991 in the regulation by reference.

IEEE Std 603-1991 has several technical requirements that are addressed by the RadICS Platform design:

- Equipment Qualification (Section 5.4)
- System Integrity (Section 5.5)
- Independence (Section 5.6)
- Capability for Test and Calibration (Section 5.7)
- Control of Access (Section 5.9)
- Repair (Section 5.10)
- Identification (Section 5.11)
- Reliability (Section 5.15)

The RadICS Platform EQ program described in Chapter 9 satisfies the EQ requirements of IEEE Std 603-1991 Section 5.4. The RadICS Platform Equipment Qualification Plan conforms to IEEE Std 323-2003 (Reference 12-15), as endorsed by RG 1.209 (Reference 12-16). The seismic qualification testing is performed in accordance with the IEEE Std 344-2004 (Reference 12-17), as endorsed by RG 1.100 (Reference 12-18), using the generic seismic spectra documented in EPRI TR-107330 (EPRI website version) (Reference 12-19). The electromagnetic compatibility testing is performed in accordance with testing standards endorsed by RG 1.180 (Reference 12-20). The licensee for a project-specific

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application of the RadICS Platform will address the correspondence of the generic qualification envelope for the RadICS Platform with the site-specific qualification bounding envelopes.

The RadICS Platform predictability and repeatability design features described in Sections 6.3, 6.4, 6.8, and 6.10 satisfy the system integrity requirements of IEEE Std 603-1991 Section 5.5.

The RadICS Platform independence features described in Section 6.6 satisfy the independence requirements of IEEE Std 603-1991 Section 5.6 for the RadICS Platform equipment. The RadICS Platform isolation features also satisfy IEEE Std 384-1992 (Reference 12-21), as endorsed by RG 1.75 (Reference 12-22). The electrical fast transient testing, surge withstand testing, and Class 1E to non-Class 1E isolation testing in the RadICS EQ program described in Chapter 9 address the review guidance in BTP 7-11 (Reference 12-23).

The RadICS Platform design features described in Sections 6.7, 6.11, and 6.12 provide the capability for test and calibration, which satisfy the test and calibration requirements of IEEE Std 603-1991 Section 5.7. The specific means for complying with the system level test and calibration requirements must be assessed on a project-specific basis.

The RadICS Platform control of access features described in Section 6.9 satisfy the control of access requirements of IEEE Std 603-1991 Section 5.9. Additional means for complying with the system level control of access requirements must be assessed on a project-specific basis.

The RadICS Platform design features described in Sections 6.1.3, 6.4 and 6.7 along with the design considerations summarized in Section 7.6.3 facilitate timely recognition, location, replacement, repair, and adjustment of malfunctioning equipment, which satisfy the repair requirements of IEEE Std 603-1991 Section 5.10.

The RadICS Platform Human-Machine Interface features described in Section 6.2.1.6 satisfy the identification requirements of IEEE Std 603-1991 Section 5.11. Additional means for complying with the system level identification requirements must be assessed on a project-specific basis.

The RadICS Platform FMEDA described in Section 9.2.1 satisfy the reliability requirements of IEEE Std 603-1991 Section 5.15.

## **12.2.2 Regulatory Guide 1.152**

NRC RG 1.152, Revision 3, endorses IEEE Std 7-4.3.2-2003 as an acceptable method for satisfying NRC regulations with respect to high functional reliability and design requirements for computers used in the safety systems of nuclear power plants.

IEEE Std 7-4.3.2-2003 has several technical requirements that are addressed by the RadICS Platform design:

- Computer system testing (Section 5.4.1)
- System integrity (Sections 5.5.1, 5.5.2, and 5.5.3)
- Independence (Section 5.6)
- Identification (Section 5.11)

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- Reliability (Section 5.15)

The RadICS Platform EQ program described in Chapter 9 specifies the performance of operability and prudency tests, as defined in EPRI TR-107330. In RG 1.209, NRC noted that it has accepted EPRI TR-107330 as an acceptable method for addressing mild-environment qualification of digital platforms. The RadICS Platform EQ program satisfies the computer system testing requirements in IEEE Std 7-4.3.2-2003 Section 5.4.1.

The RadICS Platform predictability and repeatability design features described in Sections 6.3, 6.4, 6.8, and 6.10 satisfy the design for computer integrity requirements in IEEE Std 7-4.3.2-2003 Section 5.5.1. The RadICS Platform diagnostic features described in Section 6.4 were developed in accordance with the ED development process described in Chapters 7 and 8. The RadICS Module EDs were subject to the V&V process described in Section 7.4 and the configuration management process described in Section 7.5. The controls for the development of the RadICS Platform diagnostic features satisfy the design for test and calibration requirements in IEEE Std 7-4.3.2-2003 Section 5.5.2. The RadICS Platform diagnostic features described in Section 6.4 satisfy the fault detection and self-diagnostics requirements in IEEE Std 7-4.3.2-2003 Section 5.5.3. The RadICS Platform diagnostic features described in Chapter 6.4 address the review guidance in BTP 7-17. The use of these automatic test features as credit for performing Technical Specification surveillance test functions must be assessed on a project-specific basis. The RadICS Platform timing diagrams and Working Cycles described in Section 6.10 addresses the BTP 7-21 (Reference 12-24) review guidance regarding allocation of system timing requirements to the digital computer portion of the system. The system level aspects of system timing must be assessed on a project-specific basis.

The RadICS Platform communication features described in Sections 6.3, 6.4, and 6.6 satisfy the system independence requirements of IEEE Std 7-4.3.2-2003 Section 5.6.

The RadICS Module version authentication features of the RadICS Platform described in Section 6.1.3 satisfy the identification requirements of IEEE Std 7-4.3.2-2003 Section 5.11.

The RadICS Platform FMEDA described in Section 9.2.1 satisfies the reliability requirements of IEEE Std 7-4.3.2-2003 Section 5.15.

### **12.2.3 DI&C-ISG-04**

The generic RadICS Platform communication independence features comply with the DI&C-ISG-04 guidance regarding inter-divisional communication. The generic RadICS Platform does not include priority logic for command prioritization. The generic RadICS Platform design supports multi-divisional communication only in divisional voting logic and divisional display processors as described in Chapter 6. The details of the alignment of the RadICS Platform capabilities with the criteria in DI&C-ISG-04 are presented in Appendix B.

### **12.2.4 NUREG/CR 6082**

Section 2 of NUREG/CR-6082, Data Communications, has 15 questions intended to help focus reviews of data communication systems. Table 12-1 provides an evaluation the RadICS Platform for those questions.

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**Table 12-1: Responses to NUREG/CR-6082 Communications System Questions**

NUREG/CR-6082 Question	RadICS Platform
2.1.1. Is it an event-based or state based system?	The RadICS Platform is a state-based system that operates in a deterministic way, as described in Sections 6.3, 6.4, and 6.10. The communication between the RadICS Platform Chassis is asynchronous.
2.1.2. Is there an accurate picture of the layout?	The detailed architectures of the RadICS Modules and the connection of each Unit are known, as described in Section 6.2.4.
2.1.3. Are the data rates known between all nodes of the architecture? Are they known for upset and error conditions?	The data rates between all nodes of the architecture are based on the Work Cycle time. This Work Cycle time is constant, as described in Section 6.10. The Work Cycle time is fixed and based on the definition of the data sent on the network during the design phase. The consistency of data transmission is verified, as described in Sections 6.4 and 6.8.
2.1.4. Is the message mix known? Is it known for upset and error conditions?	The messages mix is well-characterized and the data are carried in defined protocols, as described in Section 6.3.3.
2.1.5. Are the timing and delay requirements known?	Timing and delay requirements are expressed in detailed system requirements. The response time of the RadICS Platform system is defined by a theoretical model (as described in Section 6.10) and verified on the equipment during factory tests.
2.1.6. Is the system "deterministic" and the effects of error recovery accounted for?	The protocol is deterministic. Even in case of errors, the Work Cycle time is constant, as described in Section 6.10. If there is any error, they are detected by the communication error detection features described in Section 6.4. Section 6.3 describes the response of the RadICS Platform to communication errors.
2.1.7. Is the actual link capacity including interface, operating system, and protocol performance effects being quoted, or is the vendor basing calculations on raw media bandwidth?	The Work Cycle time includes the timing of reception and transmission processing (described in Section 6.10) and is used to determine the actual link capacity.
2.1.8. What are the media requirements?	The media (cable and fiber optic) are defined in Section 6.3.1. The use of these media is tested for electromagnetic compatibility, as described in Section 9.1.2.5.





NUREG/CR-6082 Question	RadICS Platform
2.1.9. Does the design meet independence requirements?	The RadICS Platform independence features are described in Section 6.6.
2.1.10. What are the communications error performance requirements?	The RadICS Platform communication error detection features are described in Section 6.4.
2.1.11. What are the protocol requirements? What services should the protocol provide?	The media are off-the-shelf product. The RadICS Platform communication protocols are proprietary and developed by RPC Radiy, as described in Section 6.3.3.
2.1.12. Is there theoretical support for performance and reliability?	For performance, the cycle time of each Chassis is fixed and monitored, as described in Section 6.10. For reliability, the FMEDA described in Section 9.2.1 included an evaluation of the communication protocols.
2.1.13. Is there experimental support for performance and reliability?	Detection of failed components is supported by system self-tests. Then repair is limited to replacement of RadICS Modules and the cabling is facilitated by use of connectors. Restoration of RadICS Platform operation after identification of any failure of an electronic component is simple and not time consuming.
2.1.14. Is there an installed base? If proprietary, how many suppliers support the medium and the protocol software?	The RadICS Platform is already installed in many NPPs, as discussed in Chapter 2. The communication protocols are provided by RadICS Platform proprietary EDs.
2.1.15. Is there a good match between nodes processors, networks controllers, and operating system and protocol stack?	The RadICS Platform is already installed in safety systems of NPPs. This long-term installation and operation allows us to claim that there is a good match between all elements of the RadICS Platform.

### 12.2.5 Branch Technical Position 7-19

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The RadICS Platform diversity solution is an acceptable regulatory solution for the digital CCF vulnerabilities present in the RadICS Platform. NRC BTP 7-19, Revision 6, states that there are two design attributes, either of which is sufficient to eliminate consideration of software based or software logic based CCF: diversity or testability. With respect to the diversity option, BTP 7-19 specifies that when sufficient diversity exists in the PS, then the potential for CCF within the channels can be considered to be appropriately addressed without further action. The evaluation of diversity in Appendix D demonstrates that sufficient diversity is incorporated into the RadICS Platform design.

### **12.3 Electronic Design Development Processes**

The software development requirements applicable to the electronic design development for the RadICS Platform Topical Report review are found in RGs 1.173 (Reference 12-25), 1.172 (Reference 12-26), 1.171 (Reference 12-27), 1.170 (Reference 12-28), 1.169 (Reference 12-29), and 1.168 (Reference 12-30). Additional review guidance is found in BTP 7-14 (Reference 12-31).

#### **12.3.1 Regulatory Guide 1.173**

RG 1.173, Revision 1, endorses IEEE Std 1074-2006 (Reference 12-32). IEEE Std 1074-2006 provides a structured approach for developing a software life cycle program consistent with this regulatory guidance. The life cycle processes for the RadICS Platform and Application ED were established according to the guidance provided in IEC 60880:2006 (Reference 12-33) and IEC 60508:2010 (Reference 12-34) and was documented in dedicated development plans, which are described in Chapters 7 and 8. The RadICS Module ED life cycle process described in Chapter 8 was established according to the guidance provided in IEC 62566:2011 (Reference 12-35). The RadICS Platform and Application ED lifecycles conform to IEEE Std 1074-2006, as endorsed by RG 1.173, Revision 1.

#### **12.3.2 Regulatory Guide 1.172**

RG 1.172, Revision 1, endorses IEEE Std 830-1998 (Reference 12-36). IEEE Std 830-1998 is a recommended practice for writing software requirements specifications; however, as a recommend practice, it does not identify any specific requirements. The RadICS Platform requirements documents described in Section 7.3.2 follow the recommendations in IEEE Std 830-1998, as endorsed by RG 1.172, Revision 1, with two exceptions. The RadICS Platform and Application ED requirements documents follow the format requirements of the respective quality assurance programs rather than the recommendation provided in IEEE Std 830-1998 Section 5. The RadICS Platform requirements are not ranked for importance, as recommended by IEEE Std 830-1998 Section 4.3.5. RG 1.172, Revision 1, does not support the ranking approach recommended by IEEE Std 830-1998.

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### **12.3.3 Regulatory Guide 1.171**

This RG endorses IEEE Std 1008-1987 (Reference 12-37). IEEE Std 1008-1987 describes a structured approach for performing software unit testing. The Function Block Library testing described in Chapters 7 and 8 represent unit level testing for the RadICS Platform. The Function Block Library testing conforms to IEEE Std 1008-1987, as endorsed by RG 1.171, Revision 1.

### **12.3.4 Regulatory Guide 1.170**

This RG endorses IEEE Std 829-2008 (Reference 12-38). IEEE Std 829-2008 provides a structured approach to software test documentation. Section 7.4.5.2 describes the RPC Radiy and Radics LLC approach to Platform and Application ED V&V test documentation. The test documents have been structured to reflect the use of RadICS Platform and Application ED development lifecycle, the use of FPGA technology, and conformance to respective quality assurance programs for document format. These adaptations are consistent with the provision identified in IEEE Std 829-2008 Section 6 and RG 1.170 Regulatory Position C.1. Radics LLC believes that the RadICS Platform test documentation conforms to the technical requirements of IEEE Std 829-2008 but not necessarily all the administrative requirements.

### **12.3.5 Regulatory Guide 1.169**

This RG endorses IEEE Std 828-2005 (Reference 12-39). IEEE Std 828-2005 describes a structured approach to software configuration management. The RPC Radiy and Radics LLC approach to electronic design and software-based tool configuration management is described in Section 7.5. The RadICS Platform and Application ED configuration management programs conform to the requirements in IEEE Std 828-2005, as endorsed by RG 1.169, Revision 1, with one exception. The RadICS Platform and Application ED lifecycles do not include interfaces with external organizations that design software or electronic design for a project. As such, the interface controls specified in IEEE Std 828-2005 Section 3.3.5 are not implemented. The design interfaces internal to Radics LLC are controlled within the design control process.

### **12.3.6 Regulatory Guide 1.168**

This RG endorses IEEE Std 1012-2004. IEEE Std 1012-2004 describes a structured approach to software V&V. The RPC Radiy and Radics LLC approach to electronic design V&V is described in Chapters 7 and 8. The RadICS Platform and Application ED V&V programs activities and tasks have been adapted to reflect the use of RadICS Platform development lifecycle and the use of FPGA technology, as allowed by IEEE Std 1012-2004 Section 1.7. The RadICS Platform and Application V&V programs conform to the requirements in IEEE Std 1012-2004, as endorsed by RG 1.168, Revision 2, with five exceptions. The specific administrative requirements for administrative and formatting requirements specified in IEEE Std 1012-2004 Sections 7 and 8 are not followed. Instead, the V&V documents conform to established design practices and quality assurance program requirements. The criticality analysis is not performed, since all RadICS Module EDs are classified at the highest level for use in safety-related systems. The FMEDA described in Section 9.2.1 and the IEC Safety Integrity Level certification described in Section 4.1.2.3 replace the hazards analyses specified in IEEE Std 1012-2004 Section 5 and Tables 1 and 2. The

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security assessments described in Chapter 11 replace the security analyses specified in IEEE Std 1012-2004 Section 5 and Tables 1 and 2. The RPC Radiy and Radics LLC approach to V&V test documentation described in Section 12.3.4 is used as an alternative to the test documentation requirements specified in IEEE Std 1012-2004 Section 6.3.1.

RG 1.168 also endorses IEEE Std 1028-2008 (Reference 12-40). IEEE Std 1028-2008 describes methods to perform software reviews and audits. The RPC Radiy and Radics LLC approach to electronic design reviews is described in Section 7.4.3. The RPC Radiy and Radics LLC approach to electronic design audits is described in Sections 7.3.1, 7.5.3.3, and 11.4. RPC Radiy and Radics LLC perform the audits and documents the results in accordance with established practices and quality assurance program requirements instead of the methods specified in IEEE Std 1028-2008.

### **12.3.7 Branch Technical Position 7-14**

BTP 7-14, Revision 5, provide a structured approach for developing software using a series of planning documents. The RadICS Platform EDs were developed according to the guidance provided in IEC 60880:2006 and IEC 61508:2010. The IEC SIL certification process requires that products developed under a FSMP. The FSMP is the main planning document and takes all IEC 61508:2010 requirements into consideration and mandates how they are applied throughout the product life cycle. The FSMP covers the same scope as five BTP 7-14 plans: Software Management Plan, Software Development Plan, Software Quality Assurance Plan, Software Integration Plan, and Software Safety Plan. The comparable RadICS Platform documents are mapped to the BTP 7-14 planning scheme in Figure 12-1. The RadICS Platform Document D11.1, *Product Safety Manual*, is closely related to the Application Guide Documentation discussed in EPRI TR-107330.

The figure also shows the mapping of the RadICS Application ED development documents to the BTP 7-14 topics. The RadICS Software Quality Assurance Plan is the main planning document and covers the same scope as seven BTP 7-14 plans: Software Management Plan, Software Development Plan, Software Quality Assurance Plan, Software Integration Plan, Software V&V Plan, Software Configuration Management Plan, and Software Safety Plan. The RadICS Product Safety Manual covers the same scope as three BTP 7-14 plans: Software Installation Plan, Software Maintenance Plan, and Software Operations Plan.

## **12.4 Secure Development and Operating Environment**

The secure development and operating environment guidance applicable to the RadICS Platform Topical Report review are found in RG 1.152, Revision 3.

### **12.4.1 Regulatory Guide 1.152**

The RadICS Platform secure development and operating environment assessment provided in Chapter 11 satisfies the requirements of RG 1.152, Revision 3, Regulatory Position C.2.

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**Figure 12-1: Mapping RadICS Documents to BTP 7-14**

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## 12.5 Chapter 12 References

- 1 Regulatory Guide 1.28, Revision 4, "Quality Assurance Program Criteria (Design and Construction)"
- 2 Regulatory Guide 1.152, Revision 3, "Criteria for Use of Computers in Safety Systems of Nuclear Power Plants"
- 3 ASME NQA-1-2008, "Quality Assurance Program Requirements for Nuclear Facilities"
- 4 10 CFR Part 50 Appendix B, "Quality Assurances Requirements for Nuclear Power Plants and Fuel Reprocessing Plants"
- 5 10 CFR Part 50 Appendix A, "General Design Criteria (GDCs)"
- 6 Nuclear Energy Institute Letter to NRC dated June 6, 2013, "Issuance of NEI 11-04A, Revision 0, Nuclear Generation Quality Assurance Program Description"
- 7 Global Quality Assurance letter to Radics LLC dated August 26, 2016, "Evaluation of the Radics LLC Quality Assurance Program Description"
- 8 IEEE Std 603-1991, "Criteria for Safety Systems for Nuclear Power Generating Stations"
- 9 IEEE Std 7-4.3.2-2003, "Standard Criteria for Digital Computers in Safety Systems of Nuclear Power Generating Stations"
- 10 IEEE Std 1012-2004, "IEEE Standard for Software Verification and Validation Plans"
- 11 BTP 7-18, Revision 5, "Guidance on the Use of Programmable Logic Controllers in Digital Computer-Based Instrumentation and Control Systems"
- 12 Regulatory Guide 1.153, Revision 1, "Criteria for Safety Systems"
- 13 DI&C-ISG-04, Revision 1, "Highly Integrated Control Rooms - Digital Communication Systems"
- 14 NUREG/CR 6082, "Data Communications," August 1993
- 15 IEEE Std 323-2003, "IEEE Standard for Qualifying Class 1E Equipment for Nuclear Power Generating Stations"
- 16 Regulatory Guide 1.209, March 2007, "Guidelines for Environmental Qualification of Safety-Related Computer-Based Instrumentation and Control Systems in Nuclear Power Plants"
- 17 IEEE Std 344-2004, "IEEE Recommended Practice for Seismic Qualification of Class 1E Equipment for Nuclear Power Generating Stations"
- 18 Regulatory Guide 1.100, Revision 3, "Seismic Qualification of Electric and Mechanical Equipment for Nuclear Power Plants"
- 19 EPRI TR-107330, "Generic Requirements Specification for Qualifying a Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants," December 1996
- 20 Regulatory Guide 1.180, Revision 1, "Guidelines for Evaluating Electromagnetic and Radio-Frequency Interference in Safety-Related Instrumentation and Control Systems"
- 21 IEEE Std 384-1992, "Standard Criteria for Independence of Class 1E Equipment and Circuits"
- 22 Regulatory Guide 1.75, Revision 3, "Criteria for Independence of Electrical Safety Systems"
- 23 BTP 7-11, Revision 5, "Guidance on Application and Qualification of Isolation Devices"
- 24 BTP 7-21, Revision 5, "Guidance on Digital Computer Real-Time Performance"
- 25 Regulatory Guide 1.173, Revision 1, "Developing Software Life Cycle Processes for Digital Computer Software Used in Safety Systems of Nuclear Power Plants"
- 26 Regulatory Guide 1.172, Revision 1, "Software Requirements Specifications for Digital Computer Software Used in Safety Systems of Nuclear Power Plants"

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- 27 Regulatory Guide 1.171, Revision 1, "Software Unit Testing for Digital Computer Software Used in Safety Systems of Nuclear Power Plants"
- 28 Regulatory Guide 1.170, Revision 1, "Software Test Documentation for Digital Computer Software Used in Safety Systems of Nuclear Power Plants"
- 29 Regulatory Guide 1.169, Revision 1, "Configuration Management Plans for Digital Computer Software Used in Safety Systems of Nuclear Power Plants"
- 30 Regulatory Guide 1.168, Revision 2, "Verification, Validation, Reviews and Audits for Digital Computer Software Used in Safety Systems of Nuclear Power Plants"
- 31 BTP 7-14, Revision 5, "Guidance on Software Reviews for Digital Computer-Based Instrumentation and Control Systems"
- 32 IEEE Std 1074-2006, "IEEE Standard for Developing Software Life Cycle Processes"
- 33 IEC 60880:2006, "Nuclear Power Plants – Instrumentation and Control Systems Important to Safety – Software Aspects for Computer-Based Systems Performing Category A Functions"
- 34 IEC 61508:2010, "Functional Safety of Electrical/Electronic/Programmable Electronic Safety-related Systems"
- 35 IEC 62566:2011, "Nuclear Power Plants – Instruments and Control Important to Safety – Development of HDL-Programmed Integrated Circuits for Systems Performing Category A Functions"
- 36 IEEE Std 830-1998, "IEEE Recommended Practice for Software Requirements Specifications"
- 37 IEEE Std 1008-1987, "IEEE Standard for Software Unit Testing"
- 38 IEEE Std 829-2008, "IEEE Standard for Software Test Documentation"
- 39 IEEE Std 828-2005, "IEEE Standard for Software Configuration Management Plans"
- 40 IEEE Std 1028-2008, "IEEE Standard for Software Reviews and Audits"



**Appendix A: RadICS Platform Application Guide**

The RadICS Platform Application Guide provides a summary of the guidance for applying the RadICS Platform in NPP I&C systems classified as safety-related. The application guidance is documented in the RadICS Platform Product Safety Manual (Reference A-1), which meets the intent of the application guide documentation described in EPRI TR-107330 (Reference A-2). The qualified RadICS Platform equipment is documented in the Master Configuration List (Reference A-3).

**A.1 RadICS Platform Capabilities**

**A.1.1 RadICS Platform Modes of Operation**

The RadICS Platform has seven modes of operation. Five modes are associated with routine operation of the RadICS Platform. Two other modes are infrequent activities associated with changing parameters used by the Application Logic, calibrating the analog I/O channels, or changing a RadICS Module Electronic Design configuration.

**A.1.1.1 Routine Modes of Operation**

Figure A-1 provides an illustration of the evolution over time of the RadICS Platform, from initial startup through infrequent failures and maintenance and return to full operation. It is representative of the modes of operation that will be seen during routine system operation.

[[

]]<sup>a,c,e</sup>

**Figure A-1: Illustrative Timeline of RadICS Platform Operating Modes**

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- POWERED-OFF mode

The RadICS Platform is in the POWERED OFF mode when both 24 VDC supplies are removed. In the POWERED-OFF mode, all RadICS Platform outputs are in their safe state. The RadICS Platform will restart only if all power is removed and then the RadICS Platform is powered up by either one or both 24 VDC power sources. [[

]]<sup>a,c,e</sup>

- Power-up → STARTUP mode

When the RadICS Platform is powered up, there is a [[ ]]<sup>a,c,e</sup> second period of operation in STARTUP mode during which all outputs are held in the safe state<sup>12</sup> and the RadICS Platform performs all standard self-diagnostic tests plus some extra tests. At the end of STARTUP mode, all Application Logic is initialized, and ready to implement the Application ED.

- STARTUP mode → RUN (SAFE) mode with SOR Set

At the end of a successful STARTUP mode period (i.e., no safety-critical failures were detected), the RadICS Platform will allow the SOR to be reset. Until the SOR is reset, the RadICS Platform operates in RUN (SAFE) mode.

In RUN (SAFE) mode, the Application ED executes normally, setting the internal values of the outputs; however, all outputs are subjected to the SOR, which sets the final outputs to the safe state. (Note: Input Modules skip the RUN (SAFE) mode because they are not equipped with the SOR. They transition directly from STARTUP to RUN mode.)

- RUN (SAFE) → RUN mode with SOR Reset

Transition out of RUN (SAFE) mode into RUN mode occurs when the Reset-SOR input is closed and all conditions that set the SOR have cleared. There are two options to implement this feature:

- 1) Manual reset by the operator [[ ]]<sup>a,c,e</sup>
- 2) Installed wiring that holds the reset circuit closed, thus providing an automatic transition from STARTUP mode, momentarily to RUN (SAFE) mode, and then within [[ ]]<sup>a,c,e</sup> milliseconds to RUN mode.

Once the SOR is reset by the operator [[ ]]<sup>a,c,e</sup>, the RadICS Platform transitions to RUN mode and all outputs are under control of the Application Logic.

<sup>12</sup> [[

]]<sup>a,c,e</sup>

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- FAULTED mode

Each RadICS Module transitions to FAULTED mode from any other mode if the RadICS Platform detects any failure that could possibly render FPGA logic unable to correctly implement the intended safety function (e.g., [[

]]<sup>a,c,e</sup> In FAULTED mode, all outputs of the Module are set to the safe state. [[

]]<sup>a,c,e</sup> display and the FAULTED mode LED will be switched on. Operator intervention is required to restore normal operation by replacing the failed Module and resetting SOR.

The LM may also be forced into FAULTED mode by the Application Logic. In this case the LM will command all output Modules to go to the safe state. If the Application Logic forced the LM into FAULTED mode, [[

]]<sup>a,c,e</sup>

**A.1.1.2 Infrequent Modes of Operation**

The TUNING mode is used to change parameters used by the Application Logic. The CONFIGURATION Mode is used for calibrating the analog I/O channels or changing a RadICS Module ED configuration.

- TUNING Mode

In this mode, parameters defined during the development of the Application Logic design can be adjusted by connecting a MATS Tuning PC with special software to the RadICS Platform. [[

]]<sup>a,c,e</sup>

- CONFIGURATION mode

CONFIGURATION mode is used in a DLS, which is a separate RadICS Chassis that is not connected to the field, for the following maintenance operations:

1) [[

]]<sup>a,c,e</sup>



## A.1.2 Response to Platform Failures

At some random point in time, a failure of a RadICS Module may occur.

- I/O Failures

A failure of a complete I/O input Module (AIM, WAIM, TIM, RIM, or DIM) or an I/O channel on an input Module may occur. If this happens, it is reported to the Application Logic, which makes the decision on managing this failure.

A failure of an I/O channel on an output Module (i.e., DOM or AOM) may occur. When such a failure is detected by the DOM or AOM, it is reported to the Application ED. The Application Logic should be designed to command the opening of the specific digital or analog output.

When the digital or analog output channel failure is reported to the Application ED, the Application Logic may then force the complete DOM or AOM (or all DOMs and AOMs) into RUN (SAFE) mode (which opens all digital or analog output channels by two mechanisms) or FAULTED mode.

- LM Failures

A failure of a LM may occur. The LM is driven to FAULTED mode and drives all other output Modules to the Safe State via two mechanisms (every digital output channel is driven open, every analog output channel is driven to the safe conditions, and the SOR is set).

When the failed LM Module is replaced, and the LM starts up and when it can enter RUN mode, it re-activates the output Modules allowing them to return to RUN mode, and normal RadICS Platform operation resumes.

- FAULTED mode

Each RadICS Module transitions to FAULTED mode from any other mode if the Platform ED detects any failure which could possibly render FPGA logic unable to correctly implement the intended safety function (e.g., power supply out of tolerance, clock failure, CRC check error).

In FAULTED mode, all outputs of the module are set to the safe state. A failed module will indicate an error code on the 4-character display and the FAULTED mode LED will be switched on (except for a total power failure). Operator intervention is required to restore normal operation by replacing the failed module and resetting SOR.

If any I/O module goes into FAULTED mode, LM will replace all data from that module (I/O values, validities, diagnostic data etc.) with zero values and send it to MATS. However, if LM goes into FAULTED mode, it will stop sending any data to MATS after 10 milliseconds. This time is needed to ensure that MATS got the latest data including critical faults.



### A.1.3 User Designed Response to Platform Failures

The RadICS Platform will not go into a fail-safe mode automatically upon detection of the following failures and, therefore, the Application Logic must implement the desired action for these events:

- 1) Any failure of a field input signal,
- 2) Any failure of an individual I/O channel on a module,
- 3) Any complete failure of a module,
- 4) Any failure in a remote RadICS Chassis which has switched to the RUN (SAFE) mode and that communicates with the local chassis under consideration (the resulting stale data from such a remote chassis must be detected by Application Logic in the local chassis), and
- 5) EEPROM failure after STARTUP (Note: These EEPROMs are used only at power-up, so a detected failure occurring during operation is an early warning that the next power-up will not succeed).

The Application Logic can be designed to detect these failures by:

- 1) Setting the safe state by setting the SOR via the SETSOR function block,
- 2) Driving appropriate DOs or AOs to the safe state, or
- 3) Simply setting a DO or AO to signal an alarm.

### A.1.4 Local Indications of RadICS Platform Modes and Status

Each RadICS Module of has two LEDs on the front (RUN and FAULT) as well as a 4-character digital display. The LEDs are the major status indicators, as shown below:

FAULT LED	Off	No failure (or power failure)
	Flashing	(Occurs normally during startup) Non-critical failure when the RadICS Platform is not in startup sequence
	On	Type I fault
RUN LED	On	Normal Operation
	Flashing	While Module is in CONFIGURATION mode
	Off	(Occurs normally during startup) Type I fault (or power failure)

In the absence of failures, the 4-character display indicates the operating mode as follows:

STARTUP	RUN (SAFE)	RUN	CONFIGURATION
STUP	RUNS	RUN	CFG



If a failure occurs the 4-character display shows an error code, and maintenance will generally be required. The RadICS Product Safety Manual contains a listing of all the faults codes.

## A.2 System Design Guidance

### A.2.1 RadICS Chassis Configuration

The qualified RadICS Chassis configuration consists of one LM, located in slot F1 (left end from front side). Slot F2 (right end from front side) is not used. The 14 central module slots may be empty or used for any combination of I/O Modules. The backplane provides separate and dedicated communications lines between slot F1 and every optional module slot (i.e., 14 separate dedicated communications lines).

The qualified RadICS Chassis supports the use of IOPMs for EMI/RFI protection. The IOPMs are mounted within the chassis at the rear directly behind their respective I/O Modules. The IOPMs are specific to the type of I/O Module they protect. This means that changing the use of a slot from one type of Module to another requires relocating the IOPMs.

### A.2.2 Power Supplies

The entire RadICS Chassis is supplied with one or two +24 VDC power supplies which are mounted externally to the RadICS Chassis. The two power sources are independently supplied to every module slot, and every module has its own galvanically isolated power supply sub-module which uses both supply lines.

The power supply requirements are two separate feeds, each meeting the following requirements:

Nominal:	24 VDC
Operating Limits:	[[     ]] <sup>a,c,e</sup> VDC to [[     ]] <sup>a,c,e</sup> VDC
Capacity:	Calculated based on rack configuration

The nominal maximum load for the RadICS Chassis depends on the numbers of modules of each type and should be calculated by the end user. The end user should then allow a suitable margin in power supply capacity. The nominal maximum loads for each Module type are:

Module	Consumption (A)
LM	0.92
AIM	0.85
DOM	0.63
DIM	0.77
AOM	1.42
OCM	0.5
RIM	0.29



Module	Consumption (A)
TIM	0.4
WAIM	1.01

Note: Nominal power consumption can deviate by  $\pm 0.15$  A depending on Module load and operating mode.

### A.2.3 Environmental Conditions

The RadICS Platform should be stored and shipped, and operated within the environmental conditions indicated below:

Operating Temperature	0 – 50 °C (cabinet temperature)
Operating Temperature	0 – 70 °C <b>[[</b> <b>]]<sup>a,c,e</sup></b>
Storage Temperature	-40 – +65 °C
Operating Humidity	Up to 90% (50 °C), Relative Humidity (non-condensing)
Storage Humidity	Up to 30 - 60% (20 $\pm$ 10 °C), Relative Humidity (non-condensing)

**[[** **]]<sup>a,c,e</sup>**

Operating temperature of the RadICS Modules must be monitored because the failure rates do vary as a function of temperature. Temperature monitoring is used to ensure the RadICS Platform is operating within the qualified envelope. The Application Logic must be configured for monitoring of the surface temperature of the RadICS Modules to alarm or go to the safe state, as specified by the end user requirements.

### A.2.4 Inputs and Outputs

The RadICS Modules have the following I/O capacities:

LM	Discrete inputs: 3 Channels (Channel 1 is reserved) Discrete outputs: 6 Channels Fiber Optic: 3 Channels LAN: 3 Channels
AIM	32 channels
WAIM	32 channels
TIM	32 channels
RIM	8 channels
DIM	32 channels



DOM	32 channels
AOM	32 channels
OCM	5 fiber optic channels and 5 RS-232/485 channels

Single chassis I/O capacity can be extended using OCMs to connect three chassis in series. The limit of three is Radics LLC recommendation, not a hard functional limitation. The end user can build a configuration with four or five chassis in series, provided that the time response and reliability are adequate for the application.

#### A.2.4.1 Discrete Inputs

The discrete inputs are dry contacts (24 VDC supplied by each discrete input channel). The contact properties are:

- sensed open: Impedance > 20 k $\Omega$  (provides < 2 mA (milliamp))
- sensed closed (low level): Impedance < 10.8 k $\Omega$  (provides  $\geq$  2 mA)
- sensed closed (high level): Impedance < 2.7 k $\Omega$  (provides  $\geq$  5 mA);

Maximum current: 10 mA per channel

[[

]]<sup>a,c,e</sup>

Circuit Current	Interpreted Short-Circuit	Interpreted Field State
[[		
		]] <sup>a,c,e</sup>

#### A.2.4.2 Discrete Outputs

The discrete outputs are field effect transistor driven (Form A) with a voltage and current rating of 48 VAC/VDC and 200 mA.

#### A.2.4.3 Analog Inputs

The analog inputs have the following characteristics:

- Hardware range: 0 – 5.1 VDC
- Signal range: 0 – 5.0 VDC (0 – 20 mA using a precision 250  $\Omega$  resistor)
- Common mode rejection: 86 dB

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- Input impedance (when powered on or off): 1 M $\Omega$
- Diagnostic Discrepancy Threshold: 2% of full scale. [[

]]<sup>a,c,e</sup>

#### **A.2.4.4 Wide Range Analog Inputs**

The wide range analog inputs have the following characteristics:

- Hardware range: -11 – +11 VDC
- Signal range: -10.9 – +10.9 VDC
- Common mode rejection: 86 dB
- Input impedance (when powered on or off) 1 M $\Omega$
- Diagnostic Discrepancy Threshold: 2% of full scale. [[

]]<sup>a,c,e</sup>

#### **A.2.4.5 Thermocouple Inputs**

The thermocouple inputs have the following characteristics:

- Type B thermocouple signal range: 255 – 1820 °C (0.291 – 13.820 mV)
- Type E thermocouple signal range: -200 – 1000 °C (-8.825 – 76.373 mV)
- Type J thermocouple signal range: -205 – 1195 °C (-7.996 – 69.267 mV)
- Type K thermocouple signal range: -195 – 1367 °C (-5.813 – 54.717 mV)
- Type N thermocouple signal range: -195 – 1295 °C (-3.939 – 47.333 mV)
- Type R thermocouple signal range: -45 – 1763 °C (-0.208 – 21.040 mV)
- Type S thermocouple signal range: -45 – 1763 °C (-0.215 – 18.641 mV)
- Type T thermocouple signal range: -195 – 395 °C (-5.523 – 20.563 mV)
- Diagnostic Discrepancy Threshold: 2% of full scale. [[

]]<sup>a,c,e</sup>

#### **A.2.4.6 RTD Inputs**

The RTD inputs have the following characteristics:

- Platinum ( $\alpha=0.00385$  per °C) – corresponds to IEC 751
- Platinum ( $\alpha=0.00391$  per °C)
- Copper ( $\alpha=0.00428$  per °C)
- Copper ( $\alpha=0.00426$  per °C)
- Nickel ( $\alpha=0.00617$  per °C)
- Hardware range: 0-1600 Ohms
- Signal range: 5-1500 Ohms
- R0\*: up to 350 Ohms





#### **A.2.4.7 Analog Outputs**

Each of the analog output channels can operate in one of ranges listed below:

Option 1	Hardware range: 0 – 5.0 VDC Signal range: 0 – 5.0 VDC (using > 1 k $\Omega$ load) Diagnostic Discrepancy Threshold: 2% of full scale
Option 2	Hardware range: 4– 20.0 mA Signal range: 4 – 20.0 mA (using a 50 – 350 $\Omega$ load) Diagnostic Discrepancy Threshold: 2% of full scale
Option 3	Hardware range: -10.0 – +10.0 VDC Signal range: -10.0 – +10.0 VDC (using > 1 k $\Omega$ load) Diagnostic Discrepancy Threshold: 2% of full scale
Option 4	Hardware range: 0– 20.0 mA Signal range: 0– 5.0 mA (using a 50 – 350 $\Omega$ load) Diagnostic Discrepancy Threshold: 2% of full scale

An analog output channel will be declared failed if the discrepancy between the DAC and ADC Units exceeds the diagnostic discrepancy threshold.

### **A.2.5 Operational Features**

Specific operational features that apply to the use of the RadICS Platform include the SOR and access controls for periodic maintenance.

#### **A.2.5.1 Safety Override Operation**

The SOR is a supplementary safety function of the RadICS Platform that permits a temporary override to safe-state values of the safety-critical outputs of the system when the SOR is set and allows a return to normal operation when the SOR is reset. The SOR may be used under administrative control to manually set RadICS Modules to a safe state while a maintenance work is performed in the rack.

The SOR can be set under any of several conditions (i.e., manual switch actuation or automatically by the Application Logic, if configured to do so). The SOR can only be reset by operator (or hardwired) action when all setting conditions are clear.

The SOR is always configured to be set globally by configuring the Set-SOR and Reset-SOR switches as inputs to the LM. The SOR can also be configured to be set locally (i.e., to affect only a specific output module) by configuring additional Set-SOR and Reset-SOR switches as inputs to one or more DOM or AOM.



A Keyswitch is recommended for the Set-SOR contacts for better assurance that the maintenance work has been authorized. A ganged continuous-contact pushbutton or switch can be used if there is a requirement to be able to quickly force the system into the safe state. A momentary-contact keyswitch is recommended for the Reset-SOR contact for better assurance that releasing the safe state has been authorized.

The SOR can also be configured to automatically transition through RUN (SAFE) mode to RUN mode by jumpering the Set-SOR and Reset-SOR pinouts (analogous to continuously closed switches) at the SOR connectors on the RadICS Chassis.

#### **A.2.5.2 Access Control Features**

The RadICS Platform has access control features to support TUNING mode operation.

The TUNING Keyswitch is typically mounted on the RadICS Chassis and is connected directly to a dedicated contact input on the LM. The ARMED Keyswitch operates a dry contact supplied by end user is used by RadICS Platform. It may be driven by any secure means (e.g., keyswitch). The dry contact is used to indicate that the end user downstream safety logic is secured in safe state. The ARMED key contact is connected to a designated input on LM. The keyswitches can be mounted anywhere that is convenient to the end user and consistent with their functions.

The TUNING keyswitch is typically controlled by the control room staff. This keyswitch must be present and turned to the "tune" position for the RadICS Module to provide power internally to the designated tuning port used to connect the MATS Tuning PC. The tuning activity is signaled to the MATS and the control room, as specified by the end user requirements.

The ARMED keyswitch is used to permit complete testing of single or multiple safety functions within the RadICS Platform system. The keyswitch is used to force all safety field outputs of the RadICS Platform to the safe state regardless of the state of the RadICS Platform outputs. A contact from this logic is provided to the RadICS Platform to indicate the safety load is in the safe state. The end user uses the ARMED keyswitch to place the RadICS Platform field outputs in the safe state whenever tuning the RadICS Platform Application ED and to test the effects of the tuning changes before putting the RadICS channel back online. The ARMED keyswitch circuit allows for complete testing by varying the input parameters through their complete range from non-trip conditions into trip conditions while the plant equipment is in the safe state.

#### **A.2.6 Setpoint Accuracy Calculations**

The Setpoint Analysis Support document (Reference A-4) provides the data recommended in EPRI TR-107330 for the following RadICS Platform components:

- Analog Inputs Modules (i.e., AIM, WAIM, TIM, and RIM)
- Discrete Inputs Modules
- Analog Outputs Modules
- Discrete Outputs Modules

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The accuracy specifications have been compiled from manufacturer's documentation and were updated based on the results of qualification testing of the RadICS Platform QTS and SQTS.

## **A.2.7 Reliability Calculations**

The RadICS Platform FMEA/FMEDA information can be used to develop reliability assessments, as specified by the end user requirements.

## **A.2.8 Equipment Qualification Envelope**

The RadICS Platform was qualified to the boundary conditions listed below. The parameters of the qualification envelope were updated once the qualification testing was completed.

### **A.2.8.1 *Radiation Exposure Withstand Analysis***

The radiation exposure withstand analysis demonstrated that the RadICS Platform QTS and SQTS will not experience failures or unacceptable degradation due to expected radiation exposure from normal and abnormal service conditions as required by RG 1.209 and EPRI TR-107330. Section 4.3.6 of EPRI TR 107330 defines the normal and abnormal radiation exposure levels the equipment must withstand and continue to meet the specified performance levels.

### **A.2.8.2 *Environmental Testing***

The environmental testing demonstrated that the RadICS Platform QTS and SQTS did not experience failures due to abnormal service conditions of temperature and humidity as required by RG 1.209 and IEEE Std 323-2003. Section 4.3.6 of EPRI TR 107330 defines the recommended normal and abnormal temperature and humidity exposure levels the test specimen must withstand (i.e., the test specimen must continue to meet the manufacturer specified performance levels).

### **A.2.8.3 *Seismic Testing***

Seismic testing demonstrated the suitability of the RadICS Platform for qualification as a Category 1 seismic device based on seismic withstand testing performed on the RadICS Platform QTS and SQTS in accordance with RG 1.100 and IEEE Std 344-2004. Section 4.3.9 of EPRI TR 107330 defines the seismic test levels to which the test specimen was exposed, while the test specimen continues to meet the manufacturer specified performance levels.

### **A.2.8.4 *Electromagnetic Interference /Radio Frequency Interference Testing***

The objective of EMI/RFI testing was to demonstrate the suitability of the RadICS Platform for qualification as a safety-related device with respect to EMI/RFI emissions and susceptibility levels. EMI/RFI testing of the RadICS Platform QTS and SQTS has been performed in accordance with RG 1.180, Revision 1, using additional guidance from EPRI TR-107330 as applicable. The specific EMI/RFI tests to be performed include:

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#### **A.2.8.5 *Electrical Fast Transient Testing***

The objective of EFT testing was to demonstrate the suitability of the RadICS Platform for qualification as a safety-related device with respect to EFT susceptibility levels. EFT testing of the RadICS Platform QTS and SQTS has been performed in accordance with RG 1.180 using additional guidance from EPRI TR-107330, as applicable.

#### **A.2.8.6 *Surge Withstand Testing***

The objective of surge withstand testing was to demonstrate the suitability of the RadICS Platform for qualification as a safety-related device with respect to surge withstand levels. Surge withstand testing of the RadICS Platform QTS and SQTS has been performed in accordance with RG 1.180, using additional guidance from EPRI TR-107330 as applicable.

#### **A.2.8.7 *Electrostatic Discharge Testing***

The objective of ESD testing was to demonstrate the suitability of the RadICS Platform for qualification as a safety-related device with respect to ESD withstand levels. EPRI TR-107330, Section 4.3.8, requires that the test specimen under qualification be tested for ESD withstand capability in accordance with the requirements of EPRI TR-102323.

#### **A.2.8.8 *Class 1E to Non-Class 1E Isolation Testing***

The objective of Class 1E to non-Class 1E isolation testing was to demonstrate the suitability of the RadICS Platform for qualification as a safety-related device with respect to providing electrical isolation at non-Class 1E field connections, as required by IEEE Std 384-1992. EPRI TR-107330, Section 6.3.6, requires that the test specimen under qualification be tested for Class 1E to non-Class 1E isolation capability in accordance with the requirements of EPRI TR-107330, Section 4.6.4.

### **A.2.9 Application Logic Development**

The Application Logic designer is responsible for designing into the logic the appropriate response to the Type III diagnostic signals specified in the system functional requirements specification. For example, the three diagnostic signals for a safety critical input (failure of the input signal, failure of the input channel hardware, and failure of the input module) should be carefully considered as possible reasons to drive the outputs to the safe state.

The RadICS Platform will not go into a fail-safe mode automatically upon detection of the following failures unless the Application Logic implements the desired action for these events:

- Any failure of a field input signal
- Any failure of an individual I/O channel on a Module
- Any complete failure of a Module
- Loss of communications between the LM and a DOM or AOM, which will only cause the affected DOM or AOM to go immediately to the safe state



- EEPROM failure after STARTUP, since these EEPROMs are used only at power-up. A failure detected during operation is an early warning that the next power-up will not succeed.

The end user should consult the RadICS Platform Product Safety Manual for information on the Application Logic decisions that need to be made.

#### **A.2.9.1 Verification of Chassis Configuration**

The Application Logic design should include logic to verify the following:

- The correct type of module is present in the appropriate slots
- The modules present in these slots are certified for use with the RadICS Platform
- The modules are not in CONFIGURATION mode

#### **A.2.9.2 Verification of I/O Module Status**

The Application Logic design should include logic to verify the following:

- No module critical to the system operation for safety has been removed from the chassis
- No module critical to the SIS operation for safety has suffered a complete failure (i.e., FAULTED mode)

#### **A.2.9.3 Detection of Safety-Critical I/O Failures**

The Application Logic design should include logic to respond to I/O channel failures as specified in the system functional requirements specification.

#### **A.2.9.4 Analog Input Signal Tolerance**

The Application Logic design should consider the tolerance involved in the self-diagnostic tests for an analog input channel hardware failure and the conversion accuracy in determining trip setpoints or any similar logic threshold. The Application Logic should incorporate specific considerations including:

- An AI channel is considered failed if the difference in reading of its two independent ADCs is > 2% of full-scale. (2% is default value, it can be changed during Application Logic design.)
- Reasonableness checks on analog inputs and calculated values.
- Allowance in the calibration so that RadICS can detect field transmitter failures that result in out-of-range signals.

#### **A.2.9.5 Setting the Safety Override or Tripping to Reach a Safe State**

The Application Logic can be designed to request the LM to set the SOR. In this state, all safety critical outputs are set to the safe state by the SOR, although in other respects the Application Logic runs normally. The SOR safe state is recoverable.

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The Application Logic can be designed to request a SOR-RESET (by no longer requesting a SOR-Set, but the actual reset must be performed by an operator or technician unless the RadICS Platform has been wired for automatic transition into RUN mode.

The Application Logic can be designed to request the LM to go to RUN (SAFE) mode, which drives all safety critical outputs to the safe state. Human intervention is required to release outputs from the safe state and pass them to the control of the Application Logic

The Application Logic can be designed to set the SOR on individual output modules so they are only put in the safe state. It is usually advisable to set all safety critical outputs to the safe state when any one single output channel goes to the safe state, whether due to individual failure or the result of Application Logic action. This action is advisable because to do otherwise would put some parts of a plant into a safe state but not others, thus possibly putting the plant into an unanalyzed state, which could pose unpredictable hazards. However, the decision to set all safety critical outputs to the safe state must be carefully evaluated based on system design requirements and potential operational impacts.

#### **A.2.9.6    *Latching Trip Decisions***

The Application Logic should include logic to latch trip decisions, as specified in the system functional requirements specification.

It is strongly recommended that trip decisions be latched, where the Application Logic designer intends that the trip action be retained until maintenance activity is complete. This is particularly important for safety functions that trip on a process variable going high and the shutdown of the plant process could cause this parameter value to drop below the setpoint.

#### **A.2.9.7    *Monitoring Module Temperature***

The Application Logic should monitor the operating temperature of the RadICS Modules and specify whether the condition is alarmed or the Module is put into the safe state, as specified in the system functional requirements specification.

### **A.3    *Installation***

#### **A.3.1    *Physical Security***

Radics LLC recommends that the RadICS Platform and other associated safety-related I&C equipment be installed in a secure location to which access is controlled.

#### **A.3.2    *Mounting***

The minimum space required around the chassis is as follows:

- Vertical space above the fan assembly portion of the chassis:  $\geq 3$  cm
- Vertical space below the chassis:  $\geq 3$  cm

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- Horizontal depth behind the chassis (to accommodate the I/O cables):  $\geq 15$  cm

The RadICS Chassis is supported by its front panel and should be installed with required number of bolts and the supplied locking brackets. The bolts should be torqued to the specified values.

RadICS Modules must be fully inserted, and the hold-down latches secured by screws. The screws should be torqued to the specified values.

The RadICS IOPMs must be fully inserted and the hold-down latches secured by screws. The screws should be torqued to the specified values.

Cables connected to the RadICS Chassis must be fully inserted and the locking bars is in the locked position. Unused connectors should be covered with a dust cap.

## **A.4 Routine Maintenance Activities**

This section provides the recommended periodic inspection and testing procedures for the RadICS Platform. These requirements are intended to identify important considerations for maintaining the environmental qualification of the RadICS Platform.

### **A.4.1 Periodic Inspection**

A visual inspection and then a physical inspection should be conducted periodically to confirm that the equipment is physically in the environment and condition that are expected. It is recommended to inspect the RadICS Platform whenever scheduled preventative maintenance is performed on equipment in the same cabinet.

Visually inspect the terminal blocks of all Modules and confirm:

- There is no evidence of corrosion (e.g., discoloration on conductors or terminals)
- There is no evidence of frayed wires

Physically inspect the RadICS Platform and its connections to confirm:

- The RadICS Chassis itself is firmly mounted
- All RadICS Modules are firmly in place and the latches are in the locked position
- All connector locking brackets are in place.

Inspect the RadICS Chassis vents for dust and confirm there is air flow at the vents at the front of the RadICS Chassis fan assembly.

### **A.4.2 Periodic Testing**

The RadICS Platform has extensive self-testing features. These tests are supplemented by the following periodic tests that are typically performed during a refueling outage:

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- [[

]]<sup>a,c,e</sup>

- Test injection signals should be used to drive the input variables to the end of the instrumentation range at the safe end of the instrumentation range (i.e., apply conditions that do not trip the safety setpoint). The injection signal should be gradually increased (or decreased) until the setpoint trips to verify it meets requirements. The injection signal should be reduced (or increased) to below (or above) the trip setpoint to verify that the [[  
]]<sup>a,c,e</sup>. The injection signal should be driven to the high (or low) end of the instrumentation range to check the calibration of the signal.

### A.4.3 Periodic Calibration

Periodic calibration of the analog inputs and outputs for the RadICS Platform is typically performed during a refueling outage. AIM, WAIM, TIM, RIM, or AOM calibration can be performed by removing the Module from the in-service chassis and installing it in the DLS or it may be performed in the in-service chassis. CONFIGURATION mode is used to calibrate Modules and places the Chassis in a safe state. The Radiy supplied calibration support equipment utilizes the Tuning interface to verify calibrated inputs and generate the desired outputs for calibration. Calibration is performed in accordance with plant procedures.

### A.4.4 Adjustable Parameter Tuning

Operational parameters may need to be adjusted during a reactor operating cycle or between cycles. The RadICS Platform provides the ability to tune these parameters via the Fiber Optic Tuning Interface. Tuning is normally locked out and is enabled only by a keyswitch. In this mode, tuning parameters that are specified in the Application ED can be adjusted by connecting a MATS Tuning PC with special software to the RadICS Platform system. The MATS Tuning PC requires a password.

The end user performs functional tests to confirm the tuning values before restoring the system to normal operation. The RadICS Platform system also checks tuning values for 'reasonableness' and basic validity. The Application Logic can also be engineered to perform other specified checks.

The LM will transition to the RUN (SAFE) mode if the TUNING keyswitch is present while ARMING keyswitch is not. The LM will transition to the TUNING mode if the TUNING and ARMING keyswitches are present. The LM will transition to the RUN mode if TUNING key or ARMING key is removed. The Tuning Parameters will be set to the previously stored values from the Tuning EEPROM if the keys are removed before a Tuning update is completed. The LM will transition into FAULTED mode if Type I faults are detected during self-diagnostics tests.





#### **A.4.5 Product Life**

The product lifetime of the RadICS Platform is 30 years from date of manufacture. There are no consumables related to RadICS Platform operation and periodic maintenance (e.g., batteries or electrolytic capacitors) that require periodic replacement.

#### **A.5 Appendix A References**

- 1 RadICS Document D11.1, "Product Safety Manual"
- 2 EPRI TR-107330, "Generic Requirements Specification for Qualifying a Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants," December 1996
- 3 RadICS Platform Master Configuration List, Radics LLC Document No. 2016-RTS002-MCL-018)
- 4 RadICS Setpoint Analysis Support, Radics LLC Document No. 2016-RTS002-SAS-003
- 5 RadICS Setpoint Analysis Support, Radics LLC Document No. 2019-SRTS004-SAS-003



## Appendix B: DI&C-ISG-04 Compliance Matrix

Section #	DI&C-ISG-04 Requirements	Compliance of the RadICS Generic Platform
1	<b>INTERDIVISIONAL COMMUNICATIONS</b>	
	<p>1 A safety channel should not be dependent upon any information or resource originating or residing outside its own safety division to accomplish its safety function. This is a fundamental consequence of the independence requirements of IEEE Std 603.<sup>1</sup> It is recognized that division voting logic must receive inputs from multiple safety divisions.</p>	<ul style="list-style-type: none"> <li>Physical and functional independence of communication divisions is achieved by configuring the LM ports used for the safety to non-safety interfaces for MATS and the LM and OCM ports used for intra- and inter-division communication for the project-specific system architecture. The RadICS Platform features described in Sections 6.3 and 6.6 do not depend upon information coming from outside its safety division, except for trip requests coming from the other divisions and input to the voting logic.</li> <li>The RadICS LM in a safety division provides functions of input data acquisition, data processing, application logic execution, diagnostics, and output data conditioning that do not depend on the other safety divisions.</li> </ul>
	<p>2 The safety function of each safety channel should be protected from adverse influence from outside the division of which that channel is a member. Information and signals originating outside the division must not be able to inhibit or delay the safety function. This protection must be implemented within the affected division (rather than in the sources outside the division), and must not itself be affected by any condition or information from outside the affected division. This protection must be sustained despite any operation, malfunction, design error, communication error, or software error or corruption existing or originating outside the division.</p>	<ul style="list-style-type: none"> <li>RadICS Platform equipment and communications design prevents propagation of failures between redundant equipment in separate divisions. In addition, communication paths to non-safety I&amp;C systems are electrically isolated with one-way communications from the RadICS Platform to the non-safety I&amp;C system. These features prevent faults in a non-safety I&amp;C system from adversely affecting the RadICS Platform.</li> <li>The implementation of radial (point-to-point) architecture in RadICS Platform inter-division communication links provide the RadICS Platform with the capability to maintain failure-free data exchange between I&amp;C components even when one of the divisions has failed. Additional measures designed to achieve the desired physical and functional independence are the application of fiber-optic communication lines for data exchange between I&amp;C components and the separation of safety and control functions from information and diagnostic functions.</li> <li>The RadICS LMs exchange voting logic data with other safety divisions by fiber optic interface that meets the SIL 3 safety requirement.</li> </ul>



Section #	DI&C-ISG-04 Requirements	Compliance of the RadICS Generic Platform
		<ul style="list-style-type: none"> <li>• Communication among safety divisions is point-to-point and asynchronous. The transmitting safety division sends only once during a Work Cycle.</li> <li>• The Communication Units (i.e., OPTO, LVDS, LAN, and RS-232/485) []</li> </ul> <p>]]<sup>a,c,e</sup>. The receiving safety divisions do not need to wait or synchronize with these messages to issue their own safety actuations.</p> <ul style="list-style-type: none"> <li>• IF SD of communications is crucial for providing safety integrity and functional safety. IF SD is performed by each safety division's RadICS Module ED SD, since communication interfaces cannot perform any actions except data transmission.</li> <li>• Generalized measures intended to provide IF SD are: <ul style="list-style-type: none"> <li>- []</li> </ul> </li> </ul> <p>]]<sup>a,c,e</sup></p>
3	<p>A safety channel should not receive any communication from outside its own safety division unless that communication supports or enhances the performance of the safety function. Receipt of information that does not support or enhance the safety function would involve the performance of functions that are not directly related to the safety function. Safety systems should be as simple as possible. Functions that are not necessary for safety, even if they enhance reliability, should be executed outside the safety system. A safety system designed to perform functions not directly related to the safety function would</p>	<ul style="list-style-type: none"> <li>• The only input coming from outside a safety division is the input needed for the system coincidence voting logic (i.e., request for actuation coming from the other independent divisions). Up to 4 divisions (i.e., LMs) can be used in system coincidence voting (e.g., 1-out-of-2, 2-out-of-3, 2-out-of-4 are possible). The LM will detect that it is connected with the correct LM in other chassis for system coincidence voting).</li> <li>• The safety system is kept as simple as possible and does not include functions not related to the safety functions.</li> </ul>



Section #	DI&C-ISG-04 Requirements		Compliance of the RadICS Generic Platform
		be more complex than a system that performs the same safety function, but is not designed to perform other functions. The more complex system would increase the likelihood of failures and software errors. Such a complex design, therefore, should be avoided within the safety system.	
	4	The communication process itself should be carried out by a communications processor <sup>ii</sup> separate from the processor that executes the safety function, so that communications errors and malfunctions will not interfere with the execution of the safety function.	<ul style="list-style-type: none"> <li>The safety function is executed on the LM FPGA board and the actual data exchange communications between safety divisions is [[ ]]<sup>a,c,e</sup> and transmitted to other safety division through the corresponding Optical Transceiver Unit (OPTO) using the Radiy Proprietary Protocol (RPP).</li> <li>Faster and more deterministic performance due to capability of executing logic functions and control algorithms in a parallel mode due to the hardware parallelism inherent to FPGA technology. This parallelism also provides the ability to [[ ]]<sup>a,c,e</sup></li> </ul>
		The communication and function processors should operate asynchronously, sharing information only by means of dual-ported memory or some other shared memory resource that is dedicated exclusively to this exchange of information.	<ul style="list-style-type: none"> <li>FPGA technology [[ ]]<sup>a,c,e</sup></li> <li>All communication links of the OPTO Unit are executed according point-to-point principle between two different Modules of the same type (e.g., LM to LM). [[ ]]<sup>a,c,e</sup>.</li> </ul> <p>Each communication link uses a separate OPTO Unit. The OPTO Unit is safety related.</p>
		The function processor, the communications processor, and the shared memory, along with all supporting circuits and software, are all considered to be safety-related, and must be designed, qualified, fabricated, etc., in accordance with 10 CFR Part 50, Appendix A and B.	<ul style="list-style-type: none"> <li>RadICS Platform Hardware, as well as, the FBL electronic designs are safety related items, and have been designed, qualified and fabricated, as described in Section 6 and Section 8.</li> </ul>



Section #	DI&C-ISG-04 Requirements	Compliance of the RadICS Generic Platform
	<p>Access to the shared memory should be controlled in such a manner that the function processor has priority access to the shared memory to complete the safety function in a deterministic manner. For example, if the communication processor is accessing the shared memory at a time when the function processor needs to access it, the function processor should gain access within a timeframe that does not impact the loop cycle time assumed in the plant safety analyses. If the shared memory cannot support unrestricted simultaneous access by both processors, then the access controls should be configured such that the function processor always has precedence. The safety function circuits and program logic should ensure that the safety function will be performed within the timeframe established in the safety analysis, and will be completed successfully without data from the shared memory in the event that the function processor is unable to gain access to the shared memory.</p>	<ul style="list-style-type: none"> <li>The RadICS Modules utilize [[ ]]<sup>a,c,e</sup> is entirely controlled by the FPGA with no chance of interference from external interfaces. This feature ensures that the safety function LM can always have access without delay to the communication data for transmission or reception of data.</li> <li>Communication internal to a Module FPGA and for communication between Modules via the backplane is controlled (prioritized) by the Logic Module via the Work Cycle phases. Processing inputs and outputs are separated in time.</li> <li>Asynchronous communication between chassis (LM to LM and OCM to OCM) over fiber optics utilize a special memory structure (i.e., two independent and equal memory blocks) that is controlled to prevent simultaneous read and write operations from the same memory block.</li> <li>Separate input and output memory blocks are allocated as part of the Module design and are configured for the individual signal assignments in a point-to-point manner during the Application Logic design using RPCT.</li> </ul>
5	<p>The cycle time for the safety function processor should be determined in consideration of the longest possible completion time for each access to the shared memory. This longest-possible completion time should include the response time of the memory itself and of the circuits associated with it, and should also include the longest possible delay in access to the memory by the function processor assuming worst-case conditions for the transfer of access from the communications processor to the function</p>	<ul style="list-style-type: none"> <li>The FPGA design of the RadICS Platform does [[ ]]<sup>a,c,e</sup> for different processes. Each FPGA has [[ ]]<sup>a,c,e</sup> and, as described above, the transfer of data is handled by the RadICS LMs that operate in a deterministic timeframe.</li> <li>The Work Cycle duration of each RadICS LM functioning in all modes (except POWERED-OFF and FAULTED modes) is [[ ]]<sup>a,c,e</sup> milliseconds (see Section 6.10).</li> </ul>



Section #	DI&C-ISG-04 Requirements		Compliance of the RadICS Generic Platform
		processor. Failure of the system to meet the limiting cycle time should be detected and alarmed.	
	6	The safety function processor should perform no communication handshaking and should not accept interrupts from outside its own safety division.	<ul style="list-style-type: none"> <li>Safety function logics with the RadICS Modules [[ ]]<sup>a,c,e</sup>.</li> <li>Communications with LMs between safety divisions (system coincidence voting) is handled in communication processing Units that are [[ ]]<sup>a,c,e</sup> which does not affect the Application ED and other RadICS Module Units [[ ]]<sup>a,c,e</sup></li> </ul>
	7	Only predefined data sets should be used by the receiving system. Unrecognized messages and data should be identified and dispositioned by the receiving system in accordance with the pre-specified design requirements. Data from unrecognized messages must not be used within the safety logic executed by the safety function processor.	<ul style="list-style-type: none"> <li>All communication links are pre-defined and established during implementation. All communications are implemented on a point-to-point basis that [[ ]]<sup>a,c,e</sup></li> <li>All communications are transmitted in a [[ ]]<sup>a,c,e</sup> to ensure correctness and integrity of each data message.</li> </ul>
		Message format and protocol should be pre-determined. Every message should have the same message field structure and sequence, including message identification, status information, data bits, etc. in the same locations in every message.	<ul style="list-style-type: none"> <li>DTP SD, due to specific structure, allow implementation of reliable IF SD. Each transmitted data packet includes the following data:               <ul style="list-style-type: none"> <li>[[ ]]</li> </ul> </li> </ul>



Section #	DI&C-ISG-04 Requirements		Compliance of the RadICS Generic Platform
			]] <sup>a,c,e</sup>
		Every datum should be included in every transmit cycle, whether it has changed since the previous transmission or not, to ensure deterministic system behavior.	<ul style="list-style-type: none"> <li>All data is transmitted during each Work Cycle. Each message is [[</li> </ul> <p>]]<sup>a,c,e</sup></p>
	8	Data exchanged between redundant safety divisions or between safety and nonsafety divisions should be processed in a manner that does not adversely affect the safety function of the sending divisions, the receiving divisions, or any other independent divisions.	<ul style="list-style-type: none"> <li>FPGA technology allows for [[</li> </ul> <p>]]<sup>a,c,e</sup></p> <ul style="list-style-type: none"> <li>Communication between a safety division and non-Class 1E equipment is not allowed, except the following:               <ul style="list-style-type: none"> <li>Tuning Interface (see Section 6.9)</li> <li>MATS (see Sections 6.3 and 6.6)</li> <li>OCM RS-232/485 interface (See Section 6.2.5.2.12)</li> </ul> </li> <li>Communications ports are monitored and blocked except when specifically required (e.g., tuning interface). The safety division is placed in a safe state while the tuning interface is active.</li> <li>The interface to the MATS is one-way broadcast (i.e., non-interfering), rated at SIL 2. [[</li> </ul> <p>]]<sup>a,c,e</sup> Thus, the MATS is also non-interfering.</p>



Section #	DI&C-ISG-04 Requirements		Compliance of the RadICS Generic Platform
			<ul style="list-style-type: none"> <li>The interface to the OCM RS-232/485 is one-way broadcast (i.e., non-interfering). [[  ]]<sup>a,c,e</sup> Thus, the OCM RS-232/485 is also non-interfering.</li> <li>In the sending safety division, failure to send to the non-Class 1E equipment due to communication does not impair the safety function of the division</li> </ul>
	9	Incoming message data should be stored in fixed predetermined locations in the shared memory and in the memory associated with the function processor. These memory locations should not be used for any other purpose. The memory locations should be allocated such that input data and output data are segregated from each other in separate memory devices or in separate pre-specified physical areas within a memory device.	<ul style="list-style-type: none"> <li>The RadICS Module FPGA utilizes [[  ]]<sup>a,c,e</sup> is entirely controlled by the RadICS Module FPGA with no chance of interference from external interfaces. This feature ensures that the LM can always have access without delay to the communication data for transmission or reception of data.</li> <li>The areas of [[  ]]<sup>a,c,e</sup></li> </ul>
	10	Safety division software should be protected from alteration while the safety division is in operation. On-line changes to safety system software should be prevented by hardwired interlocks or by physical disconnection of maintenance and monitoring equipment. A workstation (e.g., engineer or programmer station) may alter addressable constants, setpoints, parameters, and other settings associated with a safety function only by way of the dual-processor / shared-memory scheme described in this guidance, or when the associated channel is inoperable. Such a workstation should be physically restricted from making changes in more than one division at a time. The restriction should be by means of physical cable disconnect, or by means of keylock switch that either physically opens the data transmission circuit or	<ul style="list-style-type: none"> <li>[[  ]]<sup>a,c,e</sup></li> <li>In TUNING mode, parameters which are provided for in the Application Electronic Design can be adjusted by connecting a laptop computer with special software to the RadICS LM. TUNING mode requires the use of a TUNING key and a contact that comes from the end user's downstream safety logic that indicates that this downstream logic is locked into the safe state (controlled by what is called the ARMING key). This permits the end user to fully test his tuning changes under safe conditions. Placing</li> </ul>





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	<p>interrupts the connection by means of hardwired logic. "Hardwired logic" as used here refers to circuitry that physically interrupts the flow of information, such as an electronic AND gate circuit (that does not use software or firmware) with one input controlled by the hardware switch and the other connected to the information source: the information appears at the output of the gate only when the switch is in a position that applies a "TRUE" or "1" at the input to which it is connected. Provisions that rely on software to effect the disconnection are not acceptable. It is noted that software may be used in the safety system or in the workstation to accommodate the effects of the open circuit or for status logging or other purposes.</p>	<p>the Module in a safe state during tuning ensures only one safety division can undergo tuning at a time.</p>
11	<p>Provisions for interdivisional communication should explicitly preclude the ability to send software instructions to a safety function processor unless all safety functions associated with that processor are either bypassed or otherwise not in service. The progress of a safety function processor through its instruction sequence should not be affected by any message from outside its division.</p>	<ul style="list-style-type: none"> <li>• [[</li> </ul> <p style="text-align: right;">]]<sup>a,c,e</sup></p>
	<p>For example, a received message should not be able to direct the processor to execute a subroutine or branch to a new instruction sequence.</p>	<p>See above.</p>
12	<p>Communication faults should not adversely affect the performance of required safety functions in any way. Faults, including communication faults, originating in nonsafety equipment, do not</p>	<ul style="list-style-type: none"> <li>• Communication transmission between safety divisions is implemented [[</li> </ul> <p style="text-align: right;">]]<sup>a,c,e</sup>. Communications faults are detected using diagnostics performed by the receiving division LM.</p>



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	constitute "single failures" as described in the single failure criterion of 10 CFR Part 50, Appendix A.	<ul style="list-style-type: none"> <li>• Communication between a safety division and non-Class 1E equipment is not allowed, except the following: <ul style="list-style-type: none"> <li>- Tuning Interface (see Section 6.9)</li> <li>- MATS (see Sections 6.3 and 6.6)</li> <li>- OCM RS-232/485 interface (See Section 6.2.5.2.12)</li> </ul> </li> <li>• Communications ports are monitored and blocked except when specifically required (e.g., tuning interface). The safety division is placed in a safe state while the tuning interface is active.</li> <li>• The interface to the MATS is one-way broadcast (i.e., non-interfering), rated at SIL 2. Receiving ports not used on the ED level. Thus, the MATS is also non-interfering.</li> <li>• The interface to the OCM RS-232/485 is one-way broadcast (i.e., non-interfering). [[</li> </ul> <p style="text-align: right;">]]<sup>a,c,e</sup> Thus, the OCM RS-232/485 is also non-interfering.</p>
	<p>Examples of credible communication faults include, but are not limited to, the following:</p> <ol style="list-style-type: none"> <li>1. Messages may be corrupted due to errors in communications processors, errors introduced in buffer interfaces, errors introduced in the transmission media, or from interference or electrical noise.</li> <li>2. Messages may be repeated at an incorrect point in time.</li> <li>3. Messages may be sent in the incorrect sequence.</li> <li>4. Messages may be lost, which includes both failures to receive an uncorrupted message or to acknowledge receipt of a message.</li> <li>5. Messages may be delayed beyond their permitted arrival time window for several reasons, including errors in the transmission medium, congested transmission lines,</li> </ol>	<p>Communication failures are detected, and appropriate safety actions are taken (see Section 6.4).</p> <ol style="list-style-type: none"> <li>1. [[</li> </ol> <p style="text-align: right;">]]<sup>a,c,e</sup> only point-to-point communication links are used, with no chance for other stations to transmit on a communication link.</p> <ol style="list-style-type: none"> <li>4. Loss of messages is detected. [[</li> </ol> <p style="text-align: right;">]]<sup>a,c,e</sup> Failure to transmit or receive a message cannot interfere with the safety function.</p> <ol style="list-style-type: none"> <li>5. Only point-to-point communication links are utilized. If the is not received [[</li> </ol> <p style="text-align: right;">]]<sup>a,c,e</sup>, this situation is detected.</p> <ol style="list-style-type: none"> <li>6. [[</li> </ol> <p style="text-align: right;">]]<sup>a,c,e</sup> Only point-to-point communication links are utilized. [[</p>



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	<p>interference, or by delay in sending buffered messages.</p> <p>6. Messages may be inserted into the communication medium from unexpected or unknown sources.</p> <p>7. Messages may be sent to the wrong destination, which could treat the message as a valid message.</p> <p>8. Messages may be longer than the receiving buffer, resulting in buffer overflow and memory corruption.</p> <p>9. Messages may contain data that is outside the expected range.</p> <p>10. Messages may appear valid, but data may be placed in incorrect locations within the message.</p> <p>11. Messages may occur at a high rate that degrades or causes the system to fail (i.e., broadcast storm).</p> <p>12. Message headers or addresses may be corrupted.</p>	<p>]]<sup>a,c,e</sup></p> <p>11. Broadcast storm will not influence the receiving Module. [[</p> <p>]]<sup>a,c,e</sup>. The Communication Units (i.e., OPTO, LVDS, LAN, and RS-232/485) are [[</p> <p>]]<sup>a,c,e</sup>. The receiving safety divisions do not need to wait or synchronize with these messages to issue their own safety actuations.</p> <p>12. The receiving processing LM tests the [[</p> <p>]]<sup>a,c,e</sup> corruption is detected.</p>
13	<p>Vital<sup>iii</sup> communications, such as the sharing of channel trip decisions for the purpose of voting, should include provisions for ensuring that received messages are correct and are correctly understood. Such communications should employ error-detecting or error-correcting coding along with means for dealing with corrupt, invalid, untimely or otherwise questionable data. The effectiveness of error detection/correction should be demonstrated in the design and proof testing of the associated</p>	<ul style="list-style-type: none"> <li>• Communication failures are detected and appropriate safety actions are taken.</li> <li>• No error correction methods are used.</li> </ul>



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		codes, but once demonstrated is not subject to periodic testing. Error-correcting methods, if used, should be shown to always reconstruct the original message exactly or to designate the message as unrecoverable. None of this activity should affect the operation of the safety-function processor.	
	14	Vital <sup>iii</sup> communications should be point-to-point by means of a dedicated medium (copper or optical cable). In this context, "point-to-point" means that the message is passed directly from the sending node to the receiving node without the involvement of equipment outside the division of the sending or receiving node. Implementation of other communication strategies should provide the same reliability and should be justified.	<ul style="list-style-type: none"> <li>Communications between safety divisions is accomplished by dedicated point-to-point links via fiber optics. Communications are always passed directly from sending node to receiving node with no chance for outside interference.</li> </ul>
	15	Communication for safety functions should communicate a fixed set of data (called the "state") at regular intervals, whether data in the set has changed or not.	<ul style="list-style-type: none"> <li>[[  ]]<sup>a,c,e</sup>, regardless of whether the data has changed or not.</li> </ul>
	16	Network connectivity, liveness, and real-time properties essential to the safety application should be verified in the protocol. Liveness, in particular, is taken to mean that no connection to any network outside the division can cause an RPS/ESFAS communication protocol to stall, either deadlock or livelock. (Note: This is also required by the independence criteria of: (1) 10 CFR Part 50, Appendix A, General Design Criteria ("GDC") 24, which states, "interconnection of the protection and control systems shall be limited so as to assure that safety is not significantly impaired."; and (2) IEEE 603-1991	<ul style="list-style-type: none"> <li>[[  ]]<sup>a,c,e</sup></li> <li>Communication between a safety division and non-Class 1E equipment is not allowed, except the following: <ul style="list-style-type: none"> <li>Tuning Interface (see Section 6.9)</li> <li>MATS (see Sections 6.3 and 6.6)</li> <li>OCM RS-232/485 interface (See Section 6.2.5.2.12)</li> </ul> </li> <li>Communications ports are monitored and blocked except when specifically required (e.g., tuning interface). The safety division is placed in a safe state while the tuning interface is active.</li> </ul>



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		IEEE Standard Criteria for Safety Systems for Nuclear Power Generating Stations.) (Source: NUREG/CR-6082, 3.4.3)	<ul style="list-style-type: none"> <li>The interface to the MATS is one-way broadcast (i.e., non-interfering), rated at SIL 2. [[ ]]<sup>a,c,e</sup> Thus, the MATS is also non-interfering.</li> <li>The interface to the OCM RS-232/485 is one-way broadcast (i.e., non-interfering). [[  ]]<sup>a,c,e</sup> Thus, the OCM RS-232/485 is also non-interfering.</li> <li>In the sending safety division, failure to send to the non-Class 1E equipment due to communication does not impair the safety function of the division.</li> </ul>
	17	Pursuant to 10 CFR 50.49, the medium used in a vital <sup>iii</sup> communications channel should be qualified for the anticipated normal and post-accident environments.	<ul style="list-style-type: none"> <li>The RadICS Platform includes selected medium and equipment used for communications (including optical fibers, twisted-shielded pair cables, etc.) that are qualified for mild environment usage (see Chapter 9).</li> </ul>
		For example, some optical fibers and components may be subject to gradual degradation as a result of prolonged exposure to radiation or to heat. In addition, new digital systems may need susceptibility testing for EMI/RFI and power surges, if the environments are significant to the equipment being qualified.	See above.
	18	Provisions for communications should be analyzed for hazards and performance deficits posed by unneeded functionality and complication.	<ul style="list-style-type: none"> <li>Each transmitted message contains the data necessary to accomplish the needed safety functions and elements needed for diagnostic to allow the Modules to detect communication failure.</li> <li>[[ ]]<sup>a,c,e</sup></li> </ul>
	19	If data rates exceed the capacity of a communications link or the ability of nodes to handle traffic, the system will suffer congestion. All links and nodes should have sufficient capacity to support all functions. The applicant should identify the true data rate, including overhead, to ensure that communication bandwidth is sufficient to ensure proper performance of all safety functions.	<ul style="list-style-type: none"> <li>[[  ]]<sup>a,c,e</sup> All communications are point-to-point and [[  ]]<sup>a,c,e</sup></li> </ul>



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		Communications throughput thresholds and safety system sensitivity to communications throughput issues should be confirmed by testing.	
	20	The safety system response time calculations should assume a data error rate that is greater than or equal to the design basis error rate and is supported by the error rate observed in design and qualification testing.	<ul style="list-style-type: none"> <li>The RadICS Platform has a deterministic behavior. The Work Cycle for each Module is fixed and the maximum response time for system architecture is established using the maximum response time of each LM and communication links. This deterministic behavior guarantees that safety outputs will always be delivered within the computed maximum response time limit. Errors in communications do not impact or increase the system maximum response time. See Section 6.10 for further details on Work Cycles and response times.</li> </ul>
<b>2</b>		<b>COMMAND PRIORITIZATION</b>	
			<ul style="list-style-type: none"> <li>The generic RadICS Platform does not include a priority logic Module. Therefore, this section of DI&amp;C-ISG-04 does not apply.</li> </ul>
<b>3</b>		<b>MULTIDIVISIONAL CONTROL AND DISPLAY STATIONS</b>	
3.1		<p>Independence and Isolation</p> <p>The following provisions are applicable to multidivisional control and display stations. These guidance provisions do not apply to conventional hardwired control and indicating devices (hand switches, indicating lamps, analog indicators, etc.).</p>	<ul style="list-style-type: none"> <li>The generic RadICS Platform does not include multidivisional control and display stations. Therefore, the requirements for multi-division controls in this section of DI&amp;C-ISG-04 do not apply.</li> </ul>
	1	<p>Nonsafety stations receiving information from one or more safety divisions:</p> <p>All communications with safety-related equipment should conform to the guidelines for interdivisional communications.</p>	<ul style="list-style-type: none"> <li>Communication between a safety division and non-Class 1E equipment is not allowed, except the following:               <ul style="list-style-type: none"> <li>Tuning Interface (see Section 6.9)</li> <li>MATS (see Sections 6.3 and 6.6)</li> <li>OCM RS-232/485 interface (See Section 6.2.5.2.12)</li> </ul> </li> <li>Communications ports are monitored and blocked except when specifically required (e.g., tuning interface). The safety division is placed in a safe state while the tuning interface is active.</li> <li>The interface to the MATS is one-way broadcast (i.e., non-interfering), rated at SIL 2. <u>[[</u></li> </ul>



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			<p>]]<sup>a,c,e</sup> Thus, the MATS is also non-interfering.</p> <ul style="list-style-type: none"> <li>The interface to the OCM RS-232/485 is one-way broadcast (i.e., non-interfering). [[</li> </ul> <p>]]<sup>a,c,e</sup> Thus, the OCM RS-232/485 is also non-interfering.</p> <ul style="list-style-type: none"> <li>In the sending safety division, failure to send to the non-Class 1E equipment due to communication does not impair the safety function of the division</li> </ul>
	2	<p>Safety-related stations receiving information from other divisions (safety or nonsafety):</p> <p>All communications with equipment outside the station's own safety division, whether that equipment is safety-related or not, should conform to the guidelines for interdivisional communications. Note that the guidelines for interdivisional communications refer to provisions relating to the nature and limitations concerning such communications, as well as guidelines relating to the communications process itself.</p>	<p>RadICS systems require interdivisional communications to support voting logics. In addition, one-way (broadcast only) communications from safety divisions to non-safety display systems that can aggregate data and perform functions/display of data/interdivisional comparisons. The interface to the MATS is one-way broadcast (i.e., non-interfering), rated at SIL 2. [[</p> <p>]]<sup>a,c,e</sup> Thus, the MATS is also non-interfering.</p> <p>The interface to the OCM RS-232/485 is one-way broadcast (i.e., non-interfering). [[</p> <p>]]<sup>a,c,e</sup> Thus, the OCM RS-232/485 is also non-interfering.</p>
	3	Nonsafety stations controlling the operation of safety-related equipment	The generic RadICS Platform does not provide this control capability.
	4	Safety-related stations controlling the operation of equipment in other safety-related divisions	The generic RadICS Platform does not provide this control capability.
	5	<p>Malfunctions and Spurious Actuations.</p> <p>The result of malfunctions of control system resources (e.g., workstations, application servers, protection/control processors) shared between systems must be consistent with the assumptions made in the safety analysis of the plant.</p>	The generic RadICS Platform does not provide this control capability; therefore, these requirements do not apply.
3.2		Human Factors Considerations	This will be determined on a project-specific basis.



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3.3	Diversity and Defense-in-Depth (D3) Considerations	This will be determined on a project-specific basis.

## DI&amp;C-ISG-04 Notes

- i IEEE Std 603-1991 (cited in 10 CFR 50.55a(h)) provides the following definitions:

channel: "An arrangement of components and modules as required to generate a single protective action signal when required by a generating station condition. A channel loses its identity where single protective action signals are combined."

division: "The designation applied to a given system or set of components that enables the establishment and maintenance of physical, electrical, and functional independence from other redundant sets of components."

For the purposes of this guidance document, the terms channel and division are further described below. Note that the following is for illustrative purposes, and is not intended to impose requirements or new interpretations:

A safety channel as used herein is a set of safety-related instruments and equipment, along with the associated software, that together generate a protective actuation or trip signal to initiate a single protective function. While an analog/hardwired system would have each functional circuit clearly assigned to only one channel, the processor and other components in a digital system may be assigned to multiple channels within a single division.

A safety division is the collection of all safety channels that are powered by a single power division. Different channels perform different functions. Different divisions perform the same set of functions, and are redundant to one another. Licensing typically credits redundancy among divisions. The voting logic that generates the final actuation signal to an item of plant equipment typically resides in one division and receives input from redundant channels in all divisions. For the purposes of this guidance, it is to be assumed that each of the actuation signals entering the voting logic that establishes the final actuation signal to an item of plant equipment is in a different division, regardless of the particular usage of the term "division" for a particular nuclear power plant.

- ii "Processor" may be a CPU or other processing technology such as simple discrete logic, logic within an FPGA, an ASIC, etc.
- iii "Vital" communications as used herein are communications that are needed to support a safety function. Failure of vital communications could inhibit the performance of the safety function. The most common implementation of vital communications is the distribution of channel trip information to other divisions for the purpose of voting.





## Appendix C: RadICS Electronic Design Documents

DI&C-ISG-06 (Reference C-1) contains a list of documents in Enclosure B that are identified for submittal with a license amendment request. The same list has been applied to digital I&C platform topical report reviews with mixed success. NRC has also been conducting a pilot license amendment request review using DI&C-ISG-06. In public meetings NRC has communicated lessons learned regarding the use of DI&C-ISG-06 for license amendment requests and topical report reviews.

An important lesson learned was with the usefulness of the documents submitted based on the DI&C-ISG-06 guidance. In particular, the list is not well suited for digital platform topical report reviews. NRC has indicated that it has found it more useful to get a smaller set of documents with the application and have access to other documents) via an electronic reading room) to conduct audits of the detailed design information that supports the information in the topical report.

The following document item numbers in Enclosure B of DI&C-ISG-06 are addressed directly in the RadICS Topical Report:

- 1.1, Hardware Architecture Descriptions
- 1.2, Quality Assurance Plan for Digital Hardware
- 1.16, Design Analysis Reports
- 1.20, Theory of Operation Description
- 2.1, Safety Analysis

The RadICS Platform design documents are cross referenced to the relevant document item numbers in Enclosure B of DI&C-ISG-06 in Table C-1.

The following document item numbers from Enclosure B of DI&C-ISG-06 are not applicable to the generic platform RadICS Topical Report:

- 1.15, D3 Analysis
- 1.17, System Description
- 1.19, System Response Time Analysis Report
- 1.21, Setpoint Methodology
- 1.22, Vendor Software Plan
- 2.3, As-Manufactured, System Configuration Documentation
- 2.6, Summary of Test Results (Including FAT)
- 2.8, FMEA
- 2.9, System Build Documents
- 2.13, As-Manufactured Logic Diagrams
- 2.14, System Response Time Confirmation Report
- 2.16, Setpoint Calculations
- 3.1, Software Integration Report
- 3.2, Individual V&V Problem Reports up to FAT
- 3.4, Test Procedure Specification

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- 3.5, Completed Test Procedures and Reports
- 3.6, Test Incident Reports
- 3.8, Software Project Risk Management Report
- 3.9, Circuit Schematics
- 3.10, Detailed System and Hardware Drawings
- 4.3, Software Training Plan
- 4.5, Site Test Documentation
- 4.7, Software Maintenance Manuals
- 4.8, Software Training Manuals
- 4.9, Installation Configuration Tables

### ***C.1 RadICS Electronic Design Related Documents***

Table C-1 contains a listing of the RadICS Platform design documents associated with the Electronic Designs for the RadICS Modules. An initial set of documents planned for submittal with the RadICS Topical Report (i.e., Phase 1 Submittals) is identified. Another set of documents to be submitted after completion of the RadICS EQ test program (i.e., Phase 2 Submittals) are identified. The remaining documents are available for audit, as requested by NRC. A set of documents planned for submittal with the RadICS Topical Report Supplement is identified. Additional documents (or extracts of key information) have been submitted, as requested by NRC during the topical report review.

**Table C-1: RadICS Electronic Design Related Documents**

RadICS Electronic Design Related Documents		DI&C-ISG-06 Category and Cross Reference
Number	Title	
D1.0	RadICS Product Concept Document	Available for Audit
D2.1	RadICS Functional Safety Management Plan	Phase 1 Submittal Items 1.4, 1.5, 1.6, 1.7, 1.8, and 1.24
D2.2	RadICS Configuration Management Plan	Phase 1 Submittal Item 1.10
D2.2.0	Baseline Independent Items Configuration Audit Report	Available for Audit Item 3.3
D2.2.1	Requirements Baseline Configuration Audit Report	Available for Audit Item 3.3
D2.2.2	Architecture Design Baseline Configuration Audit Report	Available for Audit Item 3.3
D2.2.3	Detailed Design and Coding Baseline Configuration Audit Report	Available for Audit Item 3.3
D2.2.4	Integration Baseline Configuration Audit Report	Available for Audit Item 3.3
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RadICS Electronic Design Related Documents		DI&C-ISG-06 Category and Cross Reference
Number	Title	
D2.2.5	Release Baseline Configuration Audit Report	Available for Audit Item 3.3
D2.3	RadICS Tool Selection and Evaluation Report	Phase 1 Submittal Items 1.23 and 2.17
D2.4	RadICS Overall Verification and Validation Plan	Phase 1 Submittal Item 1.9 Available for Audit for Topical Report Supplement Review
D2.4.1	RadICS Verification and Validation Testing Checklists	Available for Audit
D2.6	RadICS Document Plan	Available for Audit
D2.6.1	Project Implementation Plan	Available for Audit
D2.6.2	Project Repository Structure	Available for Audit
D2.7	RadICS Personnel Plan	Available for Audit
D2.7.1	Training Records	Available for Audit
D2.8	RadICS Security Analysis Report	Phase 1 Submittal Items 1.26 and 1.27
D2.9	RadICS Report about Compliance of FSMP to IEC 61508	Available for Audit
D2.10	RadICS Functional Safety Management Plan Extension	Phase 1 Submittal Items 1.4, 1.5, 1.6, 1.7, 1.8, and 1.24
D2.12	RadICS Project Change Log	Available for Audit
D3.1	RadICS Safety Requirements Specification	Phase 1 Submittal Item 1.12
D3.2	RadICS SRS Review Report	Available for Audit Item 2.2
D3.7	RadICS Equipment Qualification Safety Requirements Specification	Available for Audit
D3.8	RadICS Equipment Qualification Safety Requirements Specification Review Report	Available for Audit Item 2.2
D3.9	RadICS Requirements Traceability Matrix	Available for Audit Item 2.7



RadICS Electronic Design Related Documents		DI&C-ISG-06 Category and Cross Reference		
Number	Title			
D3.9.1	RadICS Requirements Tracing Matrix book	Available for Audit Item 2.7		
D3.9.2	RadICS Module Static Code Analysis / Code Review Report Tracing Report	Available for Audit Item 2.2		
D4.0	RadICS Safety Validation Test Plan	Phase 1 Submittal Item 1.11 Available for Audit for Topical Report Supplement Review		
D4.1	RadICS Safety Validation Test Specification	Available for Audit Item 2.4		
D4.2	RadICS Safety Validation Test Report	Available for Audit Item 2.5		
D5.1	RadICS Product Architecture Document	Phase 1 Submittal Items 1.3 and 1.12 Available for Audit for Topical Report Supplement Review		
D5.2	RadICS PAD Review Report	Available for Audit Item 2.2		
D5.4	RadICS AFBL/Application Logic Detailed Requirements Specification	Available for Audit		
D5.5	RadICS AFBL/Application Logic Detailed Requirements Specification Review Report	Available for Audit		
D7.23	RadICS Guideline on Design and Coding with VHDL	Available for Audit		
D7.24	RadICS FMEDA Report	Available for Audit Items 1.18 and 2.15		
D7.26.1 – D7.26-6	RadICS Modules Fault Insertion Test Specifications	Available for Audit Item 2.4		
D7.26.12 – D7.26.14	RadICS WAIM, TIM, RIM Fault Insertion Test Specifications	Available for Audit Item 2.4		
D8.11	RadICS FBL Detailed Description	Available for Audit Item 1.13		
D8.12	RadICS FBL VHDL Code	Available for Audit Item 3.7		
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RadICS Electronic Design Related Documents		DI&C-ISG-06 Category and Cross Reference
Number	Title	
D8.13	RadICS FBL VHDL Static Code Analysis / Code Review Report	Available for Audit Item 2.2
D8.15	RadICS FBL Detailed Description Review Report	Available for Audit Item 2.2
D9.11	RadICS FBL Functional Test Plan and Specification	Available for Audit Item 2.4
D9.12	RadICS FBL Functional Test Report	Available for Audit Item 2.5
D8.21.1 - D8.21.6	RadICS Modules ED Detailed Descriptions	Available for Audit Item 1.13
D8.21.8	RadICS PSWD ED Detailed Description	Available for Audit Item 1.13
D8.21.12 - D8.21.14	RadICS WAIM, TIM, RIM ED Detailed Descriptions	Available for Audit Item 1.13
D8.25.1 - D8.25.6	RadICS Modules ED Detailed Description Review Reports	Available for Audit Item 2.2
D8.25.8	RadICS PSWD ED Detailed Description Review Report	Available for Audit Item 2.2
D8.25.12 - D8.25.14	RadICS WAIM, TIM, RIM ED Detailed Description Review Reports	Available for Audit Item 2.2
D8.21.10	RadICS ED DD Data Protocols and Packages	Available for Audit
D8.22.1 - D8.22.6	RadICS Modules ED VHDL Codes	Available for Audit Item 3.7
D8.22.8	RadICS PSWD ED VHDL Code	Available for Audit Item 3.7
D8.22.12 - D8.22.14	RadICS WAIM, TIM, RIM ED VHDL Codes	Available for Audit Item 3.7
D8.23.1 - D8.23.6	RadICS Modules ED VHDL Static Code Analysis / Code Review Reports	Available for Audit Item 2.2
D8.23.8	RadICS PSWD ED VHDL Static Code Analysis / Code Review Report	Available for Audit Item 2.2
D8.23.12 - D8.23.4	RadICS WAIM, TIM, RIM ED VHDL Static Code Analysis / Code Review Reports	Available for Audit Item 2.2
D8.31	RadICS AFBL VHDL Detailed Description	Available for Audit
D8.32	RadICS AFBL VHDL code	Available for Audit



RadICS Electronic Design Related Documents		DI&C-ISG-06 Category and Cross Reference
Number	Title	
D8.33	RadICS AFBL VHDL Static Code Analysis/Code Review Report	Available for Audit Item 2.2
D8.35	RadICS AFBL VHDL Detailed Description Review Report	Available for Audit Item 2.2
D9.21.1 - D9.21.6	RadICS Modules ED VHDL Functional Test Plan and Specifications	Available for Audit Item 2.4
D9.21.8	RadICS PSWD ED VHDL Functional Test Plan and Specification	Available for Audit Item 2.4
D9.21.12 - D9.21.14	RadICS WAIM, TIM, RIM ED VHDL Functional Test Plan and Specifications	Available for Audit Item 2.4
D9.22.1 - D9.22.6	RadICS Modules ED VHDL Functional Test Reports	Available for Audit Item 2.5
D9.22.8	RadICS PSWD ED VHDL Functional Test Report	Available for Audit Item 2.5
D9.22.12 - D9.22.14	RadICS WAIM, TIM, RIM ED VHDL Functional Test Reports	Available for Audit Item 2.5
D9.23.1 - D9.23.6	RadICS Modules ED Logic Level Simulation and Timing Test Reports	Available for Audit Item 2.5
D9.23.8	RadICS PSWD ED Logic Level Simulation and Timing Test Report	Available for Audit Item 2.5
D9.23.12 - D9.23.14	RadICS WAIM, TIM, RIM ED Logic Level Simulation and Timing Test Reports	Available for Audit Item 2.5
D9.23.9.1 – D9.23.9.6	RadICS Modules ED Synthesis Results Review Reports	Available for Audit Item 2.2
D9.23.9.8	RadICS PSWD ED Synthesis Results Review Report	Available for Audit Item 2.2
D9.23.9.12 – D9.23.9.14	RadICS WAIM, TIM, RIM ED Synthesis Results Review Reports	Available for Audit Item 2.2
D9.24.1 - D9.24.6	RadICS Modules ED Static Timing Analysis Test Reports	Available for Audit Item 2.5
D9.24.8	RadICS PSWD ED Static Timing Analysis Test Report	Available for Audit Item 2.5
D9.24.12 - D9.24.14	RadICS WAIM, TIM, RIM ED Static Timing Analysis Test Reports	Available for Audit Item 2.5
D9.24.9.1 – D9.24.9.6	RadICS Modules ED Place and Route Results Review Reports	Available for Audit Item 2.2



RadICS Electronic Design Related Documents		DI&C-ISG-06 Category and Cross Reference
Number	Title	
D9.24.9.8	RadICS PSWD ED Place and Route Results Review Report	Available for Audit Item 2.2
D9.24.9.12 – D9.24.9.14	RadICS WAIM, TIM, RIM ED Place and Route Results Review Reports	Available for Audit Item 2.2
D9.25.1 - D9.25.6	RadICS Modules ED Bitstream Generation Results Review Reports	Available for Audit Item 2.2
D9.25.8	RadICS PSWD ED Bitstream Generation Results Review Report	Available for Audit Item 2.2
D9.25.12 - D9.25.14	RadICS WAIM, TIM, RIM ED Bitstream Generation Results Review Reports	Available for Audit Item 2.2
D9.31	RadICS AFBL Test Plan and Specification	Available for Audit
D9.32	RadICS AFBL Functional Test Report	Available for Audit
D10.1	RadICS Integration Test Plan	Phase 1 Submittal Item 1.11 Available for Audit for Topical Report Supplement Review
D10.2	RadICS Integration Test Specification	Available for Audit Item 2.4
D10.3	RadICS Integration Test Report	Available for Audit Item 2.5
D10.4.1 – D10.4.6	RadICS Hardware Fault Insertion Test Reports	Available for Audit Item 2.5
D10.4.12 – D10.4.14	RadICS WAIM, TIM, RIM Fault Insertion Test Reports	Available for Audit Item 2.5
D11.1	RadICS Product Safety Manual	Phase 1 Submittal Items 4.1, 4.2, 4.4, and 4.6 Available for Audit for Topical Report Supplement Review
D11.4	RadICS Product Safety Manual Review Report	Available for Audit Item 2.2
D11.5	RadICS Application Function Block Library User Reference Manual	Available for Audit
D11.6	RadICS Platform Configuration Tool User Manual	Available for Audit

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RadICS Electronic Design Related Documents		DI&C-ISG-06 Category and Cross Reference
Number	Title	
D11.10	AFBL User Reference Manual Review Report	Available for Audit
D11.11	RPCT User Manual Review Report	Available for Audit
D12.1	RadICS Functional Safety Management Audit Plan	Phase 1 Submittal
D12.2.1	RadICS Functional Safety Management Audit Report	Available for Audit
D12.2.2	RadICS Functional Safety Management Audit Report	Available for Audit
D12.2.3	RadICS Functional Safety Management Audit Report	Available for Audit
D12.3	RadICS Safety Case – FSMP Requirements Compliance	Available for Audit
D13.1	RadICS Functional Safety Assessment Plan	Available for Audit
D13.2	RadICS Functional Safety Assessment Report	Available for Audit
D13.3	RadICS IEC 61508 Assessment Recommendations	Available for Audit
2015-RTS001-SRS-009	NRC RadICS Test Specimen (RTS-001) System Requirements Specification	Available for Audit
2019-SRTS003-SRS-009	NRC Supplement RadICS Test Specimen (SRTS-003) System Requirements Specification	Available for Audit for Topical Report Supplement Review
2015-RTS001-SWRS-011	NRC RadICS Test Specimen (RTS-001) Software Requirements Specification	Available for Audit
2019-SRTS003-SWRS-011	NRC Supplement RadICS Test Specimen (SRTS-003) Software Requirements Specification	Available for Audit for Topical Report Supplement Review
2016-RTS002-QAPP-001	Quality Assurance Project Plan	Available for Audit
2016-RTS002-MCL-018	Master Configuration List	Available for Audit
2019-SRTS004-MCL-018	RadICS Platform Master Configuration List	Available for Audit for Topical Report Supplement Review
2016-RTS002-EQTP-004	Equipment Qualification Test Plan	Phase 1 Submittal Items 1.14 and 2.11
2019-SRTS004-EQTP-040	RadICS Supplemental Equipment Qualification Test Plan	Available for Audit for Topical Report Supplement Review





RadICS Electronic Design Related Documents		DI&C-ISG-06 Category and Cross Reference
Number	Title	
2016-RTS002-EQTSR-040	Equipment Qualification Test Summary Report	Phase 2 Submittal Item 2.12
2019-SRTS004-EQTSR-040	RadICS Supplemental Equipment Qualification Test Summary Report	Submittal for Topical Report Supplement Review
2016-RTS002-FATP-005	Factory Acceptance Test Procedure	Available for Audit
2016-RTS002-SSCTP-006	System Setup and Checkout Test Procedure	Available for Audit
2016-RTS002-OTP-007	Operability Test Procedure	Available for Audit
2016-RTS002-PTP-008	Prudency Test Procedure	Available for Audit
2016-RTS002-ETP-010	Environmental Test Procedure	Available for Audit
2016-RTS002-STP-011	Seismic Test Procedure	Available for Audit
2016-RTS002-EMITP-012	EMI/RFI Test Procedure	Available for Audit
2016-RTS002-EFTTP-013	Electrical Fast Transient Test Procedure	Available for Audit
2016-RTS002-SWTP-014	Surge Withstand Test Procedure	Available for Audit
2016-RTS002-ESDTP-015	Electrostatic Discharge Test Procedure	Available for Audit
2016-RTS002-1ETP-016	Class 1E to Non-1E Isolation Test Procedure	Available for Audit
2016-RTS002-SAS-003	RadICS Setpoint Analysis Support	Available for Audit
2019-SRTS004-SAS-003	RadICS Setpoint Analysis Support	Available for Audit for Topical Report Supplement Review
2019-SRTS004-FATP-005	Factory Acceptance Test Procedure	Available for Audit for Topical Report Supplement Review
2019-SRTS004-SSCTP-006	System Setup and Checkout Test Procedure	Available for Audit for Topical Report Supplement Review
2019-SRTS004-OTP-007	Operability Test Procedure	Available for Audit for Topical Report Supplement Review



RadICS Electronic Design Related Documents		DI&C-ISG-06 Category and Cross Reference
Number	Title	
2019-SRTS004-PTP-008	Prudency Test Procedure	Available for Audit for Topical Report Supplement Review
2019-SRTS004-ETP-010	Environmental Test Procedure	Available for Audit for Topical Report Supplement Review
2019-SRTS004-STP-011	Seismic Test Procedure	Available for Audit for Topical Report Supplement Review
2019-SRTS004-EMITP-012	EMI/RFI Test Procedure	Available for Audit for Topical Report Supplement Review
2019-SRTS004-EFTTP-013	Electrical Fast Transient Test Procedure	Available for Audit for Topical Report Supplement Review
2019-SRTS004-SWTP-014	Surge Withstand Test Procedure	Available for Audit for Topical Report Supplement Review
2019-SRTS004-ESDTP-015	Electrostatic Discharge Test Procedure	Available for Audit for Topical Report Supplement Review
2019-SRTS004-1ETP-016	Class 1E to Non-1E Isolation Test Procedure	Available for Audit for Topical Report Supplement Review
2015-RTS001-CGDP-LM-101	Commercial Grade Dedication Plan for LM	Phase 1 Submittal Item 1.25 Available for Audit for Topical Report Supplement Review
2015-RTS001-CGDP-DIM-003	Commercial Grade Dedication Plan for DIM	Phase 1 Submittal Item 1.25



RadICS Electronic Design Related Documents		DI&C-ISG-06 Category and Cross Reference
Number	Title	
2015-RTS001-CGDP-DOM-102	Commercial Grade Dedication Plan for DOM	Phase 1 Submittal Item 1.25
2015-RTS001-CGDP-AIM-103	Commercial Grade Dedication Plan for AIM	Phase 1 Submittal Item 1.25 Available for Audit for Topical Report Supplement Review
2015-RTS001-CGDP-AOM-104	Commercial Grade Dedication Plan for AOM	Phase 1 Submittal Item 1.25 Available for Audit for Topical Report Supplement Review
2015-RTS001-CGDP-OCM-106	Commercial Grade Dedication Plan for OCM	Phase 1 Submittal Item 1.25 Available for Audit for Topical Report Supplement Review
2015-RTS001-CGDP-CH-107	Commercial Grade Dedication Plan for Chassis	Phase 1 Submittal Item 1.25 Available for Audit for Topical Report Supplement Review
2015-RTS001-CGDP-IOPM-131	Commercial Grade Dedication Plan for I/O Connections Protection Module	Phase 1 Submittal Item 1.25 Available for Audit for Topical Report Supplement Review
2015-RTS001-CGDP-VM-132	Commercial Grade Dedication Plan for Ventilation Module	Phase 1 Submittal Item 1.25
2019-SRTS003-CGDP-RIM-151	RadICS Platform Commercial Grade Dedication Plan for RIM	Available for Audit for Topical Report Supplement Review
2019-SRTS003-CGDP-TIM-150	RadICS Platform Commercial Grade Dedication Plan for TIM	Available for Audit for Topical Report Supplement Review



RadICS Electronic Design Related Documents		DI&C-ISG-06 Category and Cross Reference
Number	Title	
2019-SRTS003-CGDP-WAIM-152	RadICS Platform Commercial Grade Dedication Plan for WAIM	Available for Audit for Topical Report Supplement Review
2019-SRTS003-CGDP-Cb-154	RadICS Platform Commercial Grade Dedication Plan for Cables	Available for Audit for Topical Report Supplement Review
2017-RTS001-CGDSR_AOM-370	Commercial Grade Dedication Summary Report for AOM	Phase 2 Submittal Item 2.18 Submittal for Topical Report Supplement Review
2017-RTS001-CGDSR_LM-371	Commercial Grade Dedication Summary Report for LM	Phase 2 Submittal Item 2.18 Submittal for Topical Report Supplement Review
2017-RTS001-CGDSR_AIM-372	Commercial Grade Dedication Summary Report for AIM	Phase 2 Submittal Item 2.18 Submittal for Topical Report Supplement Review
2017-RTS001-CGDSR_DIM-373	Commercial Grade Dedication Summary Report for DIM	Phase 2 Submittal Item 2.18
2017-RTS001-CGDSR_DOM-374	Commercial Grade Dedication Summary Report for DOM	Phase 2 Submittal Item 2.18
2017-RTS001-CGDSR_OCM-375	Commercial Grade Dedication Summary Report for OCM	Phase 2 Submittal Item 2.18 Submittal for Topical Report Supplement Review
2017-RTS001-CGDSR_IOPM-376	Commercial Grade Dedication Summary Report for IOPM	Phase 2 Submittal Item 2.18 Submittal for Topical Report Supplement Review



RadICS Electronic Design Related Documents		DI&C-ISG-06 Category and Cross Reference
Number	Title	
2017-RTS001-CGDSR_CH-377	Commercial Grade Dedication Summary Report for Chassis	Phase 2 Submittal Item 2.18 Submittal for Topical Report Supplement Review
2017-RTS001-CGDSR_VM-378	Commercial Grade Dedication Summary Report for VM	Phase 2 Submittal Item 2.18
2019-SRTS003-CGDP-RIM-157	Commercial Grade Dedication Summary Report for RIM	Submittal for Topical Report Supplement Review
2019-SRTS003-CGDP-TIM-156	Commercial Grade Dedication Summary Report for TIM	Submittal for Topical Report Supplement Review
2019-SRTS003-CGDP-WAIM-158	Commercial Grade Dedication Summary Report for WAIM	Submittal for Topical Report Supplement Review
2019-SRTS003-CGDP-Cb-159	Commercial Grade Dedication Summary Report for Cables	Audit for Topical Report Supplement Review

## C.2 Appendix C References

- 1 DI&C-ISG-06, Revision 1, "Licensing Process"



## Appendix D: Evaluation of Diversity in an Application Using the RadICS Platform

The diversity of a typical application using the RadICS Platform technology was evaluated using the methodology outlined in NUREG/CR-7007 Reference D-1.

### D.1 Evaluation Process

The NUREG/CR-7007 evaluation process consists of the following steps:

1. Classify the diversity strategy — This step involves recognition of the technology employed in the diverse systems based on the design descriptions or, if explicitly referenced, identification of the specific diversity strategy selected.
2. Confirm inherent diversity credit — This step relates to the determination of technology usage and the impact of technology difference.
3. Identify intentional diversity usage — This step consists of identification of the diversity criteria that are intentionally applied. The documentation of the proposed diversity strategy should explicitly describe the intentional diversities on which it is based.
4. Categorize diversity usage in relation to the corresponding strategy classification — This step involves capturing the combination of diversity criteria in either tabular form or a spreadsheet followed by classification in terms of a corresponding strategy and subsequent determination of the degree of adherence to one of the strategies identified in NUREG/CR-7007
5. Assess the adequacy of the diversity strategy — The activity associated with this step depends on the categorization of the proposed diversity strategy determined in Step 4.

A baseline strategy is one where the diversity usage is consistent with one of the baseline combinations of diversity criteria defined for any of the three strategy classifications in NUREG/CR-7007. The associated actions are to confirm that the diverse systems provide the specified technology difference (Step 1), the system designs do not compromise the related credit for inherent diversity (Step 2), and the explicit diversity usage employs the full set of intentional diversities (Step 3).

A variant of baseline strategy is one where the diversity is consistent with one of the alternate combinations of diversity criteria described for any of the three strategy classifications. The associated actions are to perform an assessment comparable to that described for the baseline strategy category (Step 5) with the supplemental determination of whether the conditions associated with suitability of the variant are present.

The order of steps 2 and 3 were reversed for the RadICS Platform diversity strategy to better align the steps with the RadICS Platform diversity strategy decisions. Specifically, the key decisions affecting the diversity strategy were chips selection and IEC 61508 Safety Integrity Level (SIL) 3 certification (i.e., functionally diverse self-tests and diagnostics). From these key decisions other inherent diversity attributes flowed from the detailed design implementation.

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## ***D.2 Diversity Strategy Classification***

The RadICS Platform employs several internal diversity features to provide sufficient protection to address CCFs that may be introduced using digital FPGA technology within the RadICS Platform. The RadICS Platform defensive measures work together to limit the effects of these failures and place the system into defined safe states. This RadICS Platform diversity strategy flows directly from the design strategy to achieve IEC 61508:2010 SIL 3 certification.

The RadICS Platform diversity strategy is a variant of the Strategy C, "Architectural Variants within a Technology."

## ***D.3 Identification of Intentional Diversity Usage for RadICS Platform***

The CPLD-based watchdog in the PSWD Unit is separate and inherently diverse from the Module FPGAs. Table 10-1 identifies the key technology differences between the FPGAs and CPLD. These inherent technology differences mitigate the consequences of common cause failure vulnerabilities associated with the FPGA and CPLD chip technologies. Other aspects of the RadICS Platform diversity strategy are discussed in Section 10.3.3

Appendix A of NUREG 7007/CR defines seven diversity attributes and related diversity criteria. The intentional diversity attributes specified for the RadICS Platform are:

- Design: Different architectures based on the intentional use the FPGA for the Electronic Design safety functions (i.e., signal acquisition, signal conversion, protection algorithms, and communications) and associated self-test and diagnostics and the CPLD for the PSWD function.
- Equipment Manufacturer: Same manufacturer of different versions of the same technology class (i.e., programmable logic device) based on the selection of FPGAs and CPLDs manufactured by Altera.
- Logic Processing Equipment: Different component integration architectures based on the allocation of Electronic Design safety function and self-test and diagnostic functions to segregated portions of the FPGA and the allocation of the PSWD functions to the CPLD.
- Function: Different purpose, function, control logic, or actuation means of same underlying mechanism based on the explicit design of the FPGA Electronic Design safety functions and functionally diverse self-test and diagnostic functions along with the separate and functionally diverse PSWD functions on the CPLD through the FMEDA process.
- Life-cycle: Different management teams within the same company based on the independence between the design team and the V&V team for the validation of the self-test and diagnostic and PSWD functions through FIT.
- Life-cycle: Different lifecycle documents for development of the FPGA self-test and diagnostics and PSWD functions on the CPLD.
- Logic: Different algorithms, logic, and program architecture based on the hardware parallelism inherent to FPGA technology for executing logic functions and control algorithms in a parallel mode and the segregation of Electronic Design safety functions and self-test and diagnostic functions on the same integrated circuit.



- Logic: Different algorithms, logic, and program architecture between the FPGA self-test and diagnostics and PSWD functions on the CPLD. No common design element or libraries used for the development of these separate functions.

#### ***D.4 Confirmation of Inherent Diversity Credit***

The key decisions to use FPGA and CPLD chips along with the decision to achieve SIL 3 certification resulted in several inherent diversity attributes for the RadICS Platform diversity strategy. The FPGA technology allows for more deterministic performance than a microprocessor due to capability of executing logic functions and control algorithms in a parallel mode due to the hardware parallelism inherent to FPGA technology. This parallelism also provides the ability to segregate functions on the same integrated circuit (e.g., such as Electronic Design safety functions and self-test and diagnostics). The resulting circuits are pure hardware without additional layers of platform software (operating system, drivers, etc.). Dedicated separate hardware for all functions provides the advantages of computational efficiency, but from the reliability point of view, a more important aspect is the separation of functions. There is no need for resource allocation such as memory, processor time, or data transfer on a bus. This eliminates the risk of functions interfering with each other or with the operating system or other platform functions.

The inherent diversity attributes credited for the RadICS Platform are:

- Logic Processing Equipment: Different data flow architectures based on the parallel processing of the Electronic Design safety function signals and the segregation of parallel processing of the self-test and diagnostic signals.
- Function: Different response time scale based on the parallel processing of the individual Electronic Design safety function signals and the use of three separate clock domains for the Electronic Design safety functions, self-test and diagnostic functions, and the PSWD functions.
- Life-cycle: Different designers, engineers, and/or programmers by crediting the third-party IEC 61508 certification organization for its role with the validation of the self-test and diagnostics, PSWD functions, and Netlist self-tests through the FMEDA.
- Life-cycle: Different implementation/validation teams by crediting the independent Radiy validation for its role with the validation of the self-test and diagnostics, PSWD functions, and Netlist self-tests through the fault insertion testing based on test cases established by the third-party IEC 61508 certification organization.
- Logic: Different timing or order of execution based on the parallel processing of the individual Electronic Design safety function signals and the use of three separate clock domains for the Electronic Design safety functions, self-test and diagnostic functions, and the PSWD functions.
- Logic: Different runtime environments based on the parallel processing of the individual Electronic Design safety function signals and the use of three separate clock domains for the Electronic Design safety functions, self-test and diagnostic functions, and the PSWD functions.
- Logic: Different functional representations based on the fundamental differences in the functionality of Electronic Design safety functions, self-test and diagnostic features, and the PSWD Unit.

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## ***D.5 Identification of Intentional Diversity Typical of Applications Using a RadICS Platform***

The intentional and inherent diversity attributes identified for the RadICS Platform augment the existing diversity features of the I&C system designs for the operating fleet. The functional and signal diversity incorporated into the protection system functional requirements is maintained. This diversity is expressed in the signal selection and protection system algorithms established and accepted for the plant design. The additional functional diversity that has been added to reactor trip systems based on operating experience (e.g., requiring both undervoltage and shunt trip features for reactor trip breakers) is maintained.<sup>13</sup> Additional diversity has been added to the plant I&C designs through compliance with 10 CFR 50.62 is maintained.<sup>14</sup>

The intentional system diversity attributes that exist in operating plants and maintained for systems modernized with the RadICS Platform are:

- **Function:** Different underlying mechanisms to accomplish safety function based on the existing system echelons (i.e., control reactor trip, engineered safety features actuation, and monitoring), reactor trip breaker action mechanisms, and anticipated transients without scram (ATWS) risk reduction systems.
- **Signal:** Different parameters sensed by different physical effects based on the existing signal diversity in the reactor trip, engineered safety features actuation, and ATWS risk reduction systems.

## ***D.6 Comparison of RadICS Diversity to Strategy C***

The RadICS Platform diversity attributes are compared to the diversity attributes for Strategy C in Table D-1. The differences are identified below:

- **Equipment Manufacturer** – The RadICS Platform is conservatively credited with less diversity than Strategy C by treating the FPGA and CPLD as different versions of the same product rather than different products.
- **Logic Processing Equipment** – The RadICS Platform is conservatively credited with less diversity than Strategy C by treating the FPGA and CPLD logic process as different logic processing versions in same architecture rather than different logic processing architectures since the FPGA and the CPLD originate from different families of devices from the same company. They have different microarchitectures and structural characteristics.
- **Function** – The RadICS Platform is credited with more diversity than Strategy C by recognizing the inherent diversity associated with the three separate clock domains. Additionally, the intentional diversity typical of applications using a RadICS Platform with the different underlying mechanisms to accomplish safety function present in the existing plant I&C system designs (ATWS operating experience and 10 CFR 50.62) is also recognized.

<sup>13</sup> NRC Generic Letter 83-28, "Required Actions Based on Generic Implications of Salem ATWS Events"

<sup>14</sup> 10 CFR 50.62, "Requirements for reduction of risk from anticipated transients without scram (ATWS) events for light-water-cooled nuclear power plants."



- Life-cycle – The RadICS Platform is conservatively credited with less diversity than Strategy C by treating the third-party IEC 61508 certification organization as a different management team within the same company rather than as a different design company due to its focused role with the validation of the self-test and diagnostics through the FMEDA.
- Logic - The RadICS Platform is credited with more diversity than Strategy C by recognizing the inherent diversity for different timing or order of execution based on the parallel processing of the individual Electronic Design safety function signals and the use of three separate clock domains for the Electronic Design safety functions, self-test and diagnostic functions, and the PSWD functions.
- Signal - The RadICS Platform is conservatively credited with less diversity than Strategy C by only recognizing that different are parameters sensed by different physical effects based on the existing signal diversity in the protection system utilizing the RadICS Platform. Additional diversity may be present in the existing overall plant architecture and the combination of the control, reactor trip, engineered safety features actuation, monitoring, and ATWS risk reduction systems. This additional diversity is credited in the evaluation of the RadICS Platform diversity strategy.

**Table D-1: Comparison of RadICS Diversity to Strategy C**

Diversity Attribute	Strategy C	RadICS Platform
<b>Design</b>		
Different technologies	-	-
Different approaches within a technology	-	-
Different architectures	X	X
<b>Equipment Manufacturer</b>		
Different manufacturers of fundamentally different equipment designs	-	-
Same manufacturer of fundamentally different equipment designs	-	-
Different manufacturers of same equipment design	X	-
Same manufacturer—different version	-	X
<b>Logic Processing Equipment</b>		
Different logic processing architectures	X	-
Different logic processing versions in same architecture	-	X
Different component integration architectures	X	-
Different data flow architectures	-	i
<b>Function</b>		
Different underlying mechanisms to accomplish safety function	-	X
Different purpose, function, control logic, or actuation means of same underlying mechanism	X	X
Different response time scale	-	i
<b>Life-cycle</b>		
Different design organizations/companies	X	-
Different management teams within the same company	-	X
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Diversity Attribute	Strategy C	RadICS Platform
Different designers, engineers, and/or programmers	i	i
Different implementation/validation teams	i	i
Logic		
Different algorithms, logic, and program architecture	X	X
Different timing or order of execution	-	i
Different runtime environments	X	i
Different functional representations	X	i
Signal		
Different parameters sensed by different physical effects	X	X
Different parameters sensed by the same physical effects	X	-
Same parameter sensed by a different redundant set of similar sensors	X	-

### ***D.7 Adequacy of the RadICS Diversity Strategy***

The intentional and inherent diversity attributes for the RadICS Platform were entered into the NUREG/CR-7007 worksheet. The results are shown in Table D-2. The results for the RadICS Platform (i.e., 0.97 normalized score) compare favorably with the results for Strategy C (i.e., 0.98 normalized score).

### ***D.8 Appendix D References***

- 1 NUREG/CR-7007, "Diversity Strategies for Nuclear Power Plant Instrumentation and Control Systems"



Table 12-2: NUREG/CR-7007 Worksheet Results for RadICS Platform

ATTRIBUTE CRITERIA		Click to Clear Worksheet	RadICS			
			Application			
		RANK	DCE WT	INT	INH	SCORE
DESIGN	Different technologies	1	0.500			0.000
	Different approaches within a technology	2	0.333			0.000
	Different architectures	3	0.167	X		0.167
	DAE WT. AND SUBTOTAL		1.000		0.167	0.167
EQUIPMENT MANUF.	Different manufacturers of fundamentally different equipment designs	1	0.400			0.000
	Same manufacturer of fundamentally different equipment designs	2	0.300			0.000
	Different manufacturers of same equipment design	3	0.200			0.000
	Same manufacturer of different versions of the same equipment design	4	0.100	X		0.100
	DAE WT. AND SUBTOTAL		0.250		0.025	0.100
LOGIC PROC. EQUIP.	Different logic processing equipment architectures	1	0.400			0.000
	Different logic processing versions in same equipment architecture	2	0.300	X		0.300
	Different component integration architectures	3	0.200			0.000
	Different data flow architectures	4	0.100		i	0.100
	DAE WT. AND SUBTOTAL		0.644		0.258	0.400
FUNCTION	Different underlying mechanisms to accomplish safety function	1	0.500	X		0.500
	Different purpose, function, control logic, or actuation means of same underlying mechanism	2	0.333	X		0.333
	Different response time scale	3	0.167		i	0.167
	DAE WT. AND SUBTOTAL		0.600		0.600	1.000
LIFECYCLE	Different design organizations/companies	1	0.400			0.000
	Different management teams within the same company	2	0.300	X		0.300
	Different designers, engineers, and/or programmers	3	0.200		i	0.200
	Different testers, installers, or certification personnel	4	0.100		i	0.100
	DAE WT. AND SUBTOTAL		0.683		0.410	0.600
SIGNAL	Different reactor or process parameters sensed by different physical effects	1	0.500	X		0.500
	Different reactor or process parameters sensed by the same physical effect	2	0.333			0.000
	The same process parameter sensed by a different redundant set of similar sensors	3	0.167			0.000
	DAE WT. AND SUBTOTAL		0.867		0.434	0.500
LOGIC	Different algorithms, logic, and logic architecture	1	0.400	X		0.400
	Different timing or order of execution	2	0.300		i	0.300
	Different runtime environments	3	0.200		i	0.200
	Different functional representations	4	0.100		i	0.100
	DAE WT. AND SUBTOTAL		0.733		0.733	1.000
RadICS Score (x100)				263		
Normalized Score				0.97		
Basis for Normalizing		271				





## Appendix E: Request for Additional Information Cross Reference

### *E.1 RadICS Request for Additional Information Cross Reference*

NRC Office Instruction LIC-500 (Reference E-1) specifies that the request for additional (RAI) questions and responses should be included as an appendix to the Topical Report. Alternately, the NRC notes that if the Topical Report has been revised to incorporate the RAI responses directly into the report, a table listing each RAI and where the changes were made in the TR can be used.

Table E-1 contains a cross reference showing the RadICS Topical Report sections revised based on the submittal of supplemental information and the responses to RAI questions.

**Table E-1: RadICS Request for Additional Information Cross Reference**

Topical Report Section	Letter Reference
Section 1.6 revised	Reference E-3 (RAI-PI-05)
Section 5.4.7 revised	Reference E-4
Section 6.2.2 revised	Reference E-3 (RAI-PI-01 and RAI-PI-05)
Section 6.2.4.1	Reference E-3 (RAI-PI-01 and RAI-PI-05)
Section 6.2.5.2.13 revised	Reference E-3 (RAI-PI-03)
Section 6.3.2.1 revised	Reference E-3 (RAI-PI-06)
Section 6.3.2.2 revised	Reference E-3 (RAI-PI-04)
Section 6.3.2.3 revised	Reference E-3 (RAI-PI-09)
Section 6.3.2.4 revised	Reference E-3 (RAI-PI-09)
Section 6.4.4.3 revised	Reference E-2
Section 6.5 revised	Reference E-3 (RAI-PI-07)
Section 6.11 revised	Reference E-2
Section 6.11.1 added	Reference E-2
Section 6.11.2 added	Reference E-2
Section 6.11.3 added	Reference E-2
Section 6.11.3.1 added	Reference E-2
Section 6.11.3.2 added	Reference E-2
Section 6.11.3.3 added	Reference E-2



Topical Report Section	Letter Reference
Section 6.11.4 added	Reference E-2
Section 6.11.4.1 added	Reference E-2
Section 6.11.4.2 added	Reference E-2
Section 6.11.3.2 added	Reference E-2
Section 6.11.5 added	Reference E-2
Table 6-4 revised	Reference E-3 (RAI-PI-02)
Section 10.3 revised	Reference E-4
Section 10.3.1 added	Reference E-4
Section 10.3.2 added	Reference E-4
Section 10.3.3 added	Reference E-4
Section 10.3.4 added	Reference E-4
Section 10.4 added	Reference E-4
Section 10.5 revised	Reference E-4
Section 12.2.5 added	Reference E-4
Section A.2.1 revised	Reference E-3 (RAI-PI-05)
Section A.3.2 revised	Reference E-3 (RAI-PI-05)
Appendix B revised	Reference E-3 (RAI-PI-08 and RAI-PI-09)
Appendix D added	Reference E-4

## ***E.2 Appendix E References***

- 1 NRC Office Instruction LIC-500, Revision 7, "Topical Report Process," (ADAMS Accession No. ML18227A063)
- 2 Radics LLC letter to NRC dated: September 15, 2017, "Submittal of RadICS Digital I&C Platform Topical Report Supplemental Information," (ADAMS Accession No. ML17275A191)
- 3 Radics LLC letter to NRC dated April 13, 2018, "Response to Request for Additional Information for RadICS Topical Report (CAC NO.: MF841 1; EPID: L-2016-TOP-0010)," (ADAMS Accession No. ML18107A238)
- 4 Radics LLC letter to NRC dated August 2, 2018, "Submittal of RadICS Digital I&C Platform Topical Report Supplemental Information Update (Docket Number 99902032)," (ADAMS Accession No. ML18219A747)