DOOSAN

HF Controls

HF CONTROLS CONTROL SYSTEM

HFC-6000 Product Line Components

FPGA Platform
Diagnostic Design Specification

Document No: DS901-001-81 Revision: B

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Reviewed By: Eric Patrizi

Approved By: Gordon Ngo

Revision History

Date	Revision	Author	Changes
9/19/2014	A	L. Andrews	Initial Release
5/13/2015	B	Ron Chiu	Update for current implementation

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1.0 SCOPE

The primary purpose of the HFC-6000 FPGA Platform Diagnostics is to provide FPU I/O, control and communication validation for safety applications. Software design techniques are used with all FPU modules in order to provide diagnostic pathways for confirmation [

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The purpose of this document is to act as both an overview and outline for the typical diagnostic validation process to be used on all FPU components.

2.0 REFERENCES

RS901-001-74	HFC-6000 FPGA Platform Diagnostic Requirement Specification
NUREG/CR-7006	Review Guidelines for Field-Programmable Gate Arrays in Nuclear Power Plant Safety Systems
RG 1.168	Verification, Validation, Reviews and Audits for Digital Computer Software Used In Safety Systems of Nuclear Power Plants.
RG 1.172	Software Requirements Specifications for Digital Computer Software Used in Safety Systems of Nuclear Power Plants.
WI-ENG-203	Development of Software/Firmware Design Specification

2.1 SPECIAL TERMS AND ABBREVIATIONS

AI	Analog Input
AO	Analog Output
CCA	Circuit Card Assembly
CRC	Cyclic Redundancy Check
DI	Digital Input
DO	Digital Output
DPM	Dual Port Memory
F-Link	FPGA based C-Link
FPGA	Field Programmable Gate Array
FPU	FPGA Processing Unit
FSM	Finite State Machine
HPI	HFC Peripheral Interface
I/O	Input/Output
LED	Light Emitting Diode
MBPS	Mega-bytes Per Second
PCB	Printed Circuit Board
PLL	Phase Locked Loop

3.0 TECHNICAL DESIGN

3.1 SYSTEM ARCHITECTURE

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Figure 1. Typical FPU system Diagram

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3.2 COMMUNICATION INTERFACES

The diagnostic processing module relies on the following communication interfaces:

3.2.1 HPI – HFC Peripheral Interface

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Figure 2. HPI write operation

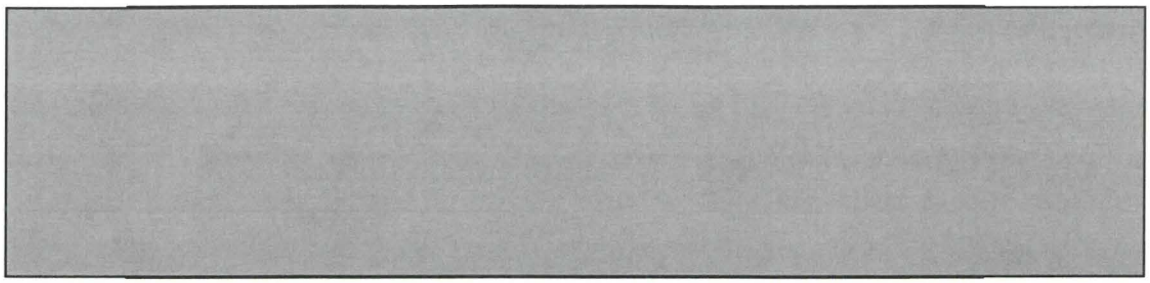

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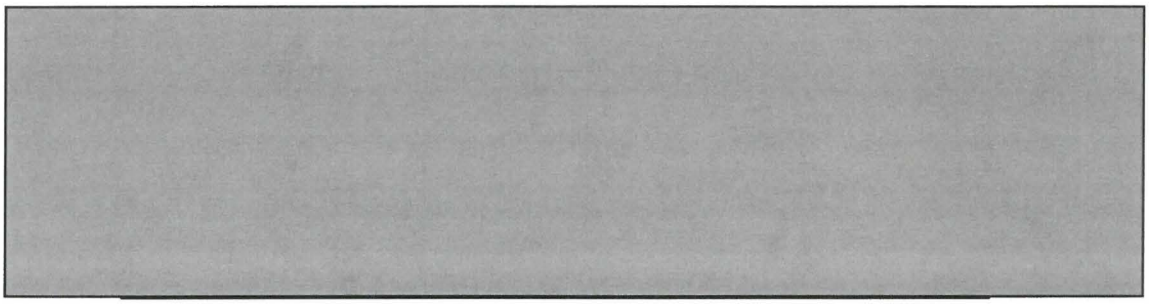
Figure 3. HPI read operation



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3.2.2 DPM interface – Dual Ported Memory interface to DDB data

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3.2.3 Discrete Module Ports

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3.3 TIMING REQUIREMENTS

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3.4 ACTIVATION

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3.5 DESIGN METHODOLOGY

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3.6 SOFTWARE STRUCTURE

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3.6.1 Design Description

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3.6.1.1 Main State Machine

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3.6.1.2 Startup Initialization task

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3.6.1.3 Check ADIO task

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3.6.1.4 Check FLCOI task

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3.6.1.5 Check Heartbeat task

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3.6.1.6 State Timeout processing

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3.6.1.7 Control signal generation

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3.6.2 Data Structures

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Table 1. HPI Semaphore Command Reference

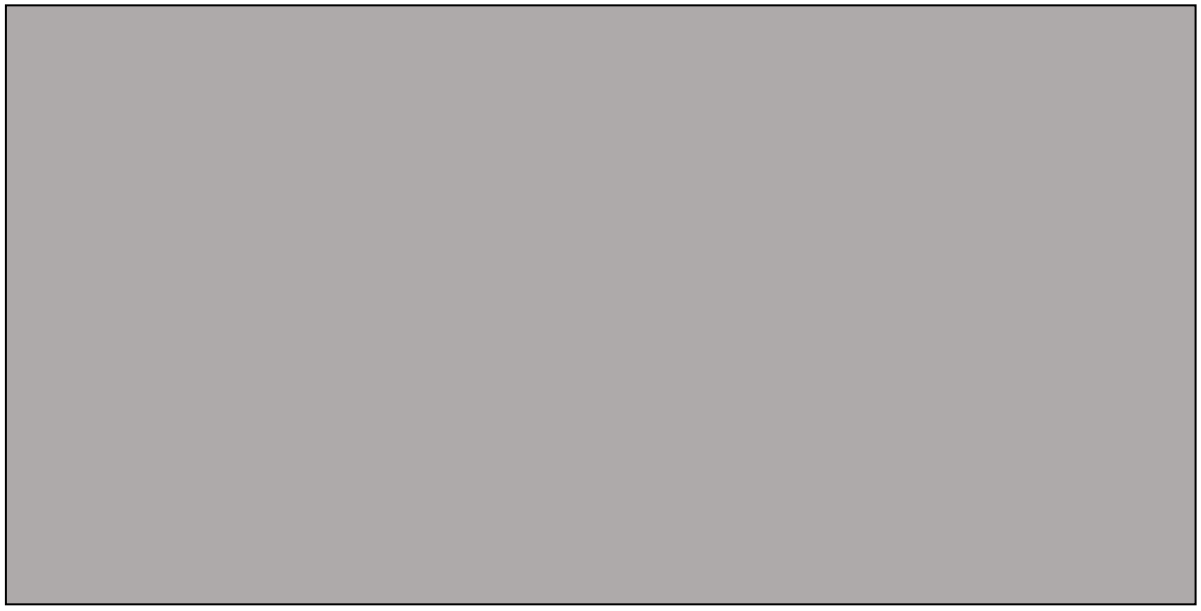

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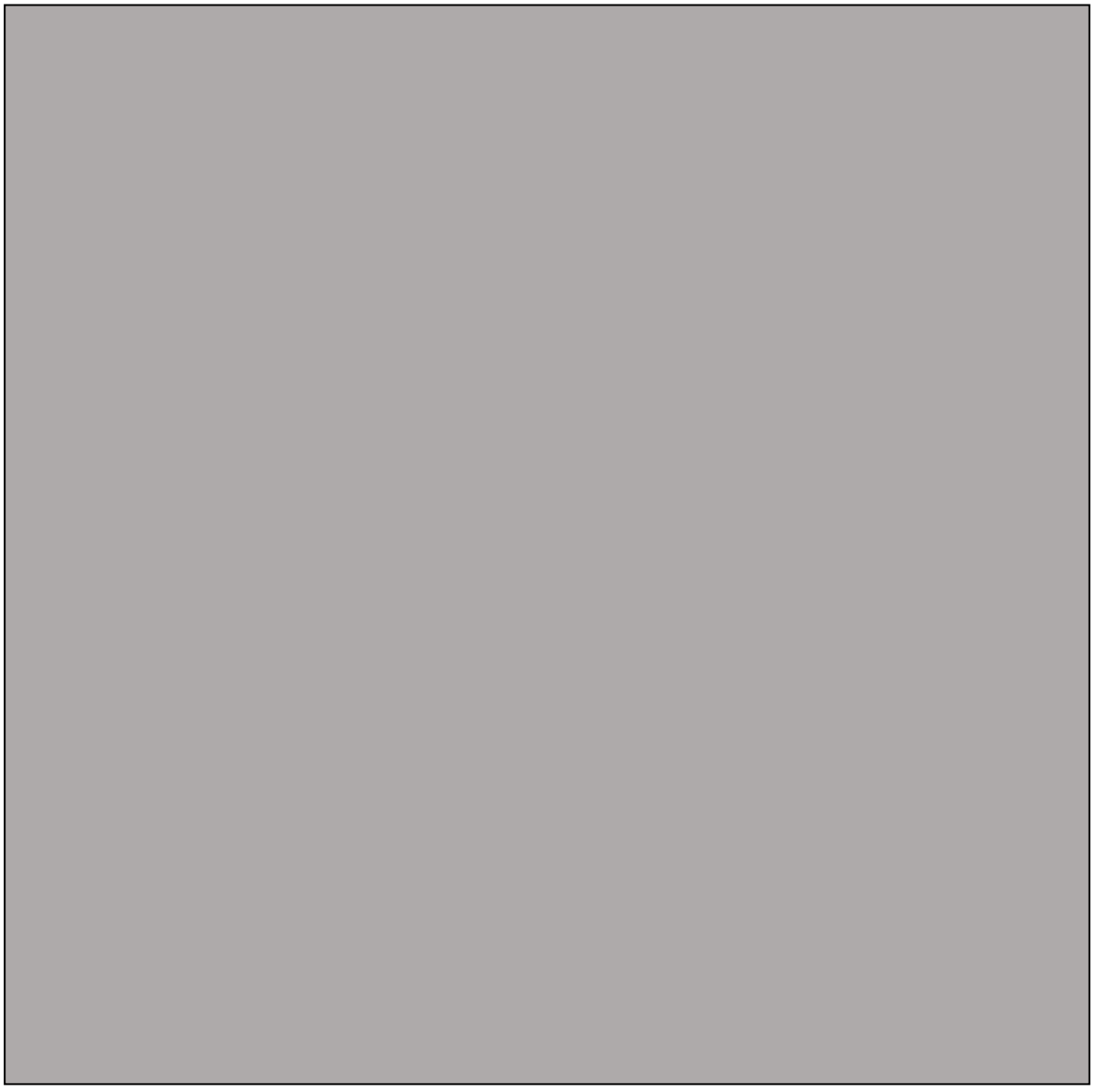
Table 2. HPI Heartbeat/Head Section Memory Configuration



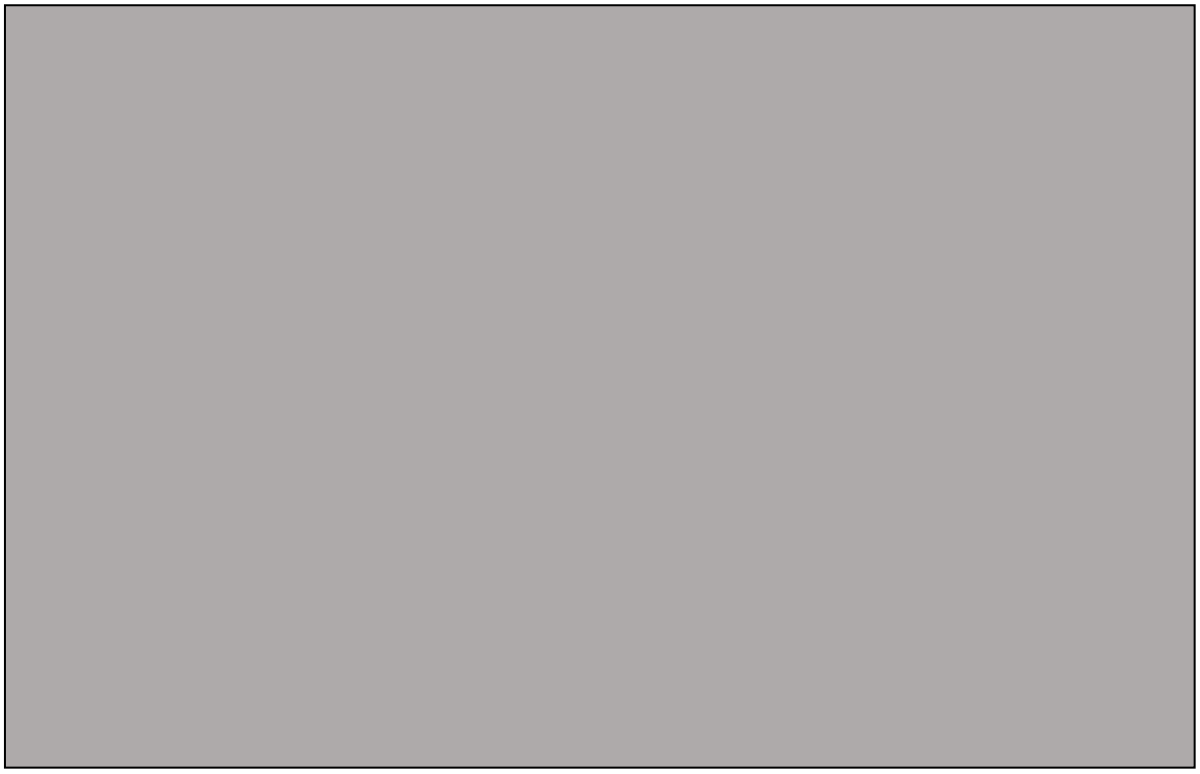
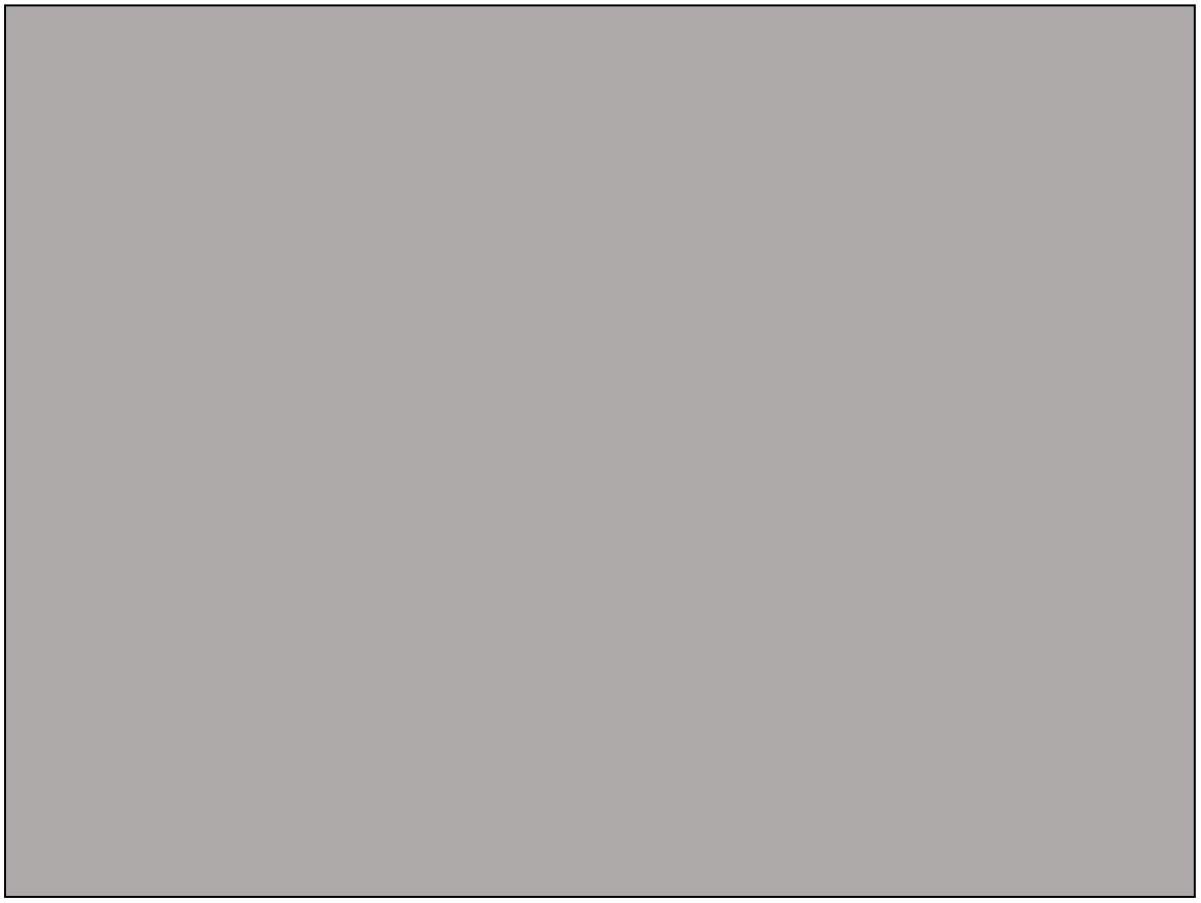


Table 3. HPI RQ Data Memory Configuration



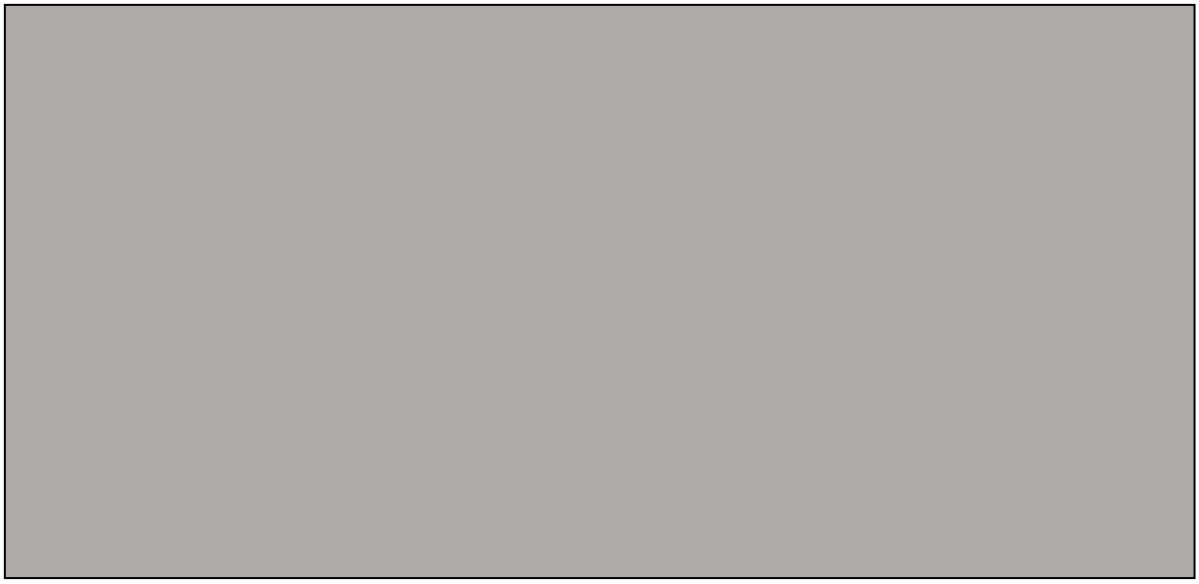


Table 4. ADIO Memory Configuration

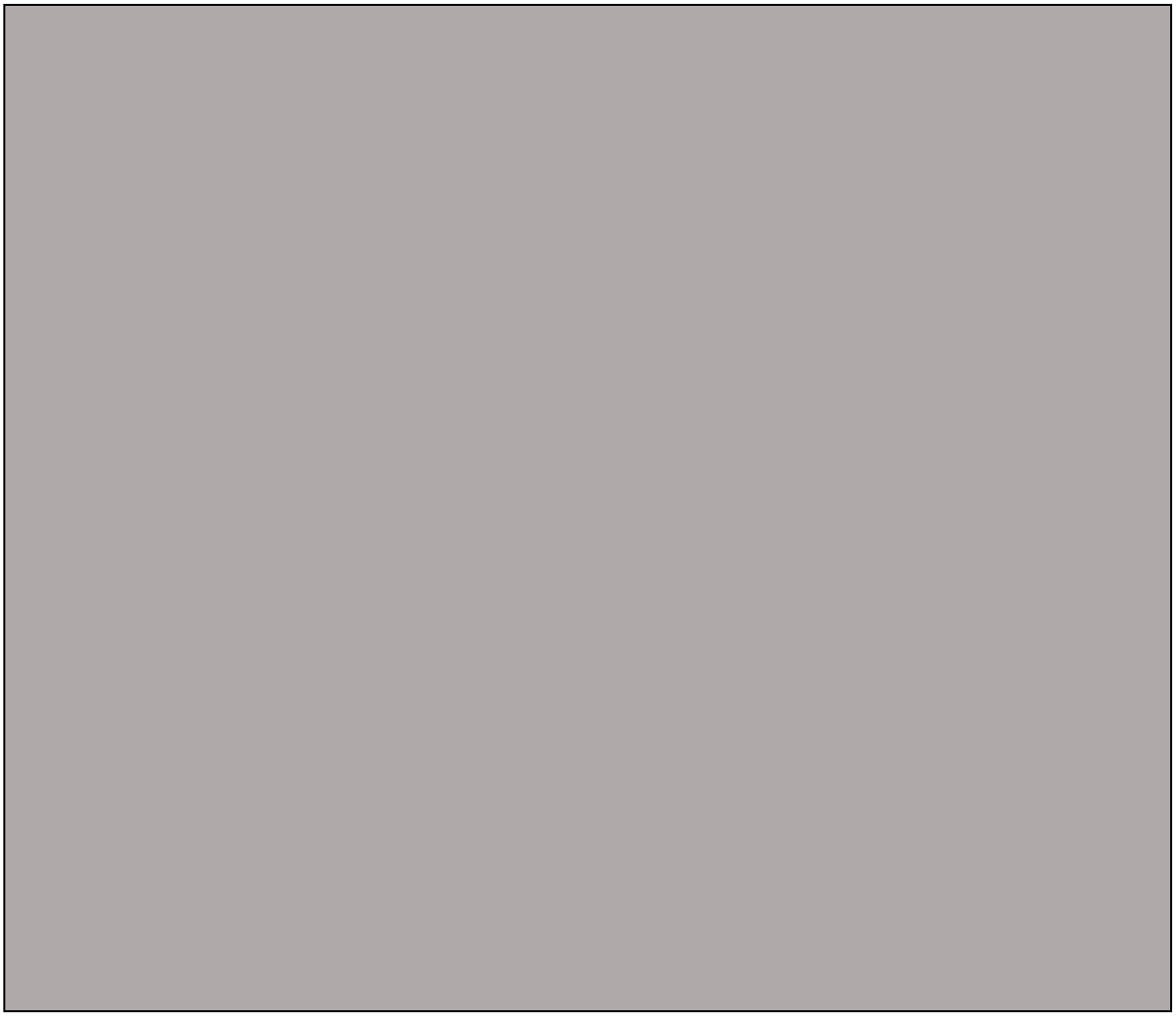


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Table 5 shows the RQ DPM memory configurations. [

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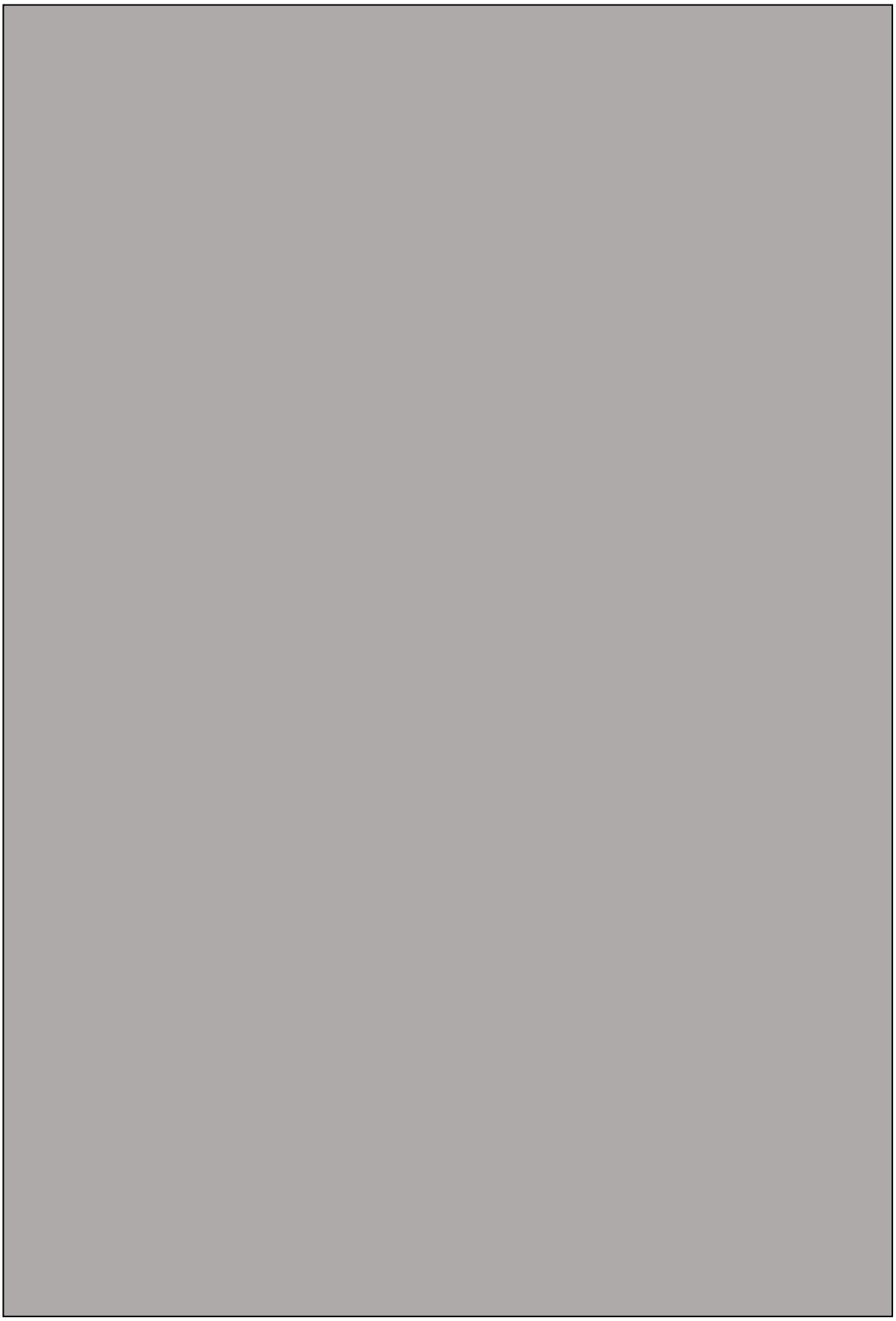
Table 5. RQ DPM memory configuration



3.6.3 Data Flow

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3.6.4 Process Control Concept

Figure 4 is the main state machine[

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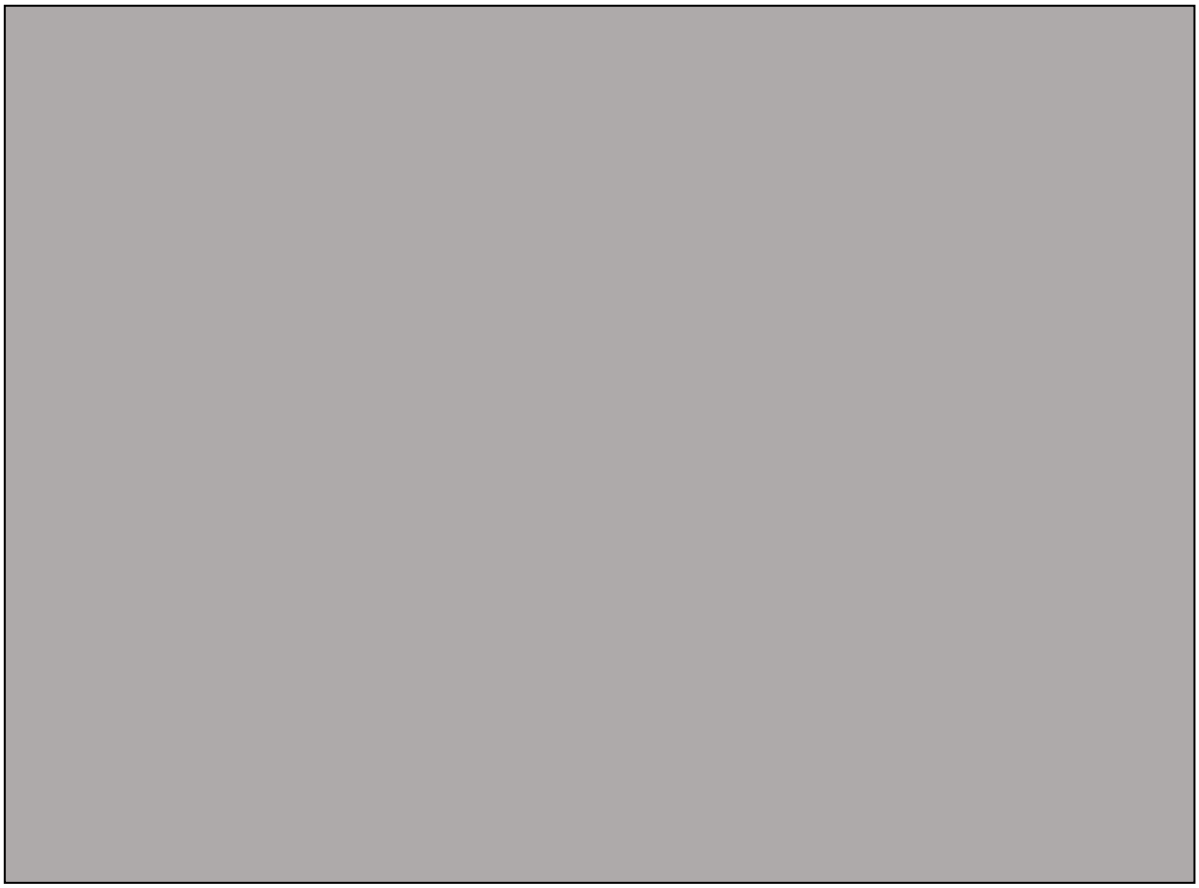
Figure 4. Diagnostic module State Machine



4.0 SOFTWARE MODULES

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4.1 DIAGNOSTIC PROCESSING MODULE

4.1.1 Source File & Interface

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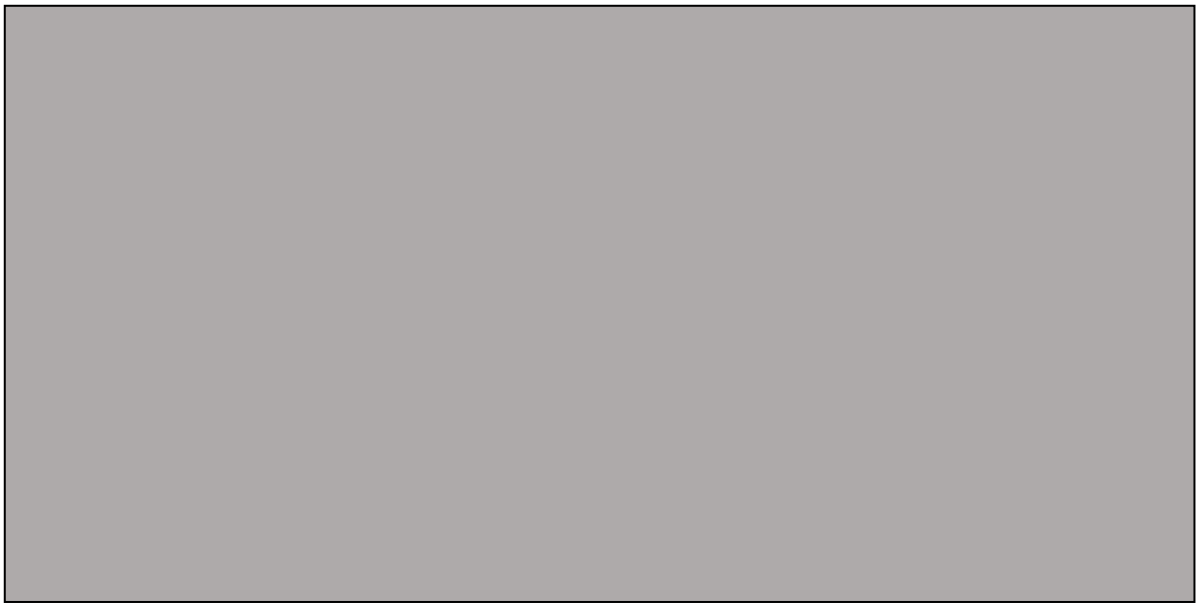
Figure 5. Diagnostic Processing Module I/O



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4.1.1.1 System Interface

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4.1.1.2 Voltage Monitoring

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4.1.1.3 Digital I/O image

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4.1.1.4 Flag Data, RQ image

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4.1.1.5 Sister Reset

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4.1.1.6 Fail-Safe control

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4.1.1.7 F-Link enable and data ready

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4.1.2 Main State Machine

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4.1.2.1 SYSTEM_RESET

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4.1.2.2 INIT_1, INIT_2

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4.1.2.3 CHK_V

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4.1.2.4 CHK_E

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4.1.2.5 TIME_CLR

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4.1.2.6 CHK_PROC

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4.1.2.7 CHK_ADIO

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4.1.2.8 CHK_FLCOI

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4.1.2.9 CHK_HB

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4.1.2.10 WDT_RTN

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4.1.2.11 WDT_MEM

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4.1.2.12 FAIL_BOARD

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4.1.3 Startup task

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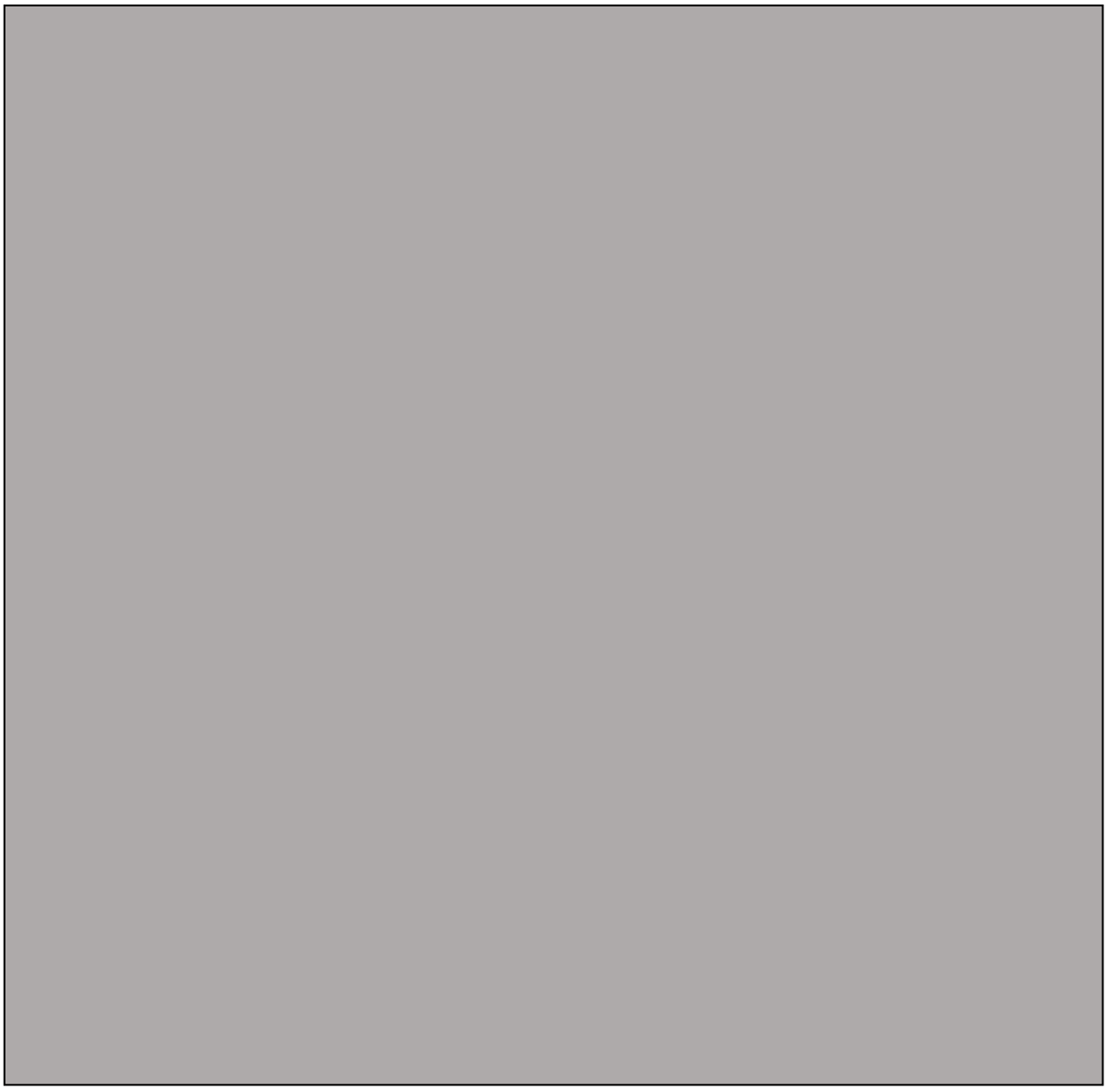
Figure 6. Start Up task flow chart



4.1.4 Check ADIO task

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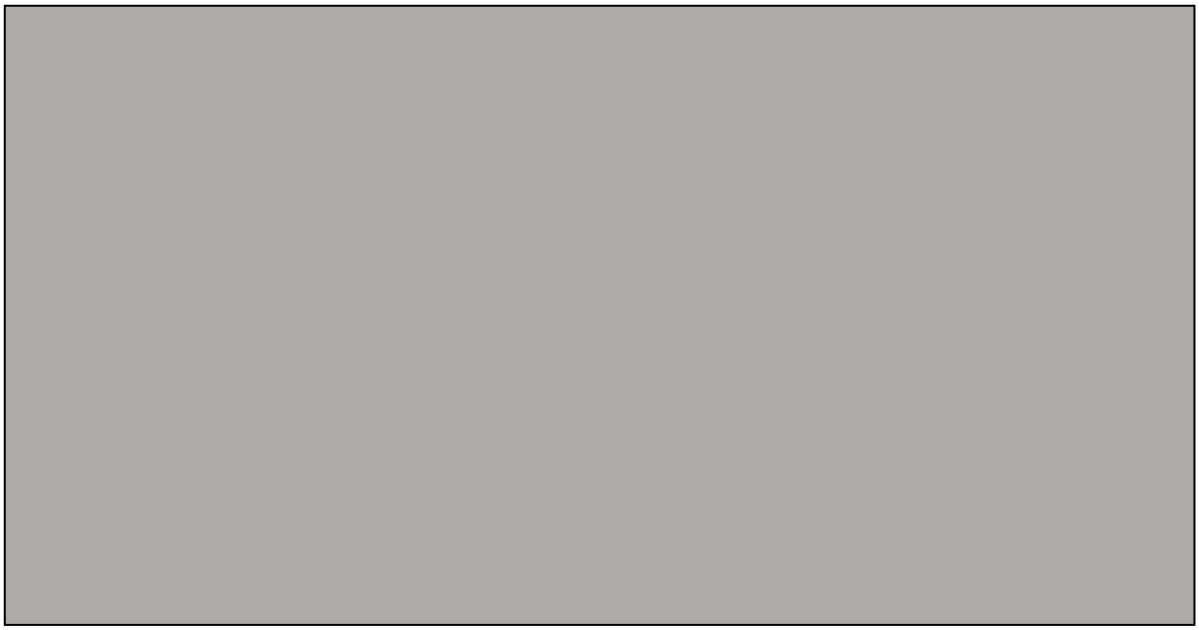
Figure 7. Check ADIO flow chart



4.1.5 Check FLCOI task

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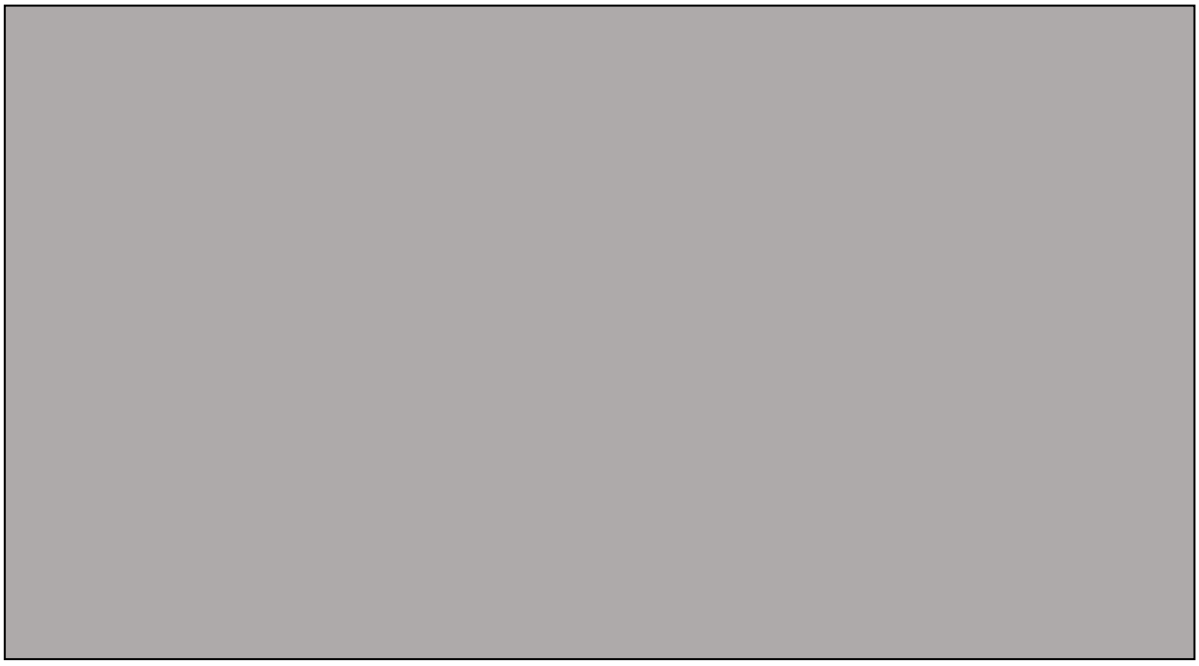
Figure 8. Check Flcoi flow chart



4.1.6 Check Heartbeat task

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Figure 9. Check Heartbeat flow chart

4.1.7 Exception Handling (State Time Out)

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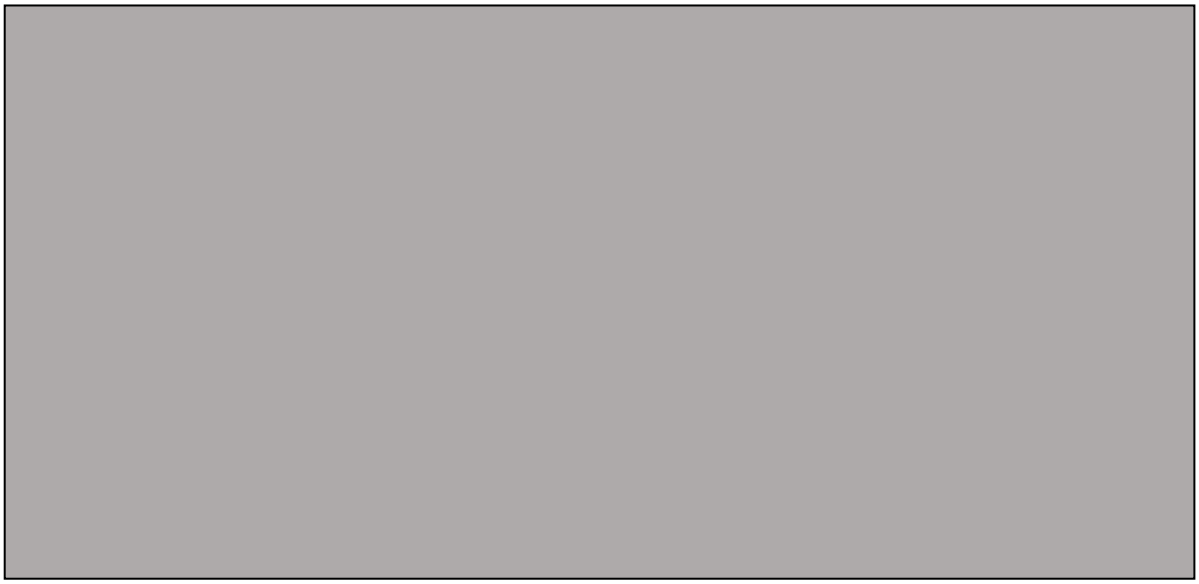
Figure 10. State Time Out flow chart 1

Figure 11. State Time Out flow chart 2



4.1.8 Diagnostic Error output code

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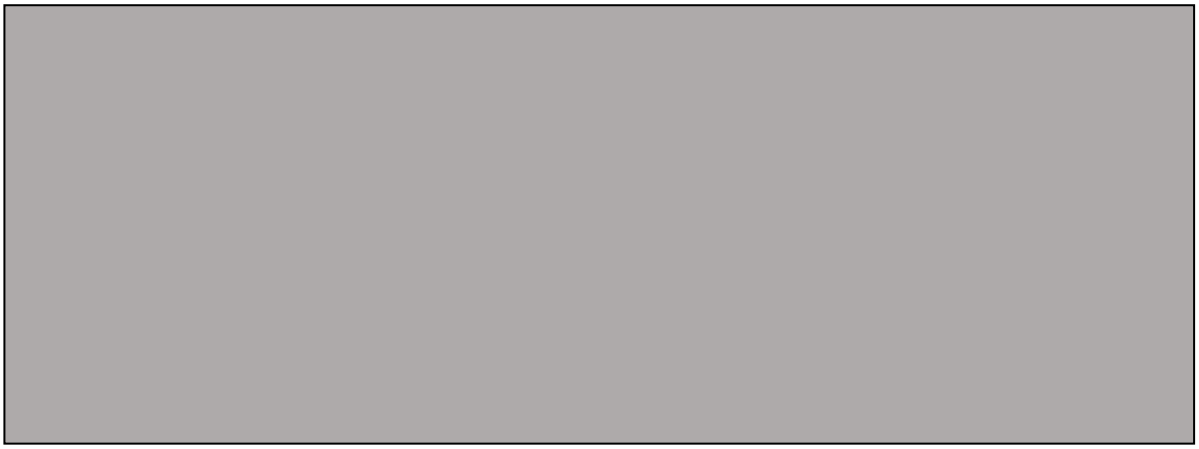
Table 6. Diagnostic Error Output Code Reference



4.2 FPU SYSTEM START UP SEQUENCE

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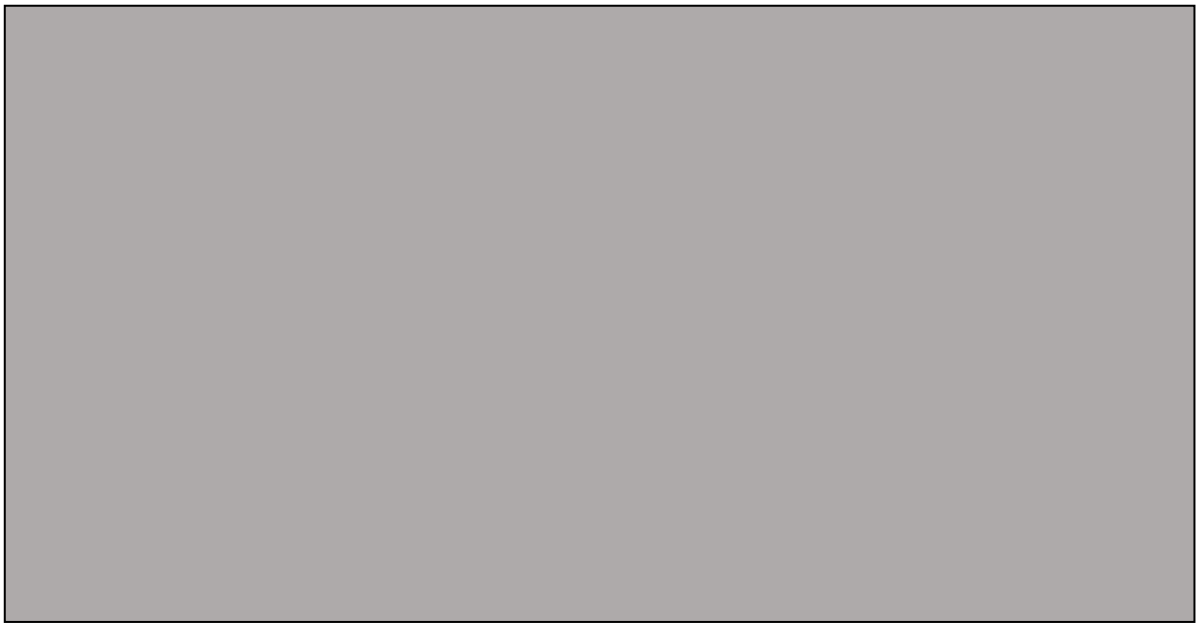
Figure 12. Diagnostic Processing Reset Sequence



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4.3 DIAGNOSTIC PROCESS OPERATION

The following sections describe the operation of the diagnostic processing module during different phase.

4.3.1 Initialization diagnostics

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4.3.2 Run Time diagnostics

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