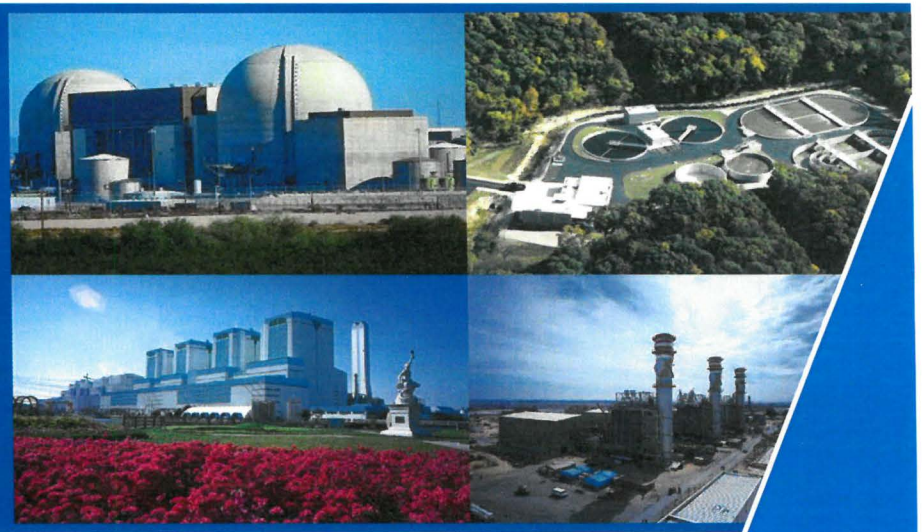
DOOSAN HF Controls

HFC-FPGA

NRC DISCUSSION 11-21



Innovation Leadership Service

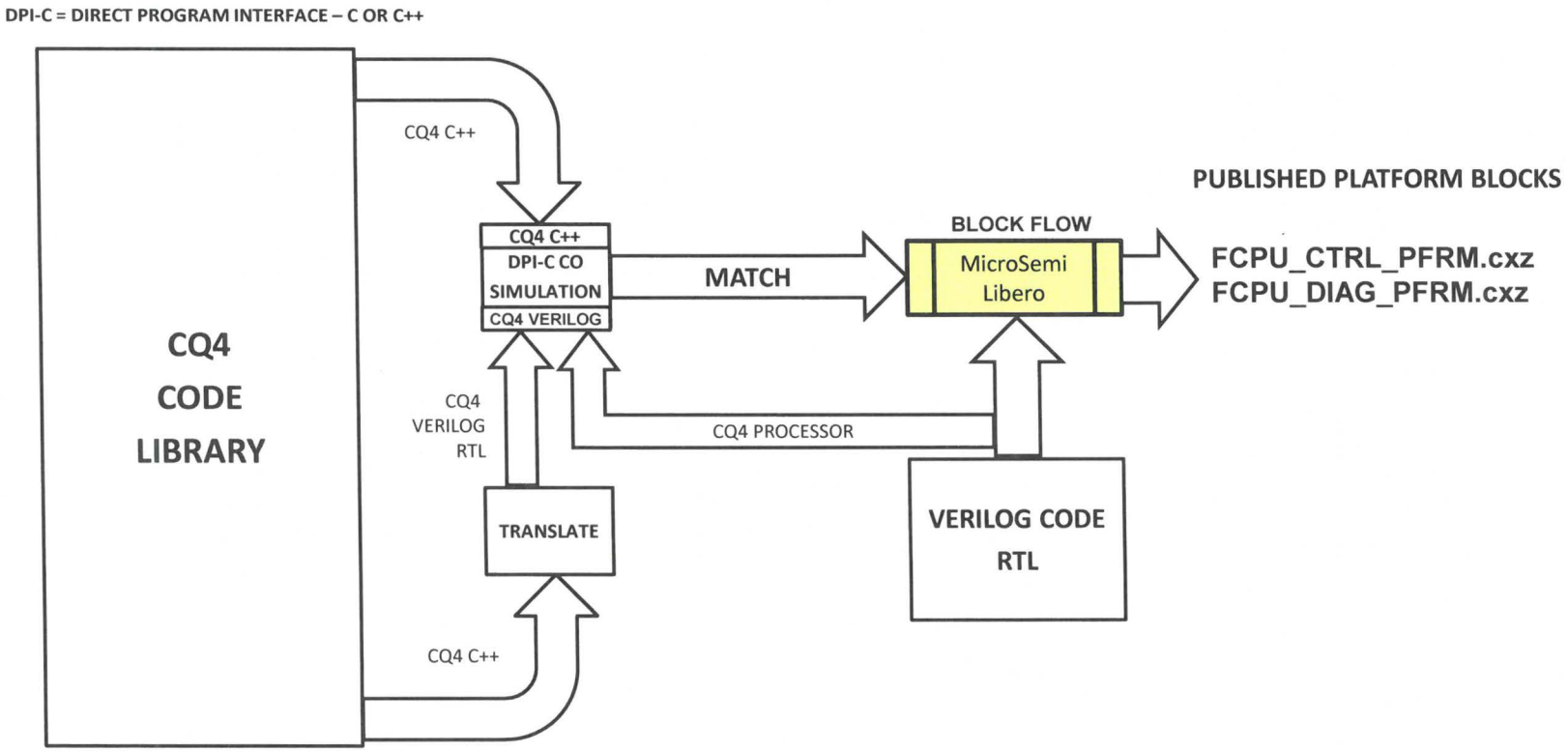
AGENDA – HFC PROPOSED

- HFC COMPANY
- SYSTEM TOPICS
  - HFC-FPGA AND PREVIOUS TR/AMENDMENT COMMONALITY
- HARDWARE TOPICS RELATED TO DOCKET ITEMS
  - INTERNAL FPGA ARCHITECTURE, INITIALIZATION, AND DATA FLOW
  - F-LINK/G-LINK OPERATION DETAILS
  - AI CALIBRATION
  - WATCHDOG
- STATUS OF OPEN DISCUSSION ITEMS
  - ITEMS WITH MORE INFORMATION REQUIRED
    - ITEMS TO CONTINUE IN DISCUSSION
    - ITEMS TO MOVE TO RAI STATUS
  - AGREEMENT ON CLOSED STATUS ITEMS

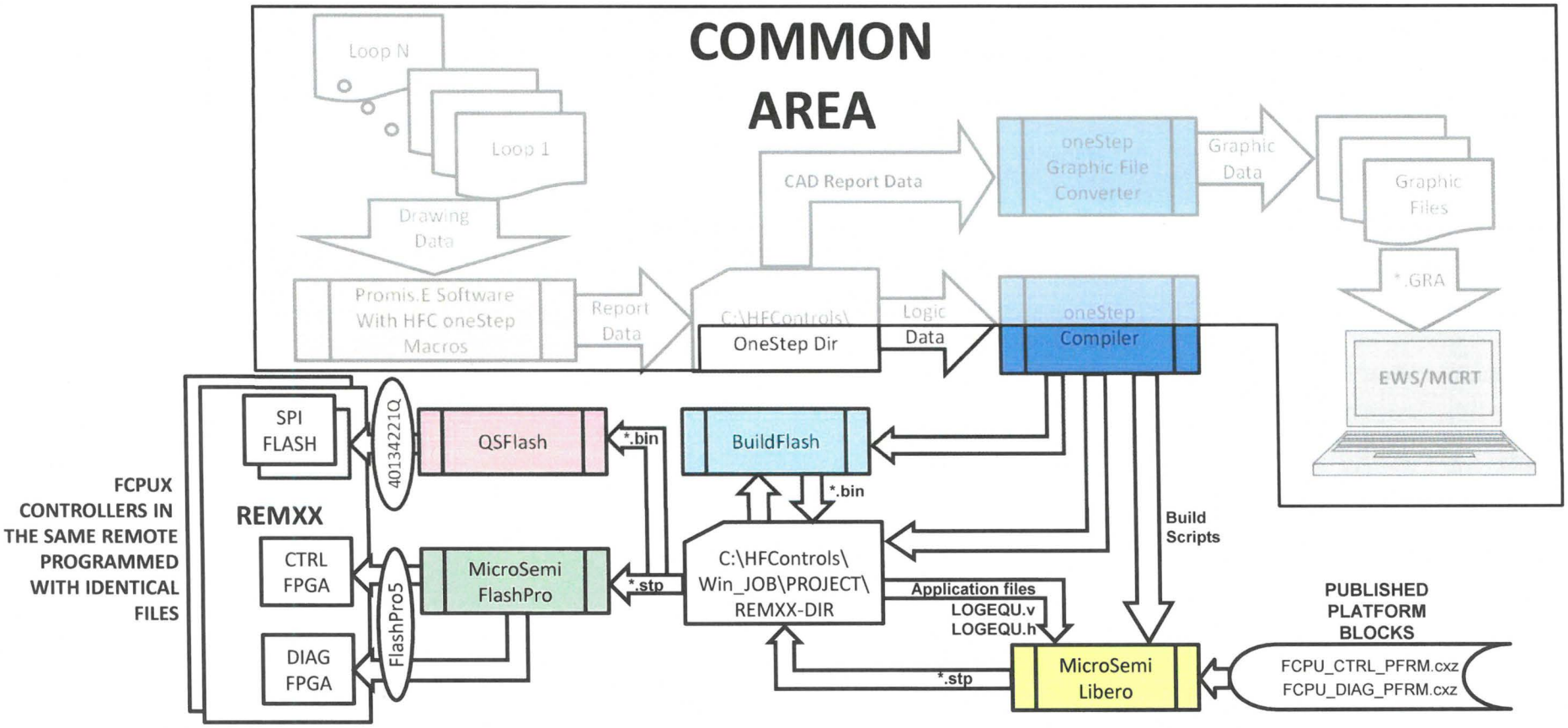
HFC-FPGA COMMONALITY WITH PREVIOUS TR

- NUCLEAR CONTROL MECHANICAL AND POWER IDENTICAL
  - CABINETS/BACKPLANES/POWER/NETWORK EQUIPMENT ETC
- I/O INTERFACE DESIGN – I/O ARE BASED ON EXTENSIVE EXPERIENCE IN INDUSTRIAL CONTROL, REDUNDANT FPGA'S REPLACE MICROPROCESSORS
- HFC-FPGA SYSTEM WAS DEVELOPED UNDER LIFECYCLE PROCESS
- CQ4 CODE LIBRARY LEVERAGED IN CQ4 RTL DEVELOPMENT
  - CQ4 VERILOG RTL DERIVED FROM C++ SOURCE
  - DPI-C TEST BENCH USED TO CO-SIMULATE C++ AND VERILOG RTL TO VERIFY RTL FUNCTIONALITY
- TOOLS AND APPLICATION PROCESS – USE DRAWING DEFINED APPLICATION AS SOURCE FOR PROCESS CONTROL
  - APPLICATION CODE DERIVED FROM SCHEMATIC DRAWINGS
    - LOGEQU.V – VERILOG THAT DESCRIBES BOOLEAN LOGIC RELATIONSHIPS FROM THE APPLICATION
    - SPI FLASH BINARY FILE – MEMORY INITIALIZATION FILES DERIVED FROM THE APPLICATION
      - BLOCK VALUE MEMORY – STORAGE LOCATION FOR APPLICATION PROCESSING, F-LINK, TIMERS, TRANSFER TABLES
      - BLOCK DATA MEMORY – CQ4 BLOCK SEQUENCE, OPTIONS FOR EACH CQ4 BLOCK
      - TIMER INITIALIZATION VALUES
- COMMUNICATION INTERFACES
  - F-LINK – MODIFIED C-LINK PROVIDES DETERMINISTIC COMMUNICATION BETWEEN CONTROLLER AND FPU IN AN FPGA NODE

HFC-FPGA COMMONALITY WITH PREVIOUS TR

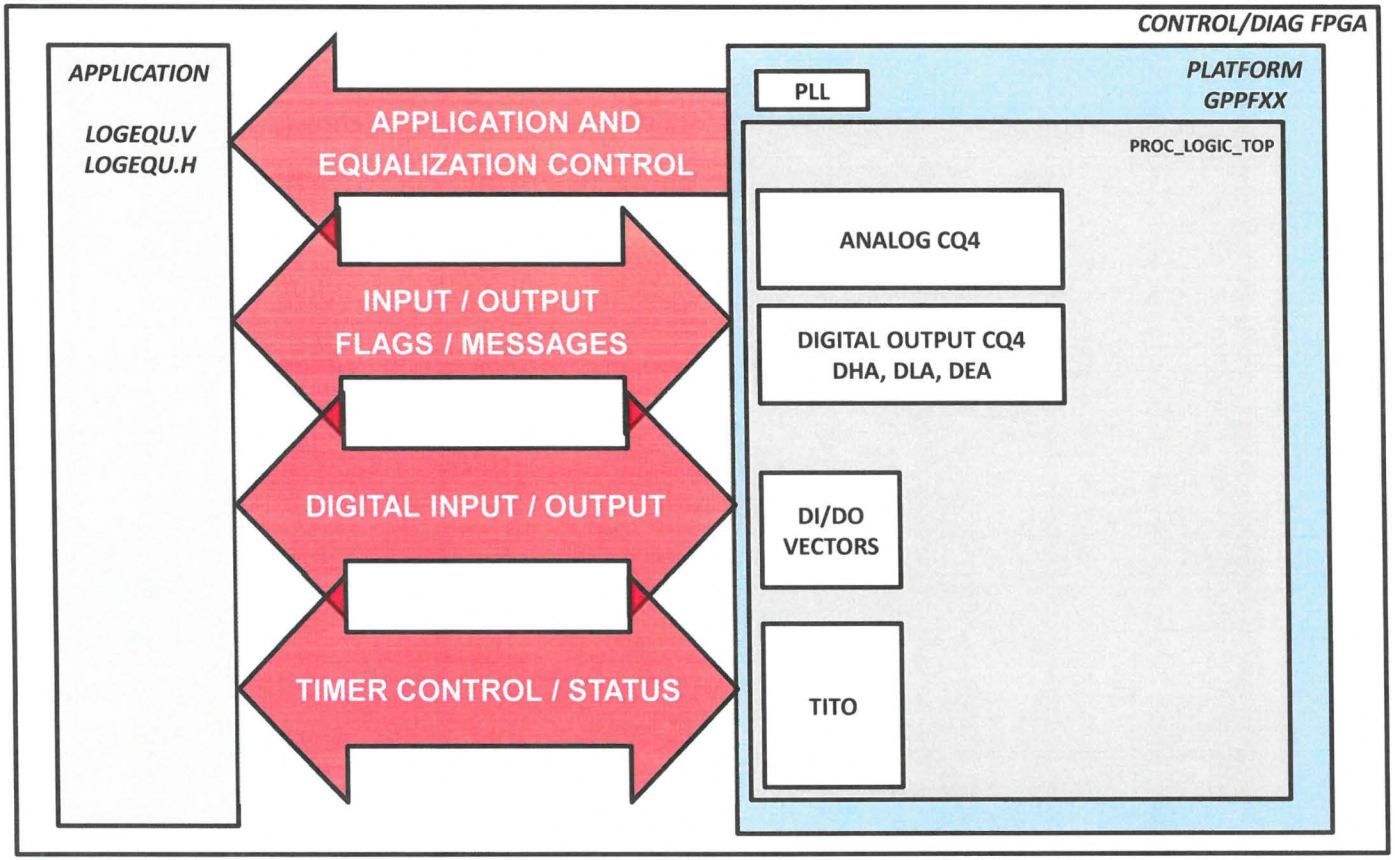


HFC-FPGA COMMONALITY WITH PREVIOUS TR



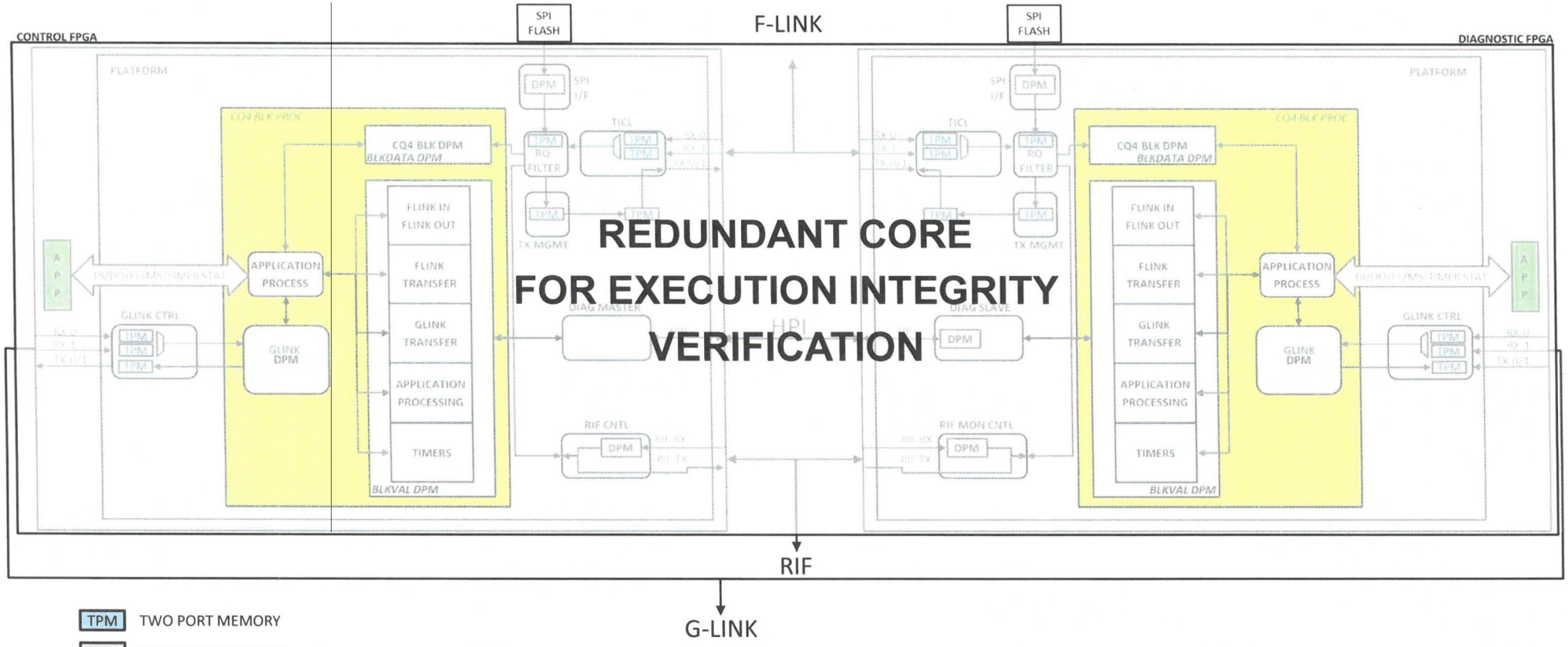
DOOSAN HF Controls

APPLICATION TO PLATFORM INTERFACE - FCPUX



FCPUX FPGA CORE ARCHITECTURE

RELEVANT TO: D-42



TPM TWO PORT MEMORY

DPM DUAL PORT MEMORY

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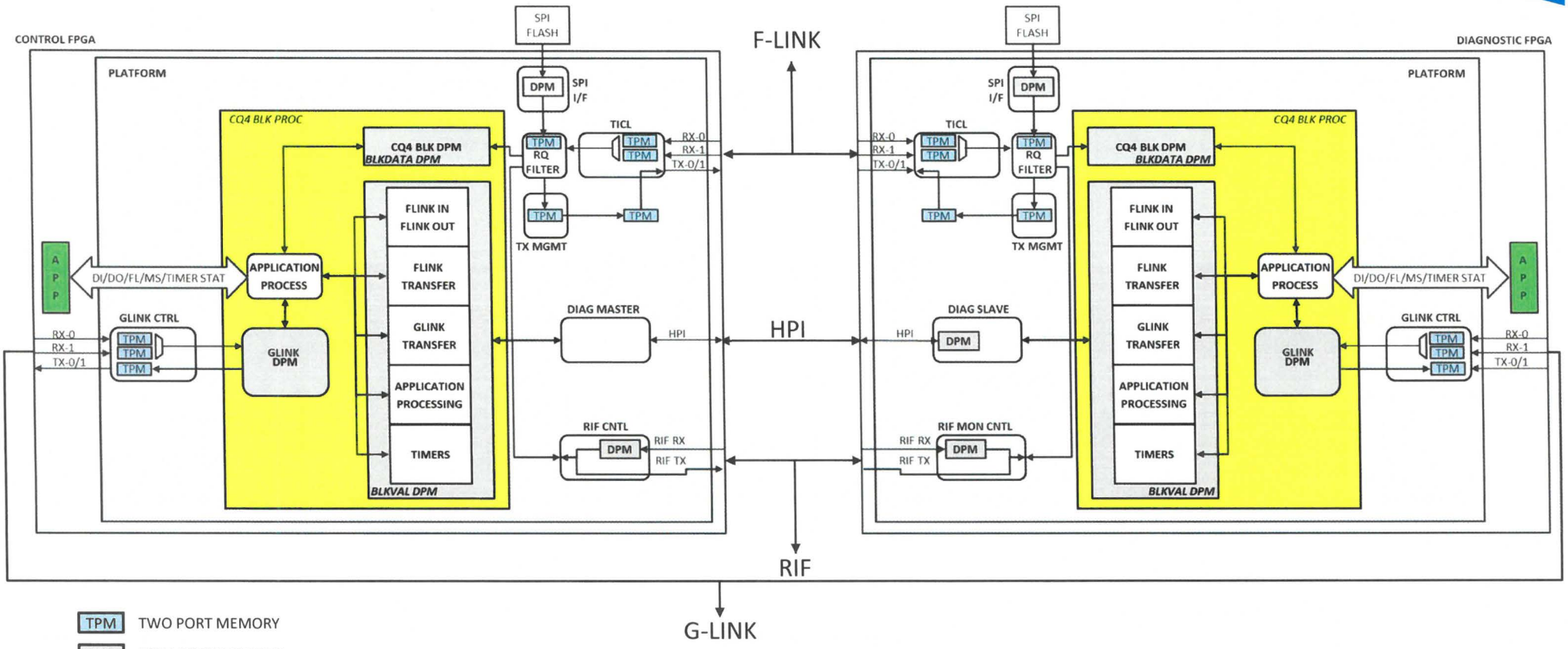
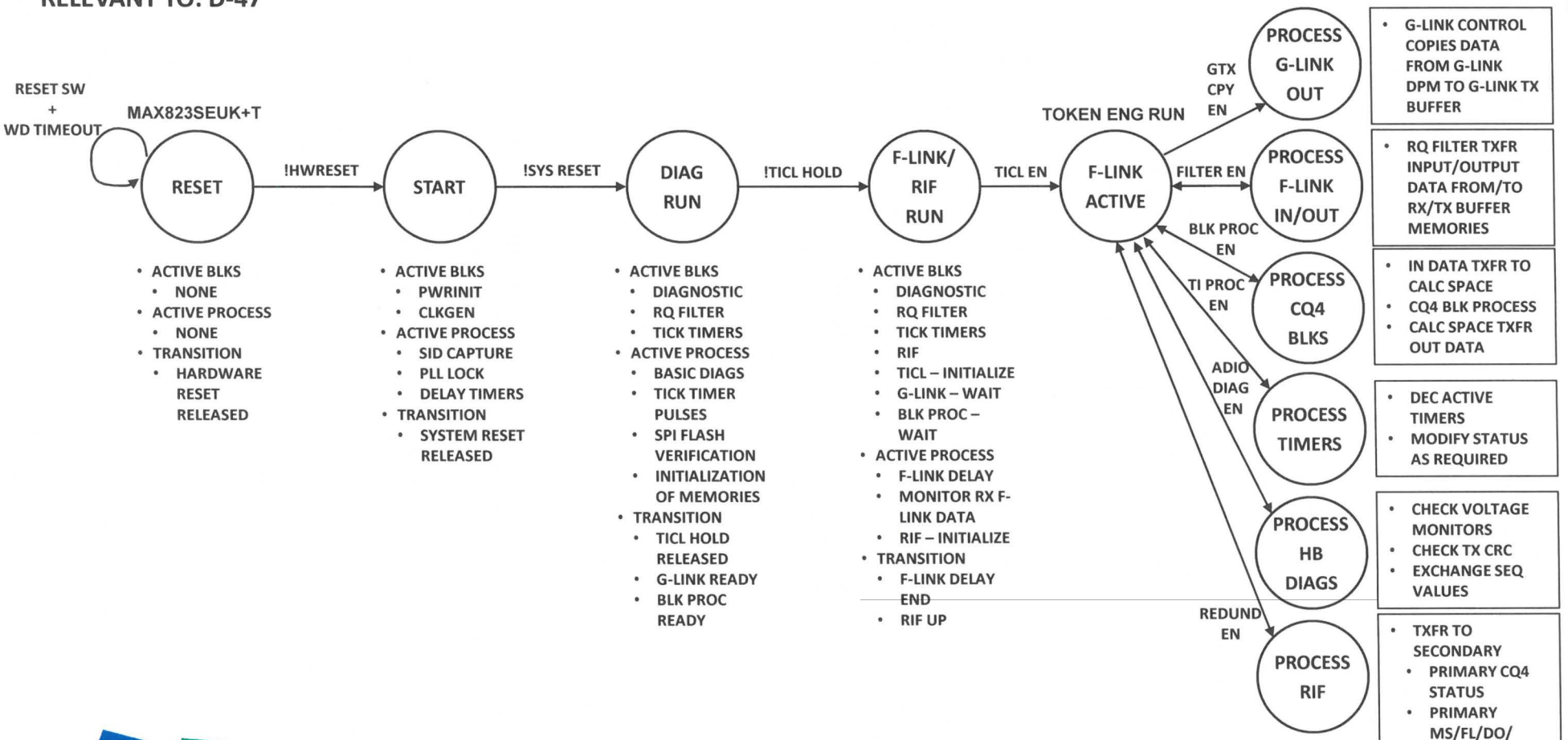
FCPUX DETAILED MEMORY BLOCK DIAGRAM

RELEVANT TO: D-47



HFC-FPGA SYSTEM STARTUP AND OPERATION

RELEVANT TO: D-47



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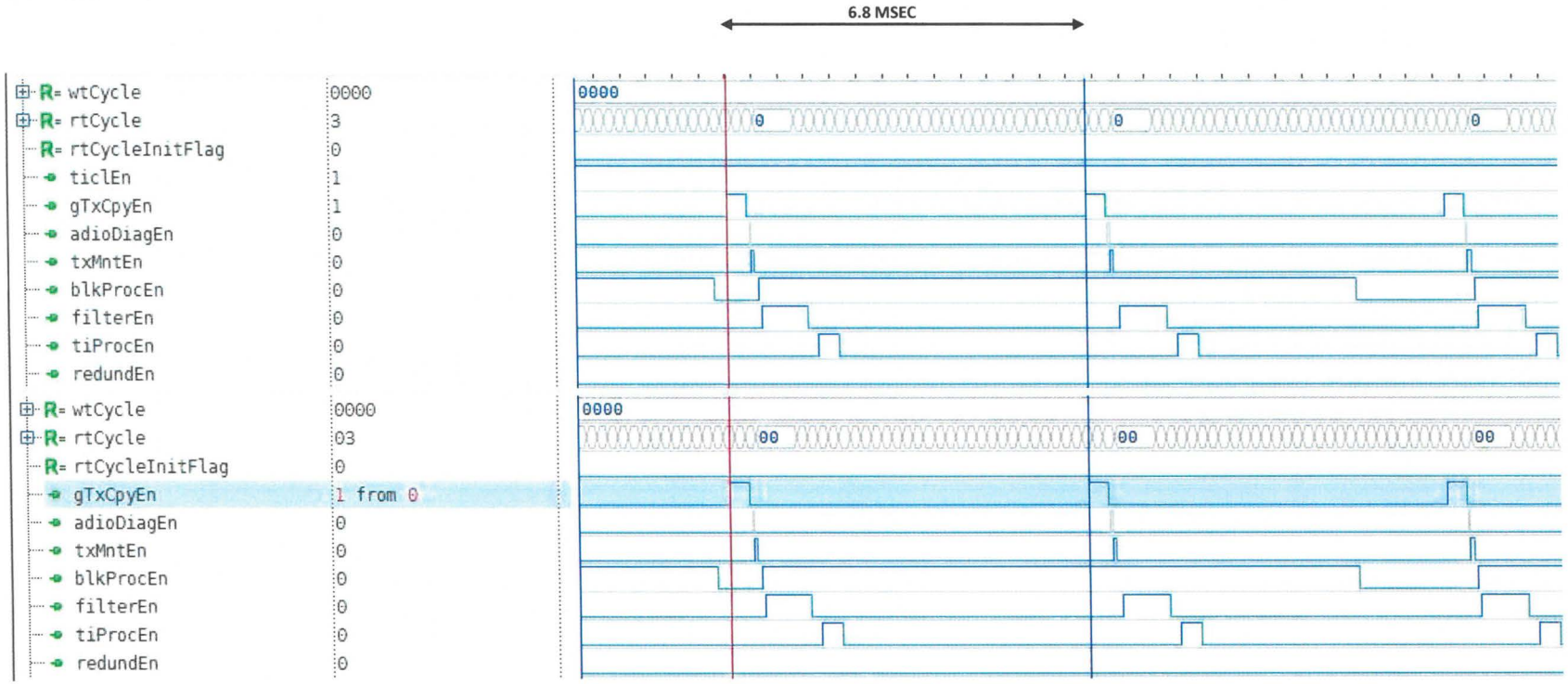
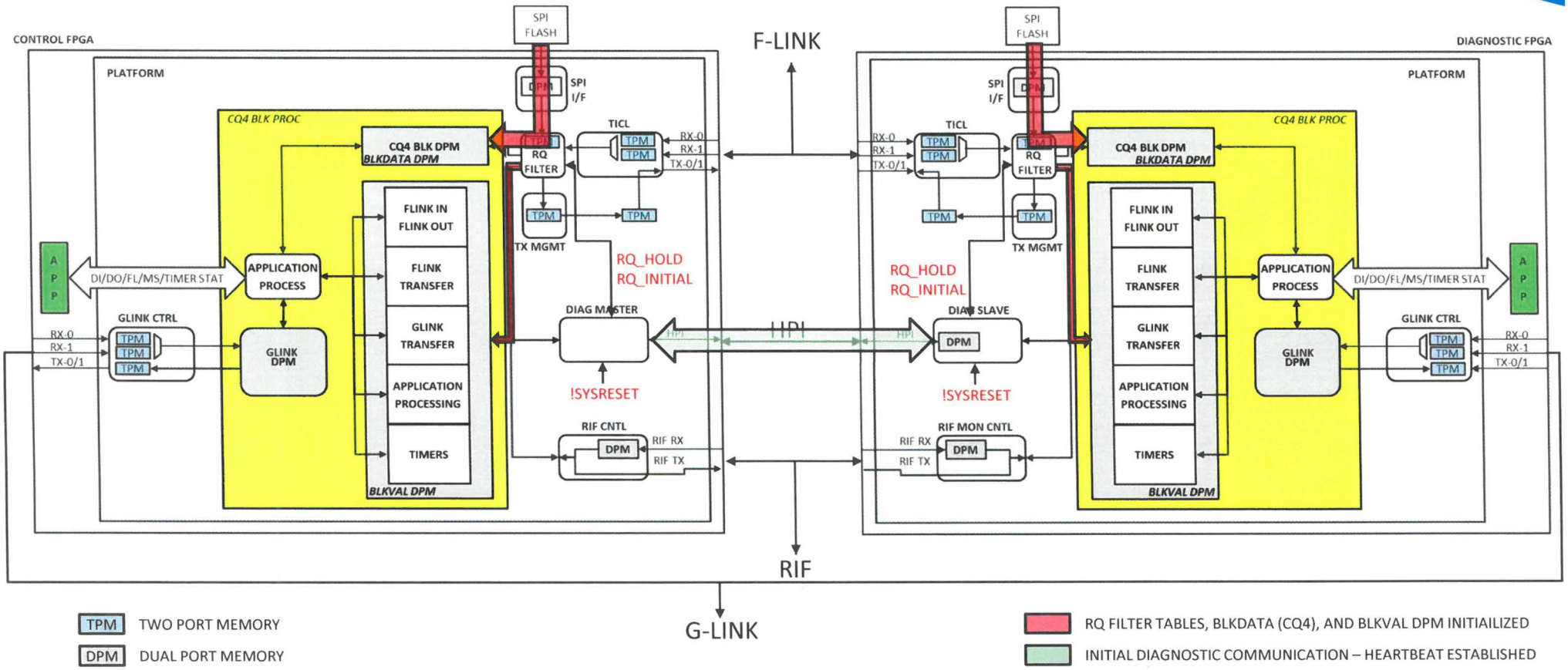
HFC-FPGA FCPUX TOKEN ENGINE OPERATION

RELEVANT TO: D-47



HFC-FPGA SYSTEM INITIALIZATON DURING BOOTUP

RELEVANT TO: D-47



TPM TWO PORT MEMORY

DPM DUAL PORT MEMORY

RQ FILTER TABLES, BLKDATA (CQ4), AND BLKVAL DPM INITIAILIZED

INITIAL DIAGNOSTIC COMMUNICATION – HEARTBEAT ESTABLISHED

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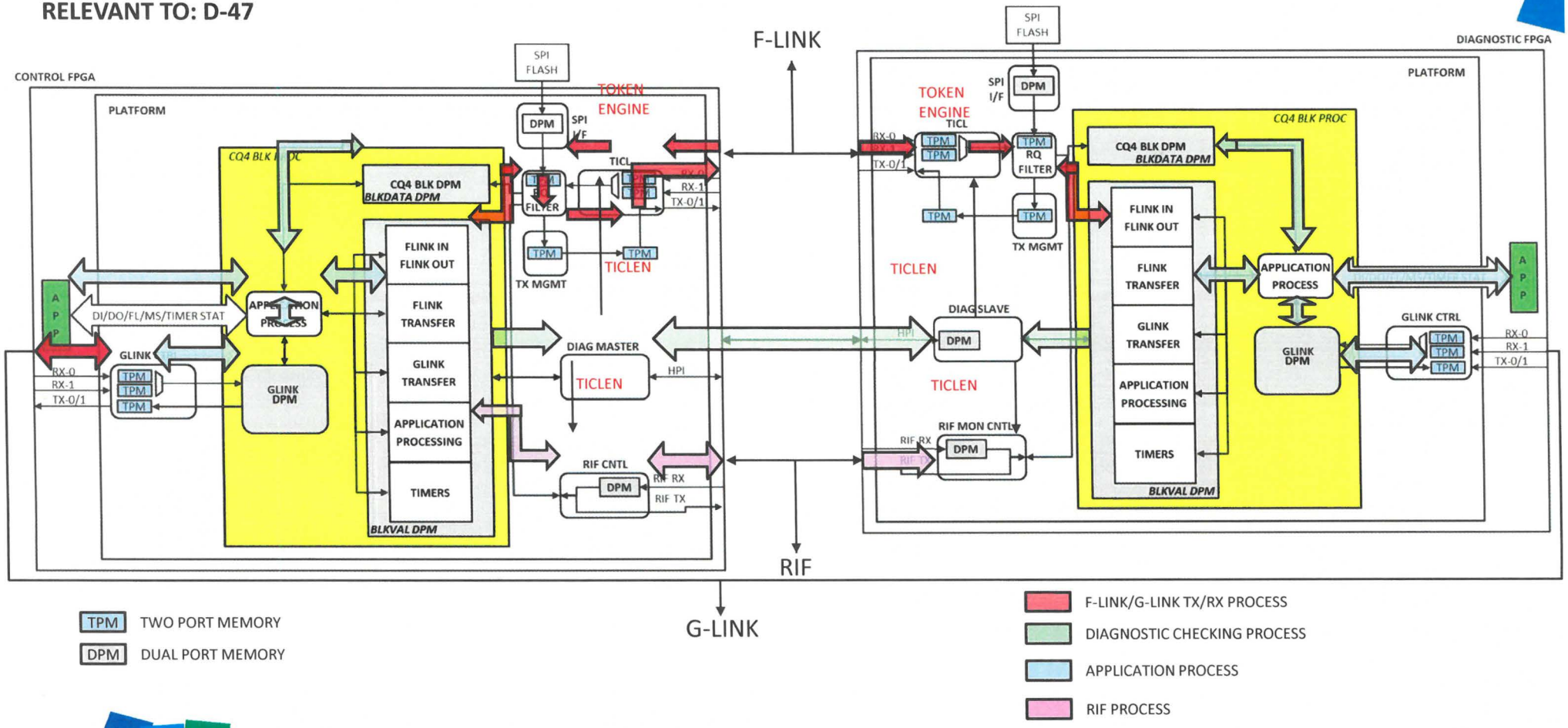
HFC-FPGA SYSTEM OPERATION – SYSUP

RELEVANT TO: D-47



TPM TWO PORT MEMORY

DPM DUAL PORT MEMORY

F-LINK/G-LINK TX/RX PROCESS

DIAGNOSTIC CHECKING PROCESS

APPLICATION PROCESS

RIF PROCESS

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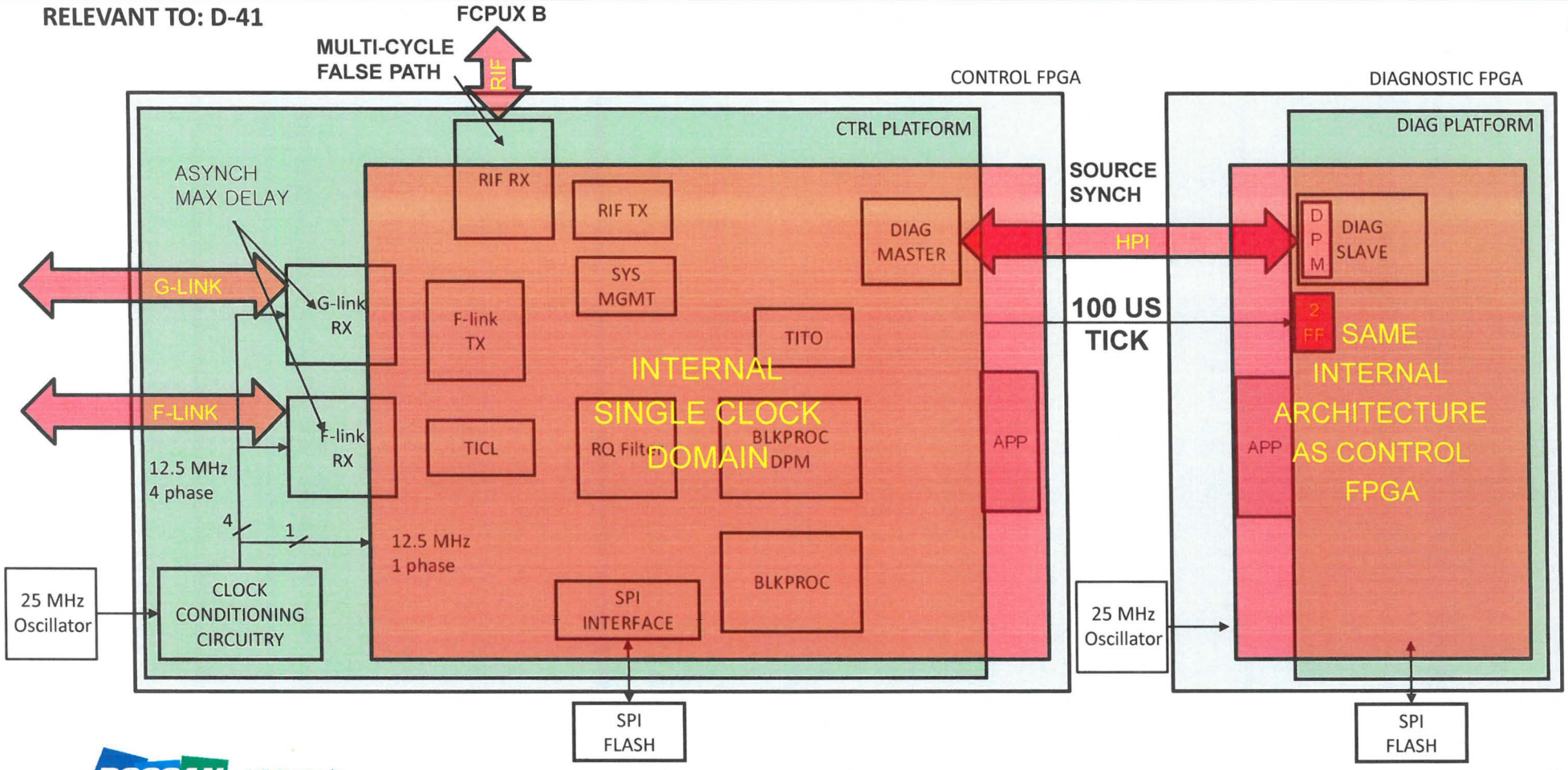
HFC-FPGA FCPUX CLOCK DOMAIN DIAGRAM



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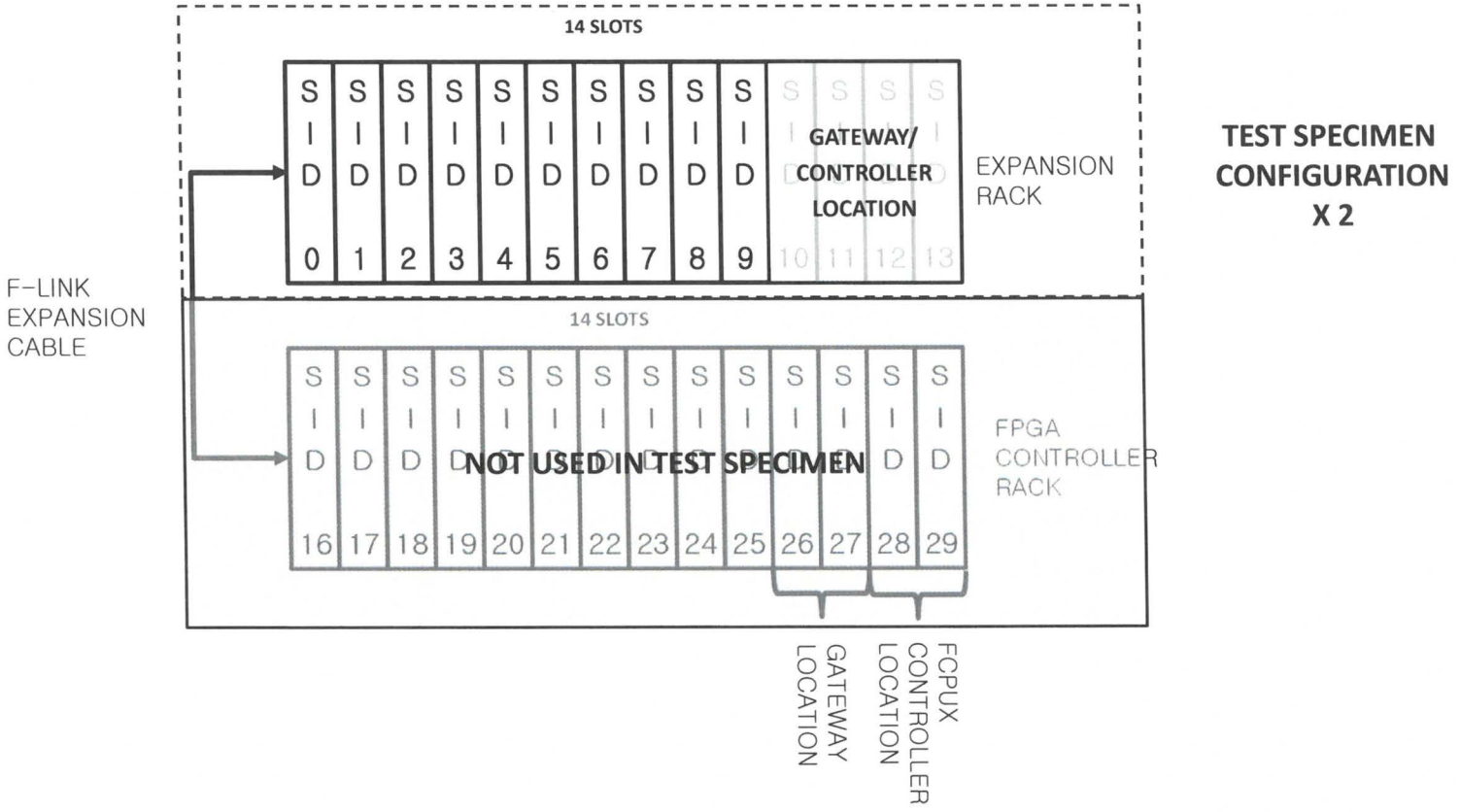
STATION ID VS SLOT – DS901-001-91 FIGURE 4

RELEVANT TO: D-25

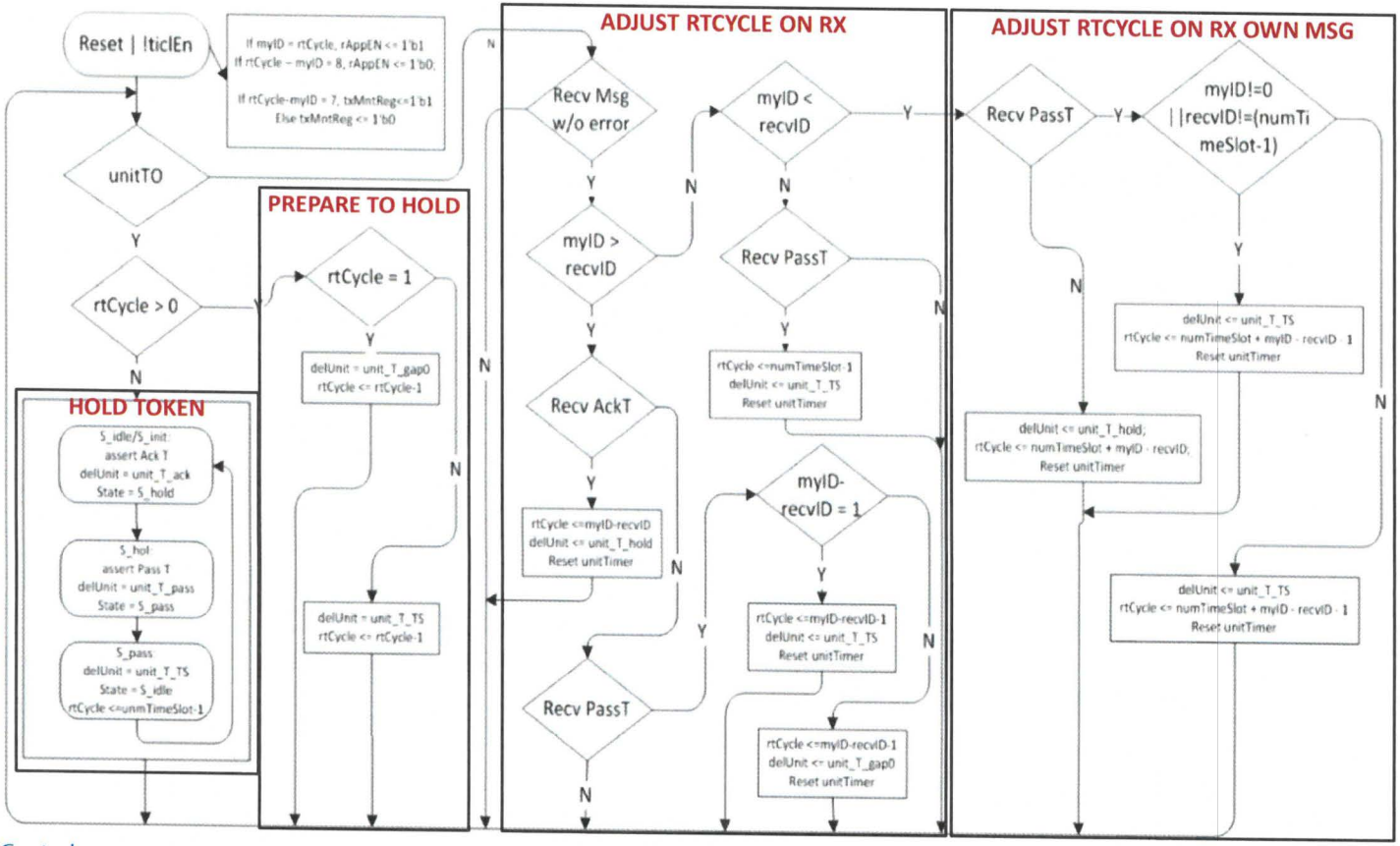


TEST SPECIMEN CONFIGURATION X 2

F-LINK CYCLE – DS001-007-01 FIG 13

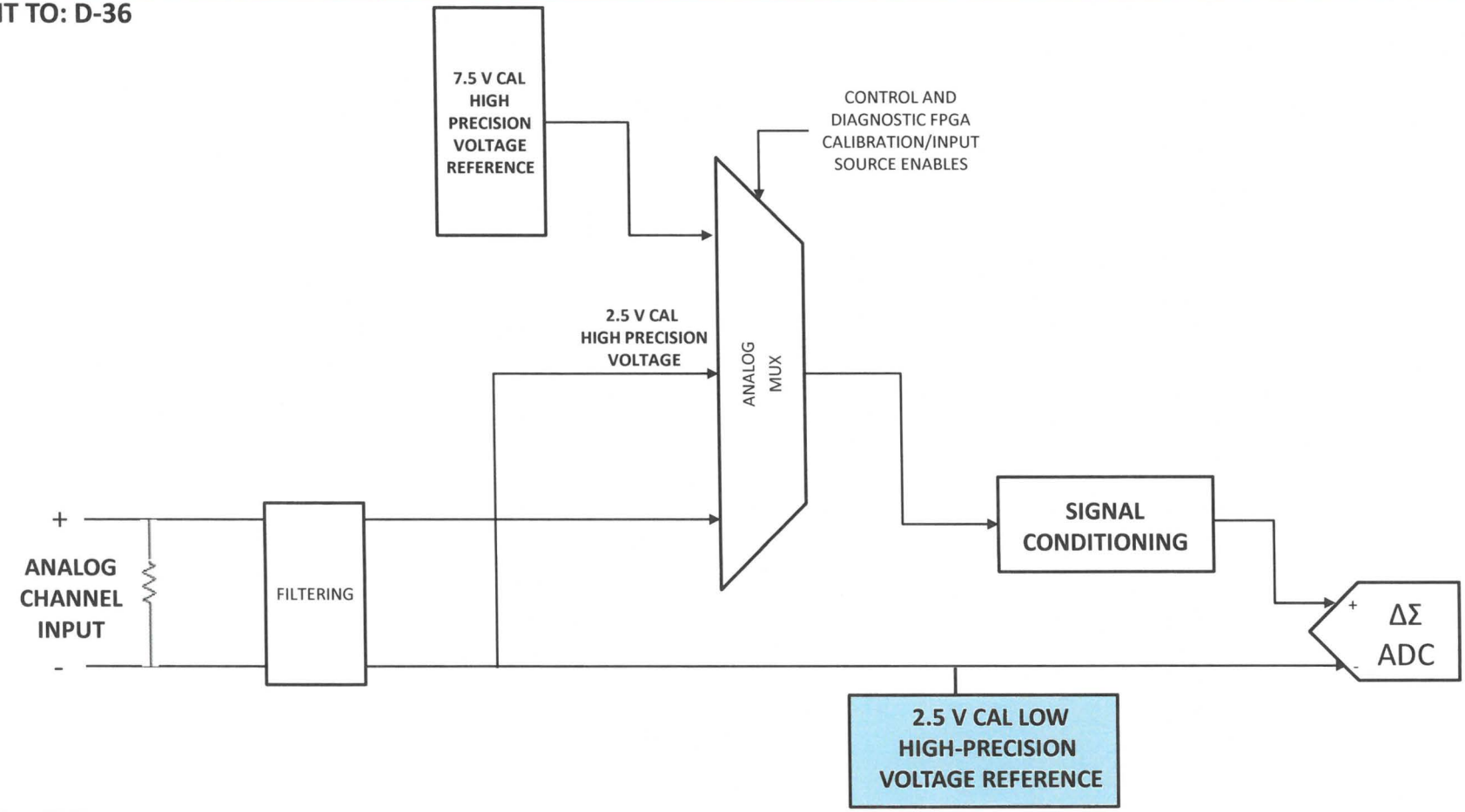
RELEVANT TO: D-13, D-16, D-53

F-LINK TX (HOLD TOKEN) = RTCYCLE = 0



ANALOG INPUT CALIBRATION

RELEVANT TO: D-36



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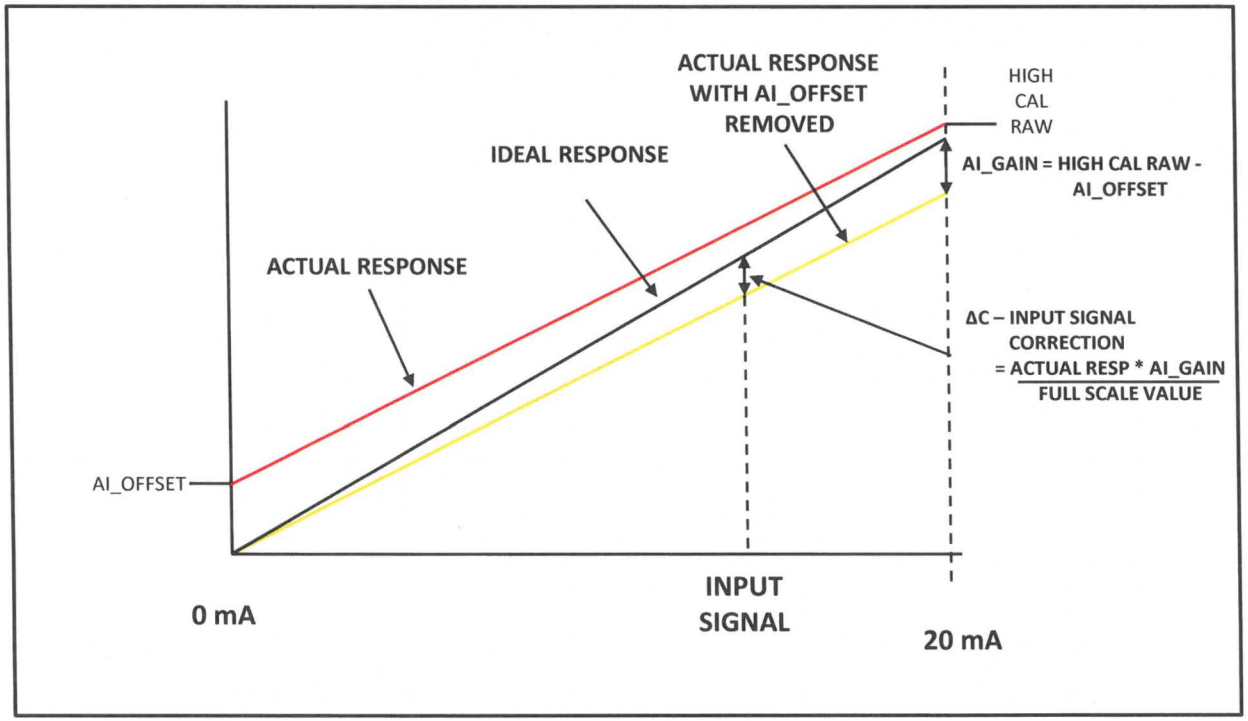
HFC ADC AI GAIN AND OFFSET CORRECTION ALGORITHM

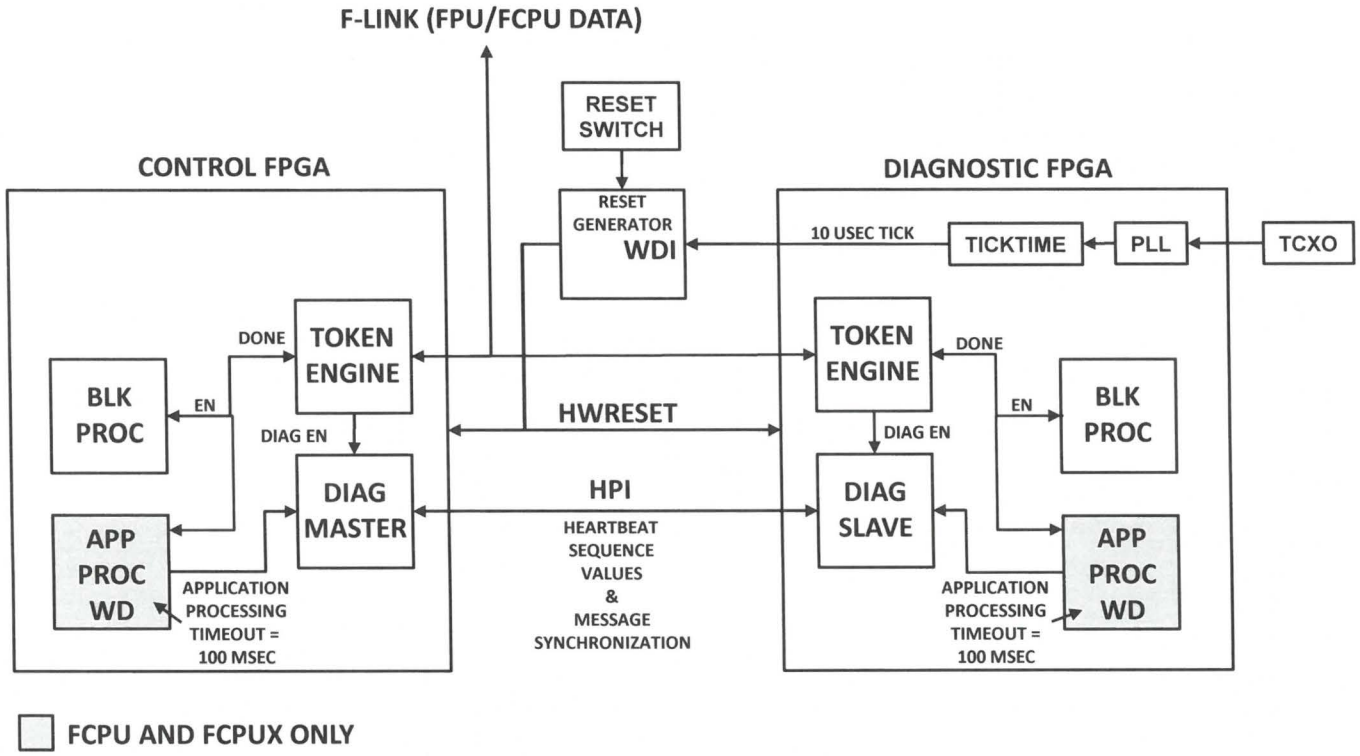
RELEVANT TO: D-36



OUTPUT VALUE = ACTUAL RESPONSE – AI_OFFSET + ΔC

HFC-FPGA WATCHDOG MECHANISMS – UPDATE TR FIG 4, 6

RELEVANT TO: D-13

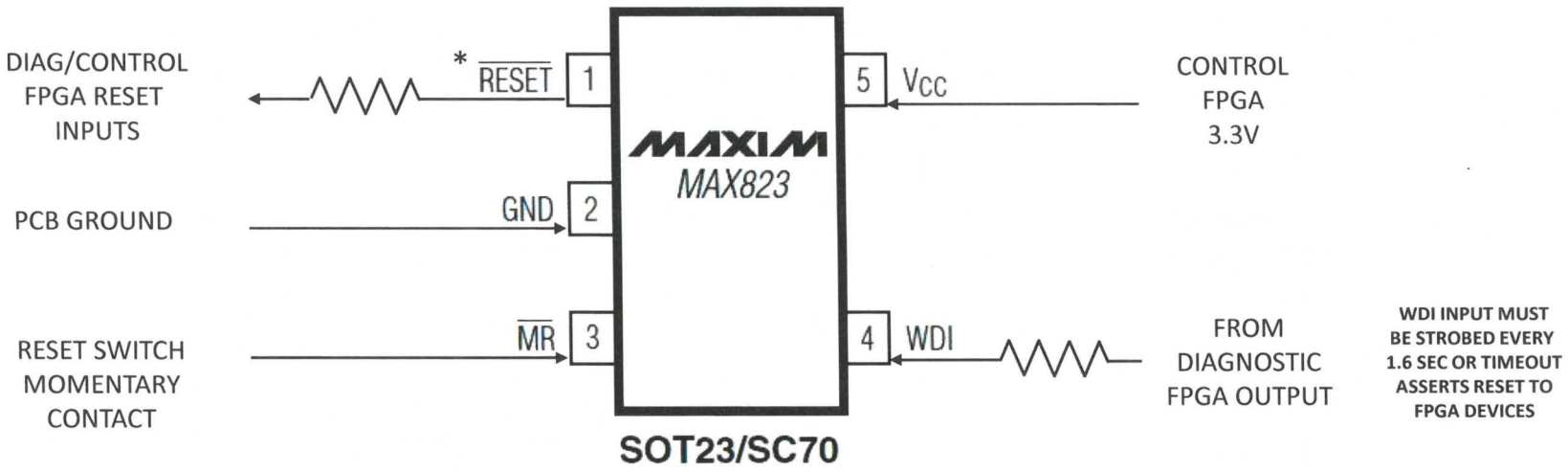


HFC-FPGA WATCHDOG DETAIL

RELEVANT TO: D-6, D-11

* RESET ACTIVE FOR 140ms MIN AFTER
POWER ON (VCC > 2.93V TYP) OR WDI TIMEOUT

MAX823SEUK+T



SOT23/SC70

DOOSAN HF Controls

QUESTIONS/COMMENTS/ACTIONS

- QUESTIONS
  1. X
- COMMENTS
  1. X
- ACTIONS
  1. X