



**HF Controls**

**HF CONTROLS CORPORATION  
HFC-FPGA Amendment 4  
Open Item Draft Response  
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**Rev A**

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Approved By: Steve Yang

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### Revision History

Date	Revision	Author	Changes
1/21/2020	A0	Jordan Mott	Initial Draft
1/22/2020	A1	Jordan Mott	Post 1/22 meeting comments
2/6/2020	A	Jordan Mott	Release

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# 1 SCOPE

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## 2 CLARIFICATION FOR HFC-FPGA FCPU/X

### 2.1 APPLICATION PROCESSING FLOW

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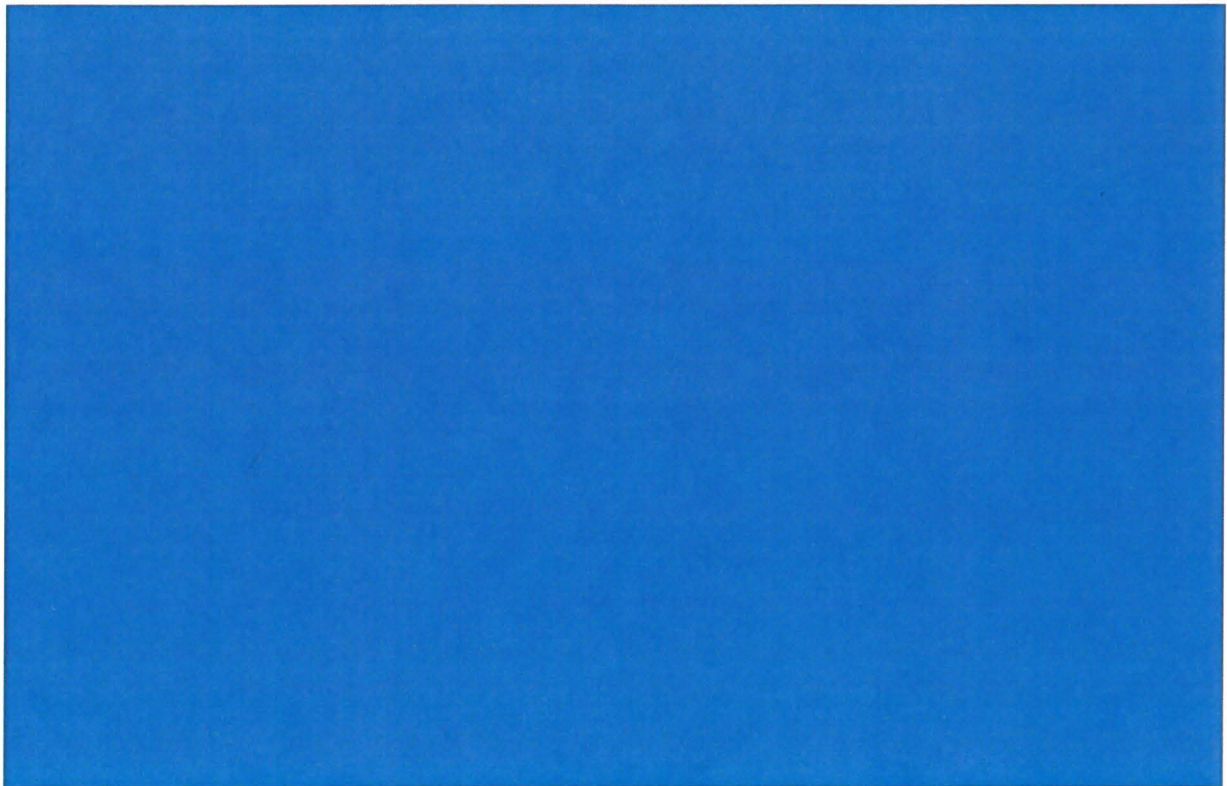
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*Figure 1 Application Processing Flow Using OneStep*

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*Figure 2 Platform and Application Digital Logic Interfaces*

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2.1.1 Clarification for PROGRAMMING

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2.1.2 CLARIFICATION FOR SYSTEM COMMUNICATION CONFIGURATION

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*Figure 3 HFC FPGA Node Station ID Configuration*

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2.2 HFC-FPGA FCPUX CONTROLLER BOOTUP (D-20, D-22, D-64)

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*Figure 4 FCPUX System Boot Block Diagram*

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*Figure 5 HFC FPGA Controller Startup to Normal Operation*

2.3 CONTROL FPGA NORMAL OPERATION (D-22, D-14)

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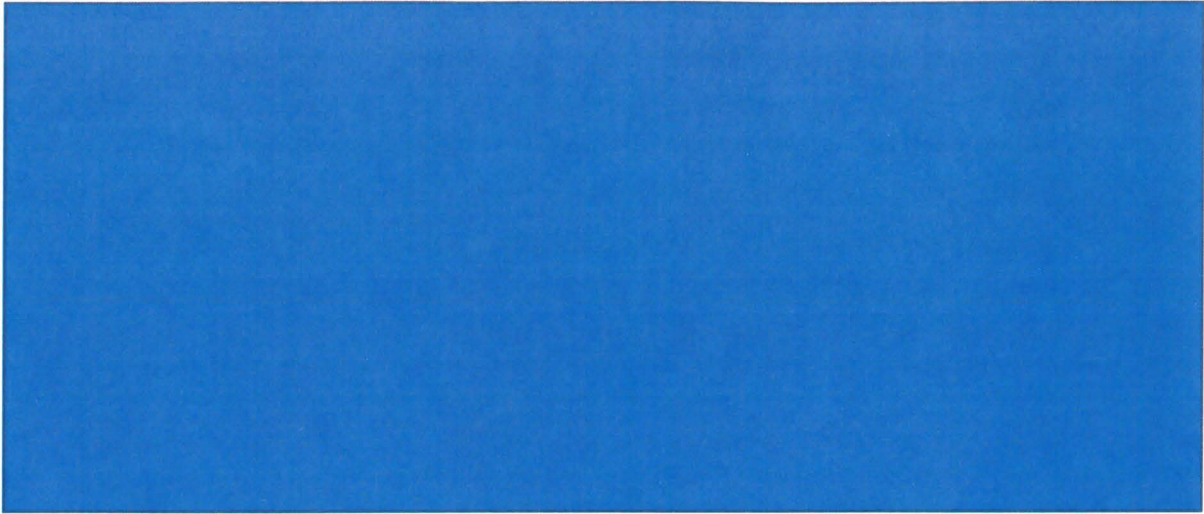
2.3.1 TOKEN ENGINE PROCESS CYCLE (D-22, D-44, D-64)

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*Figure 6 FCPUX Token Engine Process Enable Sequence*

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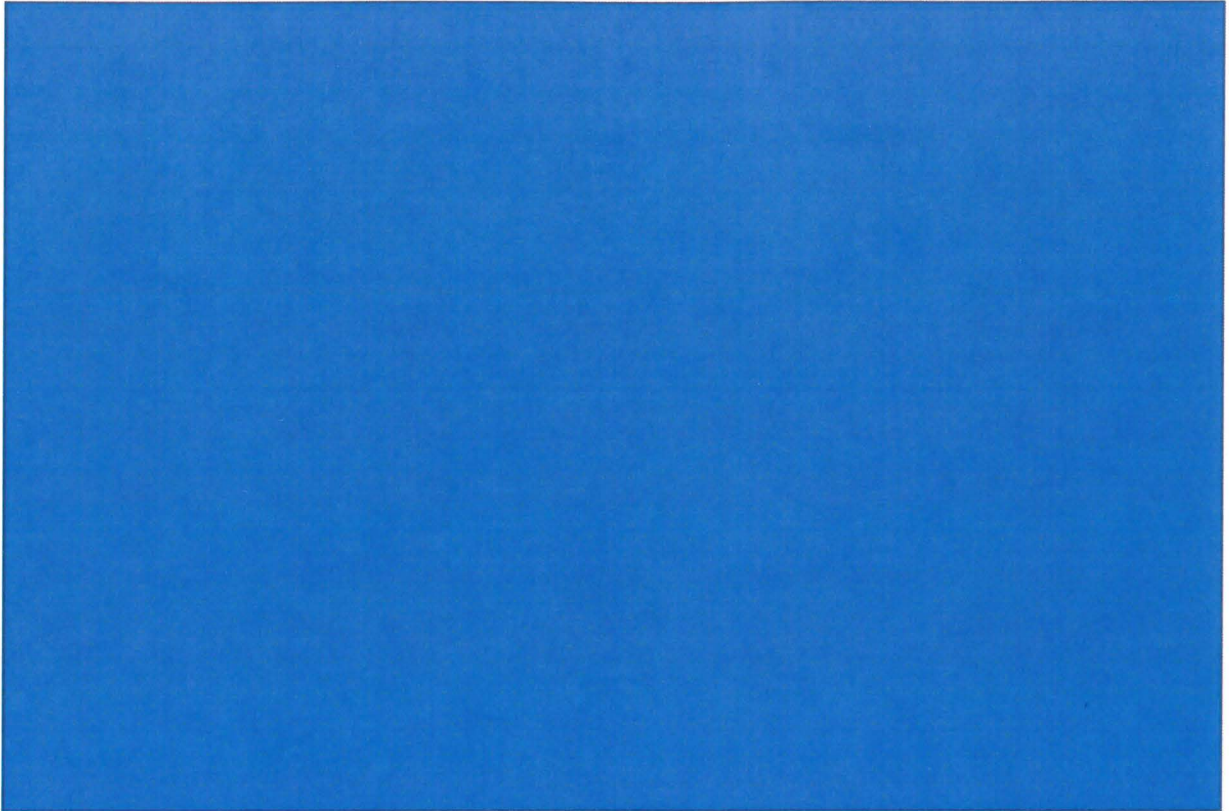
*Figure 7 HFC FPGA Normal Operation Process Dataflow*

2.3.2 F-LINK DESIGN CLARIFICATION (D-22, D-64)  
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2.3.2.1 F-LINK DATA FLOW – (D-15)  
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2.3.2.2 F-LINK MFM CONTROL  
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*Figure 8 F-LINK MFM Control Flow Diagram*



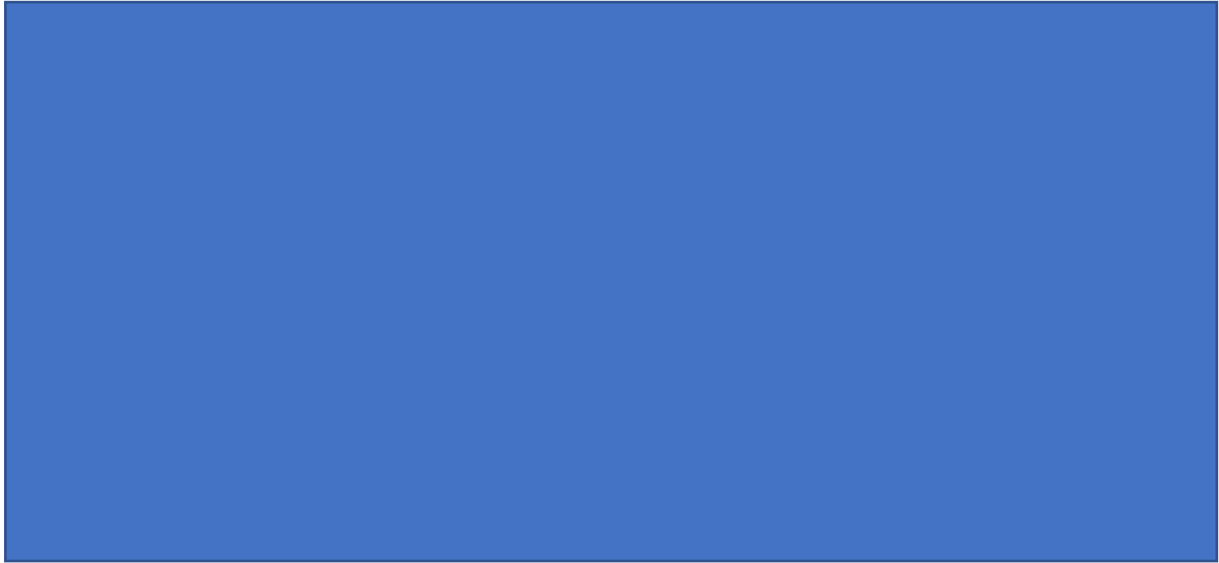
*Figure 9 F-LINK DATA FLOW DETAIL BLOCK DIAGRAM*

2.3.3 G-LINK (D-16, D-38, D-45)

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*Figure 10 G-Link Data Flow Block Diagram*

2.3.4 APPLICATION PROCESSING DESIGN CLARIFICATION (D-40)

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*Figure 11 Application Processing Data Flow Block Diagram*

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2.3.4.1      *Application Defined Data movement (D-38, D-72)*

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2.3.4.2 CQ4 Algorithm Verification

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*Figure 12 CQ4 Block Test Block Diagram*

2.3.4.3      *Application Defined Timer Processing*

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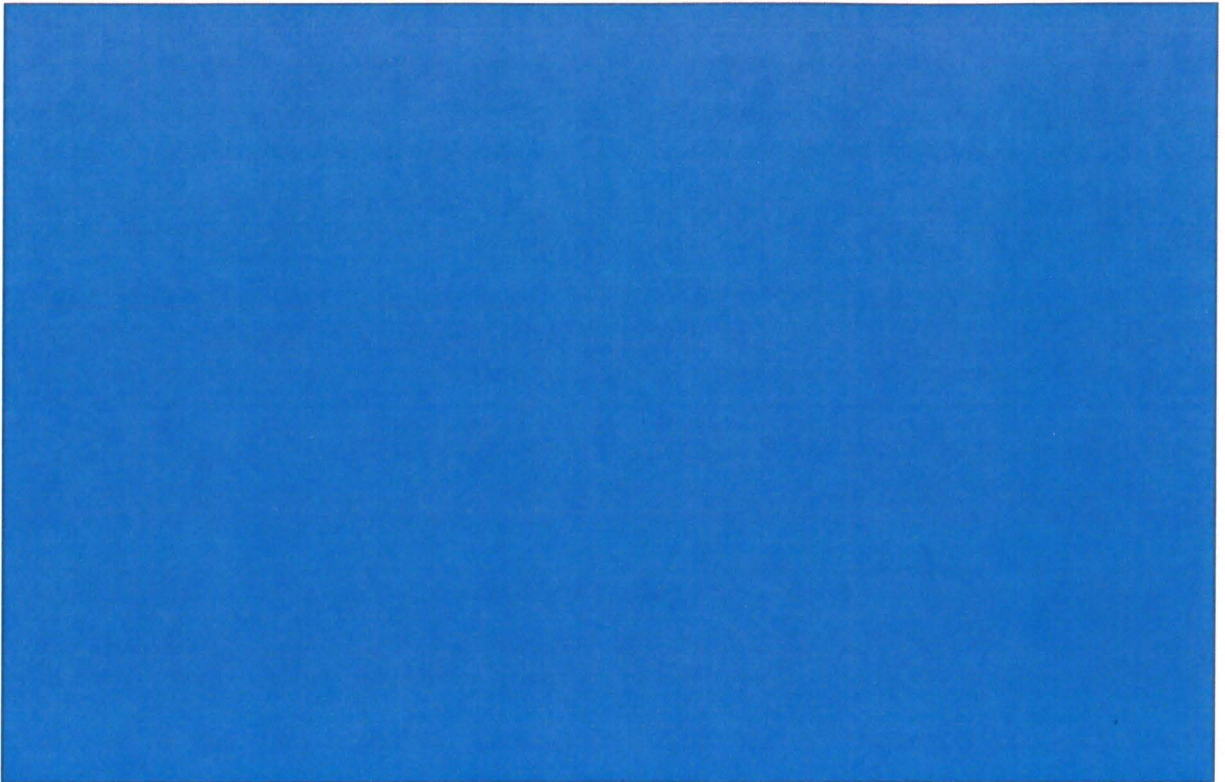
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2.3.4.4      *Application Defined Digital Logic Processing (D-18, D-19)*

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*Figure 13 Application Digital Logic Input and Output*

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2.3.4.5      Quality Data (D-18)

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2.3.5 REDUNDANCY INTERFACE – RIF (D-17)

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*Figure 14 RIF Data Flow Block Diagram*

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2.3.6 CONTROL/DIAGNOSTIC FPGA CLOCK DOMAINS (D-41)

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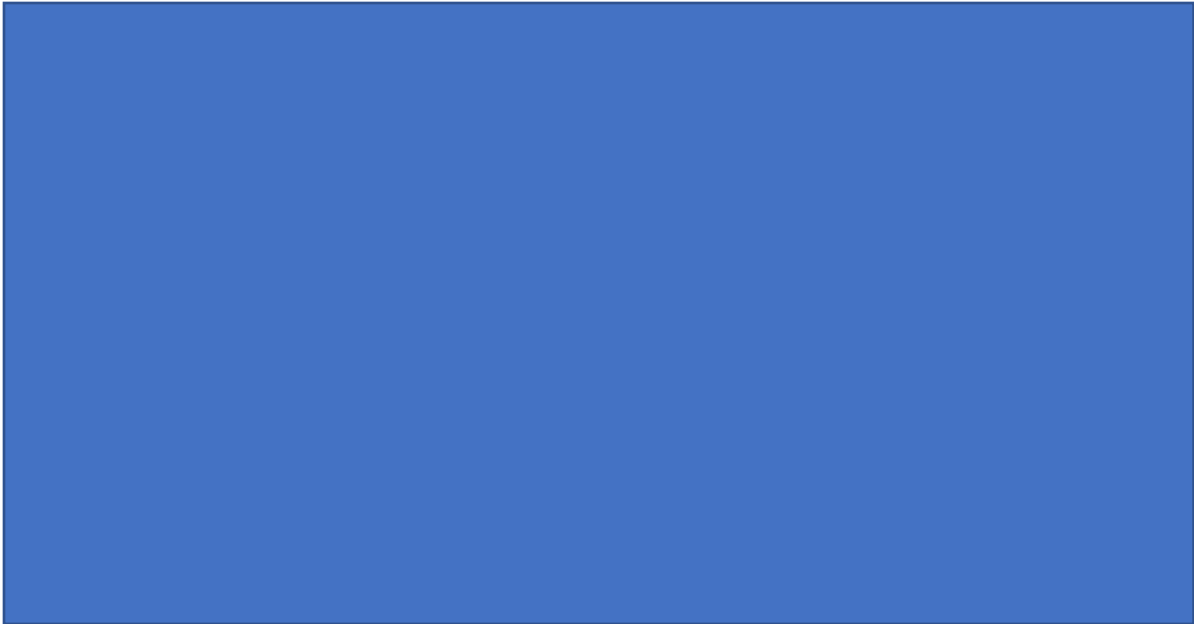


Figure 15 Control/Diagnostic FPGA Clock Domain Block Diagram

2.4 DIAGNOSTIC FPGA NORMAL OPERATION (D-48)

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*Figure 16 Control/Diagnostic Functional Role Block Diagram*

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### 3 HFC-FPGA WATCHDOG MECHANISMS

#### 3.1 WATCHDOG NORMAL OPERATION (D-20)

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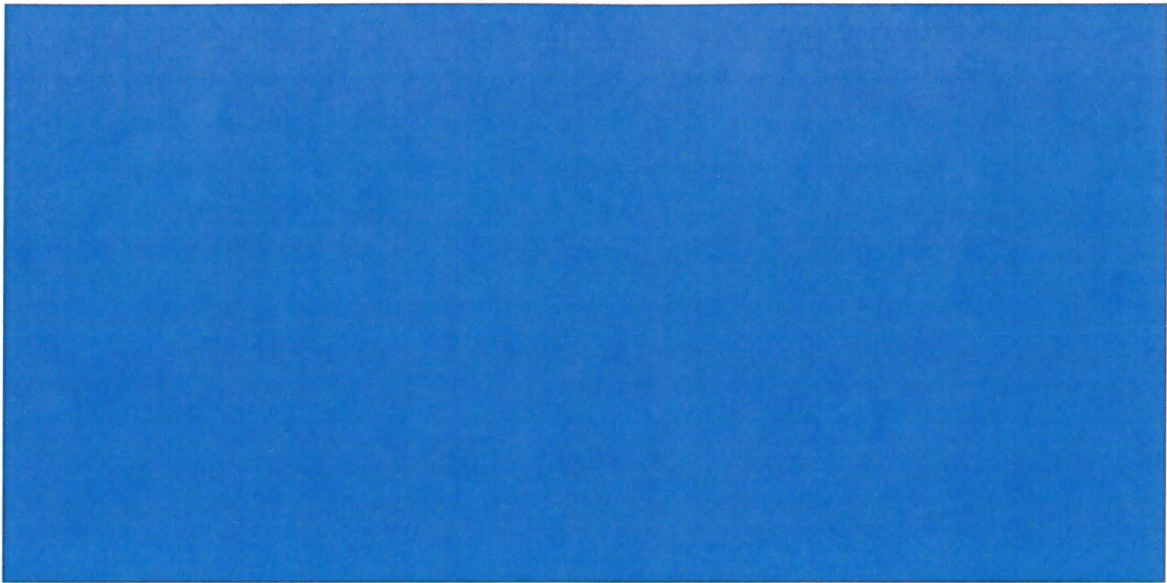
*Figure 17 FPGA Module Watchdog Block Diagram*

#### 3.1.1 DIAGNOSTIC FPGA EXTERNAL RESET WATCHDOG (D-9, D-11)

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*Figure 18 External Watchdog Circuit*

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3.1.2 DIAGNOSTIC HEARTBEAT SEQUENCE (D-7, D-12, D-49-52)

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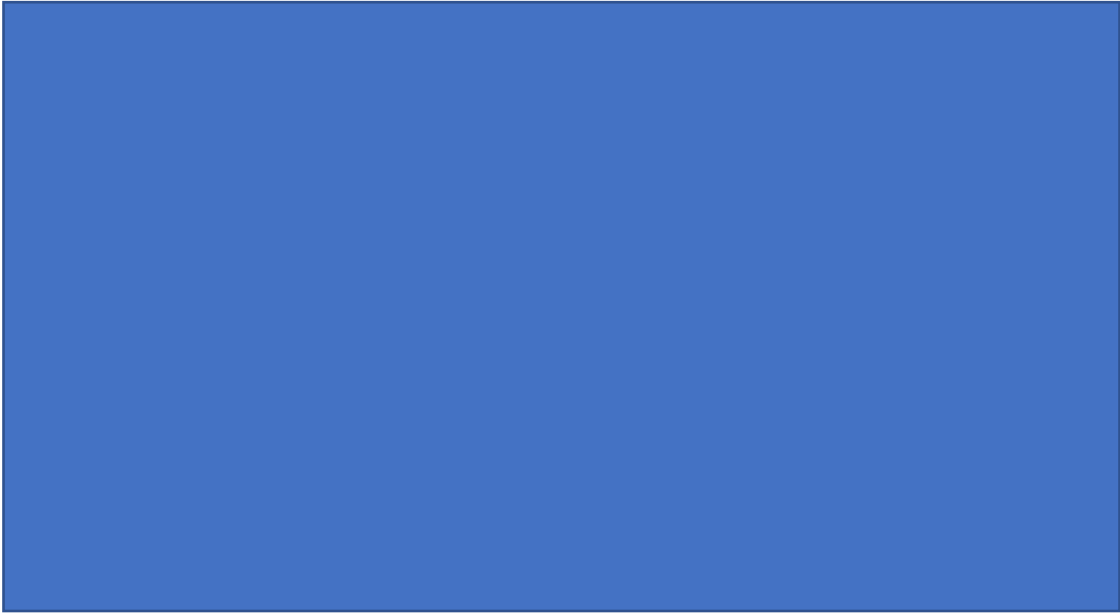
*Figure 19 Sequence Number Diagnostic Flow*

3.1.3 APPLICATION PROCESSING WATCHDOG (D-8, D-10, D-13)

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*Figure 20 Application Watchdog Flow Chart*

#### 3.1.4 WATCHDOG ELEMENT OPERATION TIMING DEPENDANCE (D-6)

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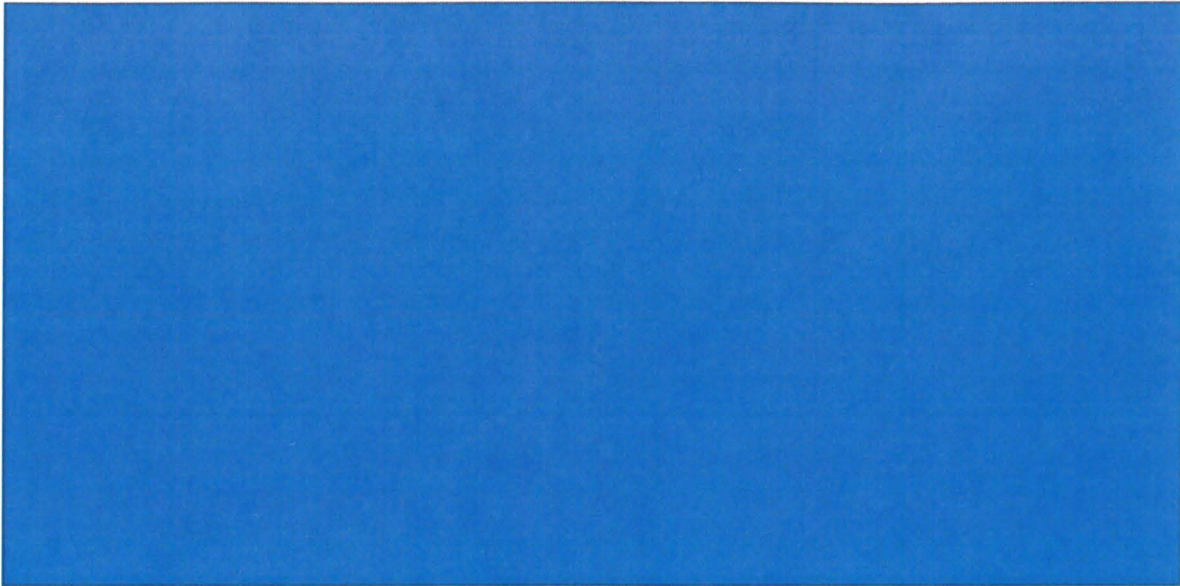
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#### 4 HFC-FPGA G-LINK GATEWAY (D-38-39, D-46, D-59, D68-72)

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*Figure 21 Interface between FPGA and CPU of HFC-FPC08 G-Link Gateway*

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#### 4.1 PROCESSOR AND FPGA NORMAL OPERATION

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##### 4.1.1 G-LINK DOWNLOAD DATA TRANSFER

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#### 4.1.2 G-LINK DATA TRANSFER – UPLOAD

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*Figure 22 G-Link Control Block Diagram*

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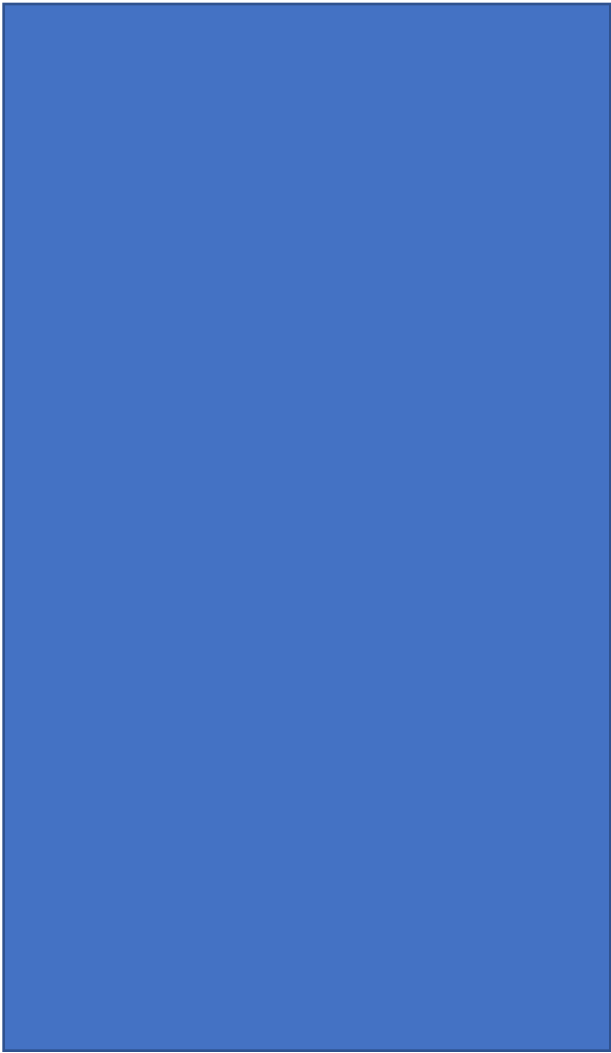


Figure 23 G-Link Control State Flow

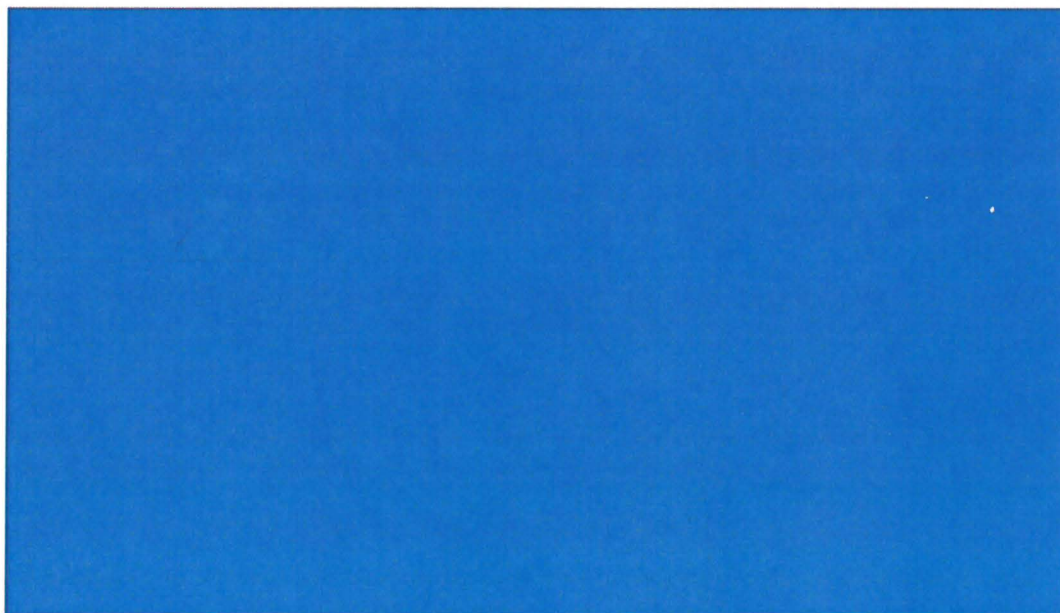
4.1.3 G-LINK DOWNLOAD DATA TYPES (D-74)

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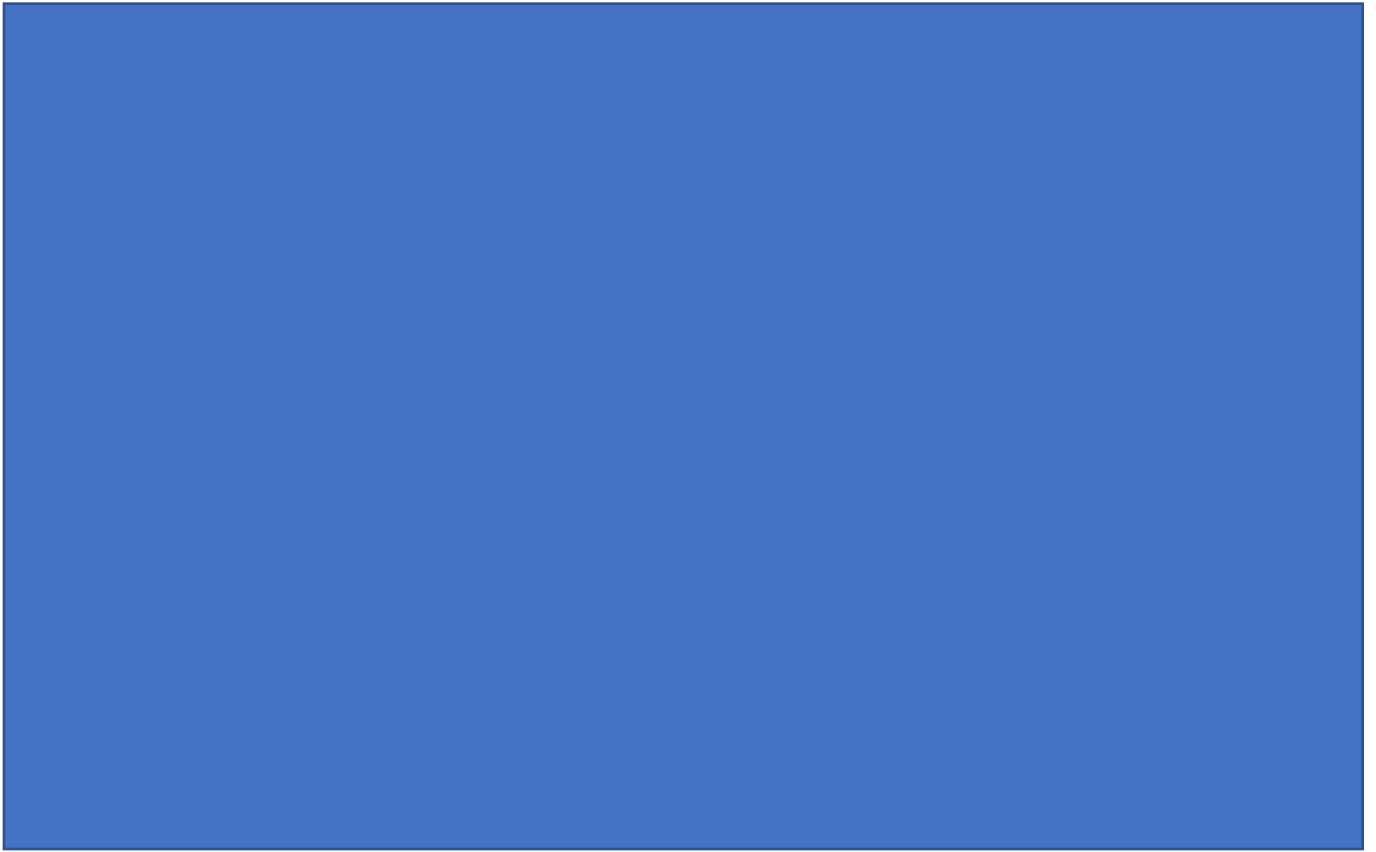
## ANALOG INPUT CALIBRATION (D-73)



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*Figure 24 Analog Input Calibration Circuit Block Diagram*

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*Figure 25 Analog Input Correction Algorithm*

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## 6 HFC-FPGA DEVICE FABRIC RESOURCE USAGE (D-60)

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*Table 1 List of Configurable Hard-core Blocks Used by HFC-FPGA Platform*



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## 7                   DIAGNOSTIC SUMMARY

(D-6, D-10, D-20, D-27, D-47, D-49, D-50, D-62, D-63, D-51)

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8 Appendix  
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*Table 2 Cross Reference Table*

