PALO VERDE NUCLEAR GENERATING STATION

UNIT 1

CEN-219(V)-NP

REVISION 00

CPC/CEAC SYSTEM
PHASE II SOFTWARE VERIFICATION
TEST REPORT

JANUARY, 1983

Combustion Engineering, Inc.

Nuclear Power Systems

Power Systems Group

Windsor, Connecticut

LEGAL NOTICE

THIS REPORT WAS PREPARED AS AN ACCOUNT OF WORK SPONSORED BY COMBUSTION ENGINEERING, INC. NEITHER COMBUSTION ENGINEERING NOR ANY PERSON ACTING ON ITS BEHALF:

A. MAKES ANY WARRANTY OR REPRESENTATION, EXPRESS OR IMPLIED INCLUDING THE WARRANTIES OF FITNESS FOR A PARTICULAR PURPOSE OR MERCHANTABILITY, WITH RESPECT TO THE ACCURACY, COMPLETENESS, OR USEFULNESS OF THE INFORMATION CONTAINED IN THIS REPORT, OR THAT THE USE OF ANY INFORMATION, APPARATUS, METHOD, OR PROCESS DISCLOSED IN THIS REPORT MAY NOT INFRINGE PRIVATELY OWNED RIGHTS; OR

B. ASSUMES ANY LIABILITIES WITH RESPECT TO THE USE OF, OR FOR DAMAGES RESULTING FROM THE USE OF, ANY INFORMATION, APPARATUS, METHOD OR PROCESS DISCLOSED IN THIS REPORT.

ABSTRACT

Phase II Testing is performed on the CPC/CEAC System to (1) verify that the CPC and CEAC software modifications have been properly integrated with the CPC and CEAC software and system hardware and (2) provide confirmation that the static and dynamic operation of the integrated system as modified is consistent with that predicted by design analyses.

This report presents the Phase II test results for the Arizona Nuclear Power Project, PVNGS-1 Plant CPC/CEAC Rev. 00, software.

The Phase II software verification tests have been performed as required in Reference 1. In all cases, the test results fell within the acceptance criteria or the results were analyzed to identify the reason for the discrepancy. Those open items discussed in Sections 3.4 and 4.3 will be resolved before the Software Package is transmitted to the Arizona Nuclear Power Project, and a supplement will be submitted to this Phase II Test Report.

TABLE OF CONTENTS

1.0 INTRODUCTION

The verification of software modifications of the CPC/CEAC System consists of several steps which address two major areas of the modification process:

(1) Specification of software modifications
(2) Implementation of software modifications

The specification of software modifications is documented in the CPC and CEAC Functional Design Description and the Data Base Document and is verified by design analyses contained in recorded calculations. The implementation of software modifications is documented in Software Design Specifications and assembly listings. The verification process for the modified software implementation includes Phase I and Phase II software verification tests.

The requirements of the Phase II software verification testing are based on the fact that the Phase I testing has been previously performed. Successful completion of Phase I testing verifies the correct implementation of the modified software. Phase II testing completes the software modification process by verifying that the integrated CPC System responds as expected.

This document contains the test results and conclusions for the Phase II software verification test.

1.1 Objectives

The primary objective of Phase II testing is to verify that the CPC and CEAC software modifications have been properly integrated with the CPC and CEAC software and system hardware. In addition Phase II testing provides confirmation that the static and dynamic operation of the integrated system as modified is consistent with that predicted by design analyses. These objectives are achieved

by comparing the response of the integrated system to the response predicted by the CPC/CEAC FORTRAN simulation code. This comparison is performed for a selected range of simulated static and dynamic input conditions.

1.2 Description of Phase II Testing

Phase II testing consists of the following tests:

(1) Input Sweep Test,
(2) Dynamic Software Verification Test, and
(3) Live Input Single Parameter Test.

These tests are performed on a single channel CPC/CEAC System with integrated software that has undergone successful Phase I testing.

1.3 Applicability

This report applies to the Phase II testing performed on the Arizona Nuclear Power Project, PVNGS-1 CPC/CEAC system software. The software revisions documented in this report are designated as Revision Number 00 to the PVNGS-1 CPC/CEAC system software.

2.0 CPC/CEAC INPUT SWEEP TESTS

The Input Sweep Test is a real time exercise of the CEAC and CPC application software and executive software with steady-state CPC and CEAC input values read from a storage device. This test has the following objectives:

(1) To determine the processing uncertainties that are inherent in the CPC and CEAC designs.

(2) To verify the ability of the CPC and CEAC algorithms used in the system hardware to initialize to a steady state after an auto-restart for each of a large number of input combinations within the CPC/CEAC operating space, and

(3) To complement Phase I module testing by identifying any abnormalities in the CPC and CEAC algorithms used in the system hardware which were not previously uncovered.

2.1 CPC Input Sweep Test Case Selection

[ ]test cases, each involving different combinations of process inputs and addressable constants, were used for CPC design qualification testing of the Revision 00 software.

2.1.1 CPC Processor Uncertainty Results

For each test case, differences in the results of the FORTRAN simulation code and CPC system were calculated. A statistical analysis of these differences produced the processing uncertainties.

The DNBR statistics did not include those cases for which the DNBR as calculated on either system was at the limits[ ]. This is because a difference of zero (or close to zero) would be computed and would incorrectly weight the distribution of differences. A total of [ ]cases remained after these cases were eliminated. The LPD statistics did not include those cases for which the LPD as calculated on either system was equal to or greater than the upper limit of [ ]core average kw/ft (=[ ] kw/ft). A total of [ ]cases remained after these cases were eliminated.

Although[ ]cases were not included in the computation of DNBR and LPD statistics, respectively, they were still included as Input Sweep test cases for the purpose of identifying potential software errors.

The processor uncertainties for DNBR and LPD are defined as the one-sided tolerance limits which encompass 95% of the distribution of DNBR and LPD differences for all test cases with a 95% confidence level. The processor uncertainties determined from Input Sweep for DNBR and LPD respectively are[ ] DNBR units, and[ ]core average kw/ft. However, since the distribution of differences is so restrictive the maximum error may be used (that is, the limits which encompass 100% of the difference). This is more conservative and yet still results in small processor uncertainties. Thus defined, the processor uncertainties for Revision 00 on DNBR and LPD are [ ]DNBR units and [ ] core average kw/ft, respectively.

2.1.2 Analysis of CPC Input Sweep Test Results

The results of the test cases exceeding the 95/95 tolerance limit were analyzed for evidences of software errors.

The review results of the DNBR and LPD test cases outside the 95/95 tolerance limit will now be discussed. For DNBR there were [ ] cases below the lower tolerance limit of [ ] (DNBR units) and [ ] test cases above the upper tolerance limit of [ ] [ ] (DNBR units). For these [ ] test cases the difference between the single channel and the CPC Fortran is within the accuracy of the two systems.

These differences do not show a significant commonality since the differences are absolute (not relative) and it should be expected that the largest differences should occur at high DNBR's. It is therefore concluded that no errors are indicated in the CPC Single Channel DNBR program.

For LPD the cases examined were: [ ] cases with differences below the lower 95/95 tolerance limit of [ ] (% of core average kw/ft), [ ] cases with differences greater than the upper tolerance limit of [ ].

The largest percent error among the [ ] cases was [ ]. The common input to these test cases was found in other test cases with less maximum difference and less percent error. Examination of the inputs to all [ ] LPD cases outside the tolerance limits showed that the inputs covered a wide spectrum. No common area was found. It is therefore concluded that there is no indication from the Input Sweep test results of software errors in the Single Channel calculation of LPD.

2.2 CEAC Input Sweep Test Case Selection

[ ]test cases, each involving different combinations of CEAC process inputs were used for CEAC design qualification testing of the Revision 00 software. These test cases covered all CEAC operating space.

2.2.1 CEAC Processor Uncertainty Results

For each test case, differences between the CEAC FORTRAN simulation code and CEAC single channel system results were calculated. The processor uncertainties for DNBR and LPD are defined as the one-sided tolerance limits which encompass 95% of the distribution of DNBR and LPD penalty factor differences for all test cases with a 95% confidence level.

The processor uncertainties for the DNBR and the LPD penalty factor differences are [ ]respectively.

2.2.2 Analysis of CEAC Input Sweep Test Results

The results were reviewed for representativeness and for any evidence of computational differences between the CPC FORTRAN simulation and the Single Channel Facility (SCF). The test data produced penalty factors which swept the respective DNBR and LPD penalty factor ranges with emphasis on the midrange values. The differences between the penalty factors from the SCF and the FORTRAN simulation were within a range which is justified by the differences in word length. Therefore, it was concluded that the results of the [ ] test cases did not indicate the existence of software errors.

3.0 DYNAMIC SOFTWARE VERIFICATION TEST

The Dynamic Software Verification Test (DSVT) is a real time exercise of the CPC application software and executive software with transient CPC input values read from a storage device. This test has two objectives:

(1) To verify that the dynamic response of the integrated CPC software is consistent with that predicted by design analyses, and

(2) To supplement design documentation quality assurance, Phase I module tests, and Input Sweep Tests in assuring correct implementation of software modifications.

Further information concerning DSVT may be found in Reference 1.

3.1 DSVT Case Selection

Test cases for DSVT are selected to exercise dynamic portions of the CPC software with emphasis on those portions of the software that have been modified.

DSVT requires that, as a minimum, cases [ ] be selected for testing (Reference 1). These cases are from the Phase II test series (identified in Reference 1) and consist of a

[ ]

All of the DSVT test cases were executed using the CPC/CEAC FORTRAN

simulation code and the single channel facility with the Rev. 00 CPC software. Because PVNGS-1 has one fewer regulating CEA banks than previous CPC-protected plants, only[ ]of the usual[ ] subcases needed to be executed in the shutdown sequence represented by case[ ]. Subcase[ ]was retained in a dummy format to preserve a test case numbering sequence which was consistent with previous tests. In addition, cases[ ], each consisting of[ ]subcases were executed to test the CPC/CEAC response to reactor power cutback.

3.2 Generation of DSVT Acceptance Criteria

Acceptance criteria for DSVT are defined (in Reference 1) as the trip times and initial values of DNBR and LPD for each test case. These trip times and initial values are generated using the certified CPC/CEAC FORTRAN simulation code. Processing uncertainties obtained during Input Sweep testing are factored into the acceptance criteria for initial values of DNBR and LPD where necessary. Trip times are affected by program execution lengths as well as by the Input Sweep uncertainties. The minimum, average, and maximum execution lengths (in milliseconds) calculated for the Revision 00 software are listed below.

CPC Application Program Execution Lengths

Program	Minimum (msec)	Average (msec)	Maximum (msec)
FLOW	[		]
UPDATE			
POWER			
STATIC			

Each DSVT case was initially executed once with nominal program execution lengths and data base values of trip setpoints using the CPC/CEAC FORTRAN simulation code. Following execution

of the same cases using the single channel facility, cases which did not yield trip times equivalent to those calculated by the CPC FORTRAN code were re-analyzed.

Each of these DSVT cases were re-executed once with the minimum execution lengths and most conservative DNBR and LPD trip setpoints and once with the maximum execution lengths and least conservative DNBR and LPD trip setpoints. This process produced a bandwidth of trip times for each test case which contained the effects of processing uncertainties and variations in application program execution lengths.

The software DSVT program also includes a[ ]millisecond interrupt cycle in order to check for DNBR and LPD trip signals. This results in a[ ]millisecond interval limit on trip time resolution which is factored into the acceptance criteria. The following tables contain the final DSVT acceptance criteria for initial values and trip times for DNBR and LPD.

Acceptance Criteria for

DNBR and LPD Initial Values (DNBR Units and kw/ft., respectively)

Test Case	DNBR (Min.)	DNBR (Max.)	LPD (Min.)	LPD (Max.)
[				]

Acceptance Criteria for

DNBR and LPD Initial Values (DNBR Units and kw/ft., respectively)

(Cont.)

Test Case	DNBR (Min.)	DNBR (Max.)	LPD (Min.)	LPD (Max.)
[				]

Acceptance Criteria for

DNBR and LPD Trip Times (seconds)

Test Case	DNBR Trip (Min.)	DNBR Trip (Max.)	LPD Trip (Min.)	LPD Trip (Max.)
[redacted]				

Acceptance Criteria for

DNBR and LPD Trip Times (seconds)

Test Case	DNBR Trip (Min.)	DNBR Trip (Max.)	LPD Trip (Min.)	LPD Trip (Max.)
[				]

DSVT TEST RESULTS

Test Case	Initial DNBR (DNBR Units)	Initial LPD (kw/ft.)	DNBR Trip (sec.)	LPD Trip (sec.)
[				]

DSVT TEST RESULTS

Test Case	Initial DNBR (DNBR Units)	Initial LPD (kw/ft.)	DNBR Trip (sec.)	LPD Trip (sec.)
[				]

3.4 Analysis of DSVT Results

For all test cases, the initial values of DNBR and LPD were within those defined by the CPC/CEAC FORTRAN simulation code generated band widths which include the processing uncertainties obtained from the CPC Input Sweep Test.

Test cases [ ] are cases with the plant initially in a trip condition. In the CPC FORTRAN simulation code, one program execution cycle is needed to generate a trip output. This implies an acceptance criterion of [ ] sec. for minimum and maximum time-to-trip, while the actual trip times for the CPC single channel were [ ] sec. These FORTRAN cases were examined to verify that a trip condition existed at time [ ] justifying the indicated acceptance criteria for time-to-trip of [ ] sec. consistent with the expected CPC single channel response.

[

]

Modification of the data base requires a software change and subsequent repetition of affected portions of Phase I and II testing. The results of that testing will be issued as a supplement to this document.

4.0 LIVE INPUT SINGLE PARAMETER TEST

The Live Input Single Parameter test is a real-time exercise of the CPC/CEAC application and executive software, with transient CPC/CEAC input values generated from an external source and read through the CPC/CEAC input hardware. The objectives of this test are:

(1) To verify that the dynamic response of the integrated CPC/CEAC software and hardware is consistent with that predicted by design analyses.

(2) To supplement design documentation quality assurance, Phase I module tests, Input Sweep Tests, and DSVT in assuring correct implementation of software modifications.

(3) To evaluate the integrated hardware/software system during operational modes approximating plant conditions.

4.1 LISP Test Case Selection

Reference 1 identifies the test cases to be used for LISP. These cases are the single variable dynamic transient test cases from the Phase II test series. In addition, a test case is included to test the Reactor Power Cutback (RPC) feature.

[These test cases, which are applicable to PVNGS-1, consist of a]

4.2 Generation of LISP Acceptance Criteria

The acceptance criteria for LISP are based on trip times for the dynamic test cases. For the RPC test case, there should be no trip during RPC.

These cases are simulated in the CPC FORTRAN simulation code and contain the following adjustment components.

[

]

Application program execution lengths used for LISP testing were the same as those for DSVT, with the addition of CEAC minimum and maximum execution lengths of [ ] msec, respectively.

The final acceptance criteria (generated by the CPC FORTRAN simulation code and adjusted for the above components) for LISP are contained in the following table.

Test Case	Minimum Trip Time (seconds)	Maximum Trip Time (seconds)
[		]

4.3 LISP Test Results

The [ ] dynamic transients were executed on the CPC Single Channel facility. The recorded trip times (in seconds) for each case are listed in the following table:

Run	[ ]

All recorded trip times met the final acceptance criteria for LISP. The result of test case [ ] showed that the RPC feature, as expected, caused no CPC trip when the single bank RPC was inserted.

Major aspects of the operator's module operation, particularly the Point ID verification and addressable constant range limits were tested. As part of the testing, the CPC and CEAC Point ID tables were checked to assure that the Point IDs displayed on the operator's module are the same as those listed in the Point ID tables.

There were some discrepancies in CPC Point IDs [

[redacted]. They will be resolved in the supplement to this document.

All aspects of automated reentry of Addressable Constants were tested and were determined to have been correctly implemented.

5.0 PHASE II TEST RESULTS SUMMARY

The Phase II software verification tests have been performed as required in Reference 1. In all cases, the test results fell within the acceptance criteria or the results were analyzed to identify the reason for the discrepancy. Those open items discussed in Sections 3.4 and 4.3 will be resolved before the Software Package is transmitted to the Arizona Nuclear Power Project and a supplement will be submitted to this Phase II Test Report.

6.0 REFERENCES

1. CPC Protection Algorithm Software Change Procedure CEN-39(A)-P, Revision 02, December 21, 1978.

2. Palo Verde Nuclear Generating Station Unit 1, Cycle 1 CPC/CEAC System Phase I Test Report, CEN-217(V)-P, Revision 00, January, 1983.