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Topical Report

Licensing Topical Report for Toshiba NRW-FPGA-based Instrumentation and Control System for Safety-Related Application

Part II
Design Description of the Platform with Application Guide

Approved by
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Note for Acronyms and References

All acronyms and references are listed in the separate Acronym and Reference Part, which is part of this LTR.

II-1 Introduction

This is Part II of the Licensing Topical Report (LTR) for the Toshiba Non-Rewritable Field Programmable Gate Array-based (NRW-FPGA-based) Instrumentation and Control (I&C) Systems for Safety-Related Applications. This part addresses the Design Description of the Platform and includes the Application Guide.

II-1.1 Background

Toshiba has extensive experience in supplying nuclear safety-grade Instrumentation and Control (I&C) systems in Japan. This experience ranges from supplying digital I&C systems, such as power range neutron monitors for individual plants, up to designing and manufacturing the world's first fully integrated digital CPU-based I&C systems for Advanced Boiling Water Reactors (ABWRs). These systems were first installed at Kashiwazaki-Kariwa Unit 6, and are in use at Kashiwazaki-Kariwa Unit 6 and Hamaoka Unit 5.

Following the installation of the CPU-based BWR digital system, Toshiba started development of I&C technology based on Non-Rewritable (NRW) Field Programmable Gate Arrays (FPGAs) and supplied the NRW-FPGA-based I&C products to Japanese Nuclear Power Plants under Toshiba's ISO 9001 program. NRW-FPGA-based products have been installed in 11 nuclear power plants including 254 NRW-FPGA-based units for non-safety-related systems, 91 units for safety-related process radiation monitors, and 60 units for safety-related neutron monitoring systems.

Toshiba also established a 10 CFR 50 Appendix B (Reference (a2)) Quality Assurance (QA) process to permit the use of Toshiba FPGA-based system in the US for safety-related applications in nuclear power plants. Toshiba implemented Appendix B QA processes in a phased approach as follows to ensure a smooth transition of the processes at the affected organizations.

- Original Process:
  Initial establishment of the Appendix B QA process in the system engineering organization. This process was applied to the development and the qualification of the Power Range Monitor (PRM) for a Boiling Water Reactor (BWR)-5. This process is referred to as the "Original Process" in this topical report.
- Current Process:
  Toshiba improved the Original Process by extending the Appendix B QA process into the design organization and closer to the manufacturing organization where other Toshiba NRW-FPGA-based I&C products are developed. This process is referred to as the "Current

Process" in this LTR. All future work will be under this process, including modifications to equipment produced under the original process.

Toshiba has used the Original Process to develop and qualify a NRW-FPGA-based PRM for a BWR-5. Toshiba used the Current Process to develop and qualify the Oscillation Power Range Monitor (OPRM) for ABWR.

This LTR uses the term, "PRM," to mean PRM for BWR-5 and uses the term, "OPRM," to mean OPRM for ABWR.

This LTR consists of the following six parts:

Part I describes software lifecycle and development processes.

Part II provides the design descriptions for the PRM and the OPRM and includes an application guide.

Part III describes the qualification results for the PRM and the OPRM.

Part IV provides compliance tables for Toshiba processes to important Codes and Standards.

Part V provides the BWR-5 PRM V&V report.

Part VI provides the ABWR OPRM V&V report.

The Acronym and Reference Part lists all the acronyms and references used in the all Parts except Part V and VI of the LTR. Part V and Part VI have their own acronym and reference list because they are the existing V&V Reports for the PRM and the OPRM.

This is Part II of the LTR.

II-1.2 Purpose

Part II of the Toshiba LTR describes the design features and provides the Application Guide for the Toshiba NRW-FPGA-based PRM and OPRM.

II-1.3 Scope

This report is submitted to the USNRC for review and approval of the Toshiba NRW-FPGA-based Safety-Related PRM and OPRM.

The NRW-FPGA-based systems have been implemented on several different plant systems, as described in Section I-1.1 in this LTR.

Part II provides the platform design description and design principles for the PRM and the OPRM. This part also provides the Toshiba Application Guide for these systems, including the adaptation of this equipment to other types of boiling water reactors, including BWR-3, BWR-4, BWR-5, and BWR-6 designs. This part includes the following information:

- Section II-1 provides introductory material including the report purpose and scope,
- Section II-2 provides descriptions of the platform and its application systems.
- Appendix II-A provides the Application Guide, which Toshiba includes as part of the topical report, for inclusion and consideration in the SER.
- Appendix II-B provides the Module Summary Descriptions (MSDs) of the modules.

II-2 FPGA System Description

II-2.1 FPGA Platform

The PRM and the OPRM are Toshiba NRW-FPGA-based Safety-Related I&C systems. This section introduces the systems in general for a better understanding of the PRM and the OPRM.

II-2.1.1 FPGAs

Figure II-2-1 below provides a graphical depiction of the text in this section.

An FPGA is a type of integrated circuit with uncommitted logic gates, which a user can program to perform specific functions. The non-rewritable FPGA used by Toshiba incorporates thousands of logic cells linked by one-time programmable connections that logically interconnect cells to implement different functional requirements. Logic cells are Register cells (R-cells) and Combinatorial cells (C-cells) in the FPGA Toshiba uses. In addition to logic cells, other programmable elements of an FPGA are input and output (I/O) blocks, which serve as the interface between internal signal lines and the chip's external pins, and interconnects, which route I/O signals to appropriate destinations. The FPGA chosen by Toshiba can only implement digital logic.

In this section and the following sections, Toshiba describes how the FPGAs are used and configured to build the NRW-FPGA-based Safety-Related I&C Systems. Where appropriate, the PRM system for a BWR-5 is used as an example.

The NRW-FPGA Safety-Related I&C Systems are based on pure logic implementations of the algorithms. Toshiba does not include a microprocessor emulator or traditional software. There is no operating system. The software issues associated with multi-tasking, interrupts, serial execution, semaphores, and other software issues are eliminated. Toshiba builds custom design logic, created solely from function blocks Toshiba developed under the Toshiba software program, to implement these systems.

Figure II-2-1 illustrates the architecture of the PRM. The PRM system consists of the Local Power Range Monitor (LPRM), Local Power Range Monitor / Average Power Range Monitor (LPRM/APRM), and FLOW units. Each unit contains a defined set of modules. Figure II-2-1 includes an example of the LPRM module, which illustrates how a module contains electronics and one or more FPGAs that implement logic cells. The FPGA logic is comprised of combinations and connections of software elements called Functional Elements (FEs). Discrete

logic cells are captured in FEs, as shown at the bottom of Figure II-2-1. The Oscillation Power Range Monitor (OPRM) architecture is similar to the NRW-FPGA-based PRM architecture described above.

The module supplier, a division internal to Toshiba, has designed, verified, registered, and placed under configuration management the standard, reusable FEs under their ISO 9001 QA program. The FEs are treated as Commercial-off-the-Shelf (COTS) software, registered in the FE library, and controlled by the module supplier. Nuclear Instrumentation and Control Systems Department (NICSD) evaluates the FEs for use in safety systems. If design changes are required to an FPGA-based safety related system, NICSD evaluates the contents of each design change under their 10 CFR 50 Appendix B QA Program to determine whether new FEs are necessary. If new FE development is necessary, NICSD instructs the module supplier to develop new FEs, which NICSD evaluates for suitability. The evaluation processes for the FEs under the NICSD CGD process is described in Section I-2.2.2.1 of this LTR.

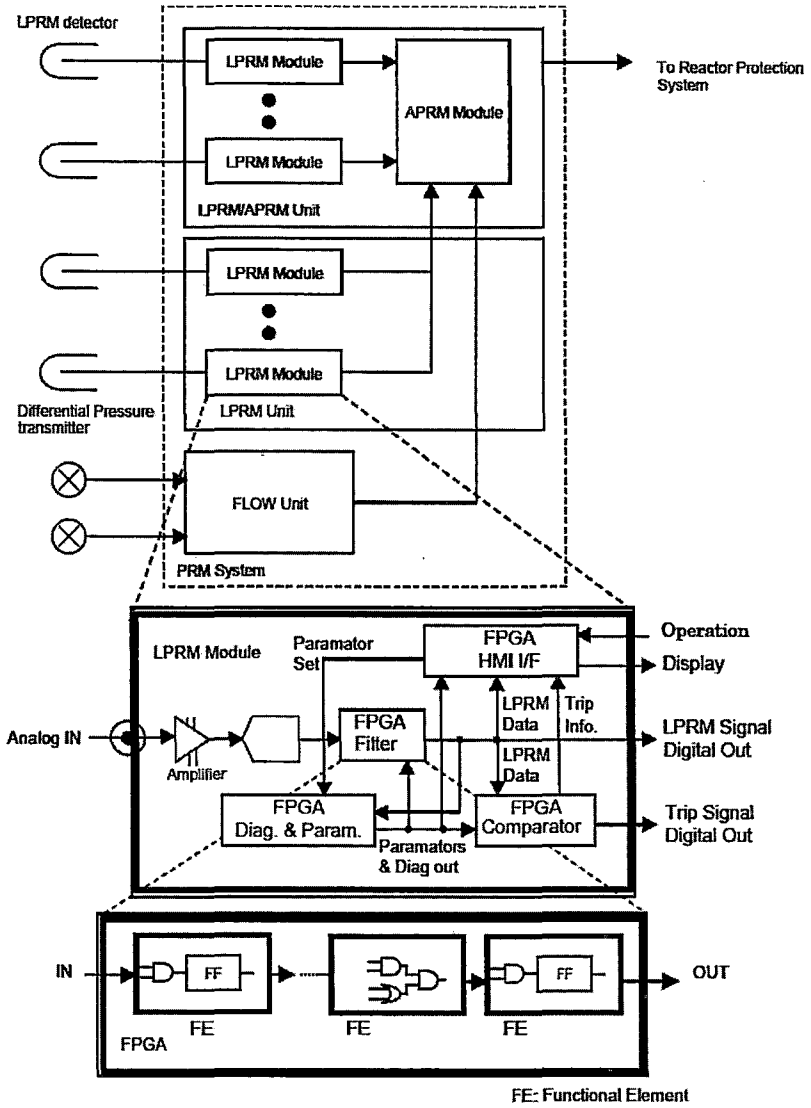


Figure II-2-1 Architecture of PRM System

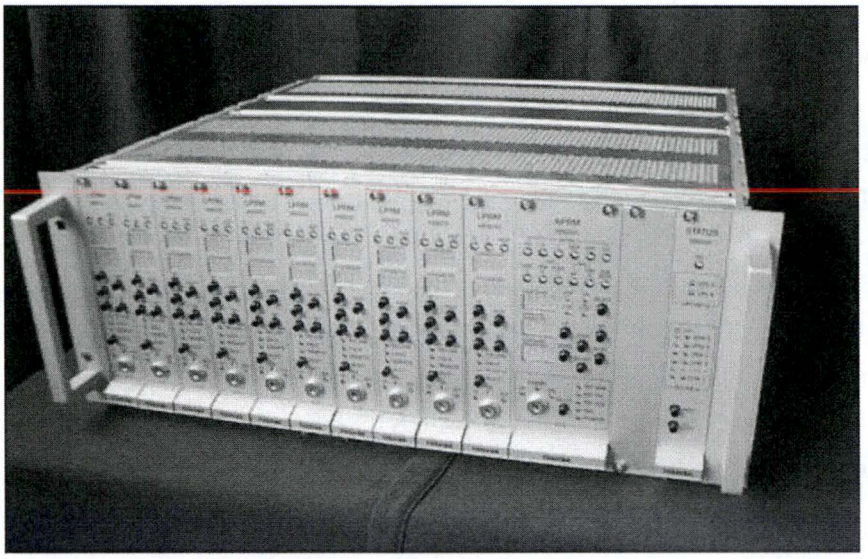
II-2.1.2 Modules

Each module consists of one or more printed circuit boards, on which the FPGAs and other circuitry are mounted, and a front panel. Some modules require two printed circuit boards, including a small printed circuit board for the Human-System Interface (HSI) on each module's front panel. The front panel provides mounting and electrical connections for the HSI. The front panel HSI provides a flat, front surface for discrete Light Emitting Diodes (LEDs) for status, numeric LEDs for values, and dedicated function pushbutton switches. The panel also provides captive screws, to ensure that the modules remain in the unit (chassis) and operable through seismic events. Analog and digital components, including the FPGA chips, are soldered to the printed circuit boards. The module configuration and module list for typical applications are described in Section II-2.2.2.4.

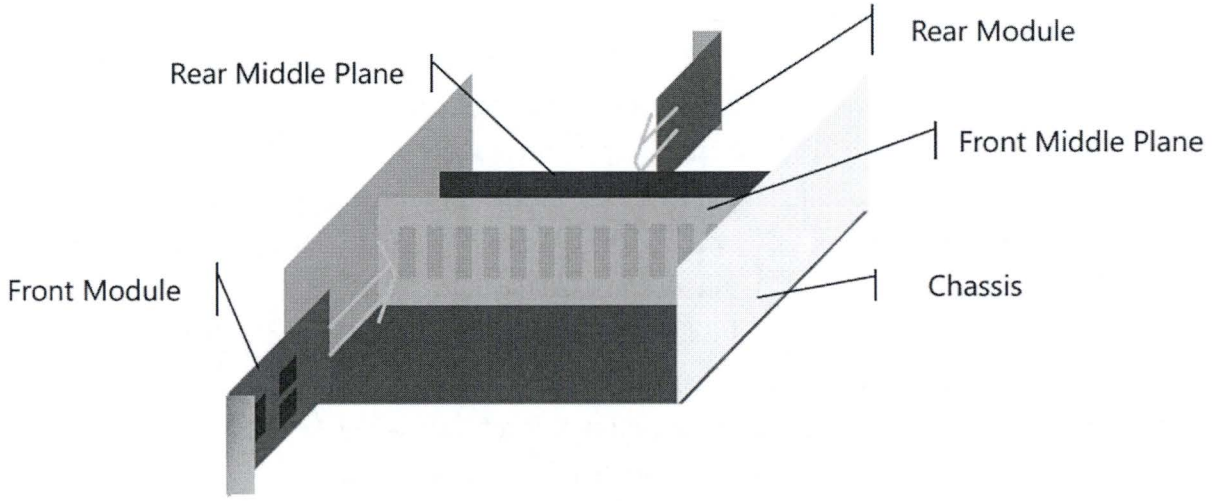
II-2.1.3 Units

Figure II-2-2 (1) below shows the LPRM/APRM unit overview and Figure II-2-2 (2) illustrates the structure of units. The unit is a chassis that has front slots and back slots to mount modules. Each unit consists of several modules. There are two vertical middle planes, a front middle plane and a rear middle plane, between the front and back slots in each unit. These middle planes are circuit boards. These circuit boards provide backplanes for the front and rear modules, with customized wiring on the middle plane circuit boards for the specific application. Modules plug into the middle planes using connectors. Once a module is plugged into the appropriate connector, it exchanges data with other modules in the unit.

The PRM and OPRM do not require forced air cooling. The PRM and OPRM are designed for natural circulation, through louvers on the top and bottom of the rear doors of the cabinets in which the system is installed. Forced cooling through fans is not required, and Toshiba did not qualify and does not plan to supply fans or other forced air cooling.



(1) LPRM/APRM Unit Overview



(2) Structure of Units

Figure II-2-2 LPRM/APRM Unit Overview and Structure of Units

II-2.1.4 Communication

II-2.1.4.1 Communication between FPGAs

Data is transferred between FPGAs over serial and parallel electrical communication links. For serial communication between FPGAs on a module, the design uses a clock, a data stream signal, and a synchronizing signal. For parallel data communication, the design uses a clocked transfer. During each data transfer, the logic sends all newly computed data and a completion signal. Failure of the completion signal to change state results in the receiving FPGA declaring the transmitting FPGA failed.

II-2.1.4.2 Communication between Modules on Middle Plane

The modules mounted in a unit communicate over copper connections printed on the two middle planes. For these data links, three-wire electrical communication links are used. In the three-wire electrical communication links, the first line conveys the data, the second line conveys the clock signal, and the third line is a load pulse that marks the end of the frame. All three lines are driven by the sender module. In the copper lines, the data are transmitted as Complementary Metal Oxide Semiconductor (CMOS) level signals on the three associated copper lines, and the data is transmitted serially.

The middle planes also provide separate three-wire electrical communication links for each analog input module (i.e., LPRM modules) and output module. For the discrete input and output (DIO) modules, the middle planes provide an individual hardwired connection for each input and output. These wires connect the module's programmable logic outputs to the appropriate DIO module input or output circuitry, and the data is transferred as parallel signals at the CMOS level. The three-wire electrical communication links and the hardwired discrete input or output wires are configured to provide the required communication links for the input and output modules in each unit.

II-2.1.4.3 Communication on Fiber Optic Communication Links between Units

Fiber optic communication links are used for communication between units.

To detect failures, the fiber optic communication link is always operating, using a clock generated on each sender module. The data link uses Manchester encoding to send zeros and ones. Each message includes parity and Cyclic Redundancy Check (CRC) in the latest versions of the TRN module and the RCV module, which make it very unlikely that any silent failure would remain

undetected by the logic.

When data needs to be transferred, a special pattern is sent to indicate the start of a data packet. A fixed length, fixed format data packet is sent after the special pattern. The receiver module must capture the message as the message is transmitted, as there is no handshaking between the modules, and thus no means to request retransmission.

The transmitting module is configured to send all required data from the unit to any external equipment. Communication to the outside world is electrically isolated using uni-directional fiber optic communication links. The fiber optic cables provide the electrical isolation. The fiber optic transmitter provides the required communication (data) isolation, making it impossible for external devices to send data back to the unit and adversely affect safety-related functions. These ports comply with the recommendations provided in IEEE Std 7-4.3.2-2003 (Reference (a30)), Annex E.

II-2.1.4.4 Communication within Divisions

This communication means the data transfer between units within the same division. All Toshiba FPGA based Safety-Related Applications apply this communication method. The communication utilizes uni-directional fiber optic communication links and communication methods described in the previous Section II-2.1.4.3 to comply with DI&C ISG-04 (Reference (a22)). The compliance table is provided in LTR Section IV-5, and communication independence is discussed in Section II-2.2.3.2.2.

II-2.1.4.5 Communication between divisions

This communication means the transfer of data between units in different divisions. This communication is not applied in the PRM or OPRM except sharing LPRM levels between divisions in the BWR-3 (see Section II-A-7.3) and the small core OPRM (see Section II-A-7.8). This communication utilizes unidirectional fiber optic communication links and communication methods described in the previous Section II-2.1.4.3 to comply with DI&C ISG-04 (Reference (a22)). The compliance table is provided in LTR Section IV-5. Communication independence is discussed in Section II-2.2.3.2.2.

II-2.1.5 FPGA Design Principles

In software development, a set of coding guidelines reduces risk and facilitates development of consistent code. For Toshiba's FPGA-based systems, the module supplier has developed a set of rules and guidance for designing logic and writing VHDL code for the FPGAs.

This section describes the general rules and considerations followed by the design engineers at Toshiba's module supplier. In addition, this section describes the measures taken by the module supplier to reduce the risk of inappropriate or incorrect system operation. This section also identifies exemptions that may be necessary in FPGA design and requirements for management approval of such exemptions.

II-2.1.5.1 General Design Rules

The following bulleted items summarize the design rules:

- Each FPGA is partitioned based on module functionality requirements and the ability to verify and validate the FPGA functionality.
- VHDL is used as the design language for FPGA logic. VHDL is defined in IEEE Std 1076-2000 (Reference (a40)).
- Each FPGA is designed for synchronous operation.
- FPGA logic is designed by combining verified Functional Elements (FEs).
- All signal paths in each Functional Element are completely tested.
- If required, the FPGA design can include input and output test pins for verification.
- The internal clear signal of the FPGA is asynchronous. The internal clear signal is used for power on reset of the FPGA. Any adverse effect from an asynchronous reset is evaluated as part of the design and any required, appropriate countermeasures are incorporated.
- Toshiba uses an antifuse FPGA architecture, which is non-volatile and non-rewriteable.
- The structure of connections of FEs in an FPGA design is retained. Toshiba allows the logic synthesis program to optimize the FEs prior to test. Once optimized and successfully tested, the FE contents are fixed and not allowed to change. Toshiba does not usually allow the logic synthesis program to optimize the connections of FEs into an FPGA. However, if the module supplier decides to use optimization, then the optimized connections will be reviewed and tested thoroughly, based on the optimized configuration.

II-2.1.5.2 Additional Design Considerations

The design engineer of the module supplier compares the cell patterns generated by the software tools against those expected based on interconnections of the FEs. Since this is important for

verification and validation efforts, the software that would optimize interconnected FEs in the FPGA logic is disabled.

The design engineers use simulation tools to verify that the FPGA logic works correctly, using test vectors written by the module supplier engineers. The functional test vectors are designed to verify the FPGA logic functions as intended. The test cases are added to ensure that all logic connections are exercised in their transitions from logic zero to logic one state, and from logic one to logic zero state. Test cases are added to the test vector, as the design engineer deems necessary. The test vectors include both the patterns to be applied and the expected state. After the source code and logic are verified, the design engineer uses the FPGA vendor's software tools to create the fusemap and embed the fusemap into an FPGA. The same test vectors are used to validate the hardware design.

(1) Testability, Feedback Loop and State Machine

If feedback is required to make the logic in an FPGA work correctly, the module supplier's design engineers route the feedback loops external to the FPGA. By so doing, the testability of the FPGA is increased, since one can now set the FPGA state with a simple sequence, rather than having to go through many test vectors to achieve a given state. The other simplifying requirement is that state machines are used only when necessary and the states are clearly defined by the signal combinations.

An example of an exception to these requirements is in the low pass filter for the Local Power Range Monitor module, where the filter requires so much feedback that there are not sufficient pins on the FPGA to support external feedback loops. Therefore, the feedback has to be performed within the FPGA. A design engineer of the module supplier functionally tests the low pass filter's operation by inputting data values into the logic and comparing the output values to the expected test vector values and verifying that they match.

(2) FPGA Resources

Microsemi (formerly Actel) states that 100% of the resources in the SX-A family FPGA can be used, including all of the input/output pins. The designer of the module supplier is still required to pay close attention to the percent utilization of various logic cells in an FPGA. The cell use and clock rates indicate an appropriately conservative design philosophy. Conservatively, Toshiba does not intend to make use of every cell in the FPGA, but leaves cells for future expansion and for correcting any design errors found during review and test.

(3) Word Size

The Toshiba FPGA design has no fixed requirements for word size. Rather, design engineers of the module supplier evaluate the mathematical functions required, and determine the appropriate number of bits required to maintain the specified device accuracy. Thus, the low pass filter on the LPRM module stores twelve-bit quantities, since that is the resolution produced by the analog-to-digital converter. When the Finite Impulse Response (FIR) filter operates, it produces mathematical results in scaled, fixed point integer arithmetic, with as many digits provided as are needed for accuracy. All FPGA logic works in fixed-point integer mode. Fractional bits are included and removed in the design as necessary to maintain the required mathematical accuracy.

(4) FPGA Interface Design

The design engineers of the module supplier design the FPGAs on a given module based on defined time constraints for the module and between FPGAs specified in a Module Design Specification. No matter how many FPGAs operate in series, the FPGA interface design must ensure that the module provides data to the next module as specified in the Module Design Specification.

If the input to the FPGA is provided over a communication link from another FPGA-based module, the FPGA can start processing without the data, but it will detect that data is not available and generate a fail signal. When an FPGA is intended to receive data from another FPGA on the module, engineers of the module supplier will design the FPGA so that the FPGA starts processing only when data is available.

II-2.1.5.3 Timing

Clocked synchronous design is used to avoid timing errors due to glitches (as described later in Section II-2.1.5.4), or other timing issues. The mechanisms that create timing errors and reasons why Toshiba's rules eliminate timing errors are explained below. Engineers of the module supplier evaluate all FE and FPGA timing by design or simulation using FPGA simulation tool.

In logic design, sequential logic can be either asynchronous or synchronous. The asynchronous class describes circuits in which the application of an input control signal propagates through the logic immediately, with no clock synchronization, and with the possibility of responding incorrectly to transient signals. In the synchronous class, changes of state occur only at selected times, controlled by a clock signal. In the logic design of FPGAs, designers may generally use two types of FEs: synchronous logic with flip-flops (FFs) and pure asynchronous logic with

combinatorial gates and no memory (no FFs).

Synchronous logic design is less sensitive to certain hazard conditions, whereas asynchronous circuits are more likely to have issues related to timing and metastability. In addition, when asynchronous data is synchronized by a clocked flip-flop, there is a probability of setup or hold time violation on the inputs to the flip-flops.

These issues originate in the propagation delays in asynchronous logic. These delays are usually very small and are responsible for introducing differential delays between signals that must travel through different numbers of logic layers and different length signal paths. Unwanted signal combinations may appear for short periods, and the logic reading those signals may interpret the short unwanted signals erroneously (refer to the discussion of glitches, provided in Section II-2.1.5.4). Well-designed synchronous circuits do not suffer from this limitation, because they conform to the control signals only when the clock pulse is present, usually after the transient spurious combinations are over.

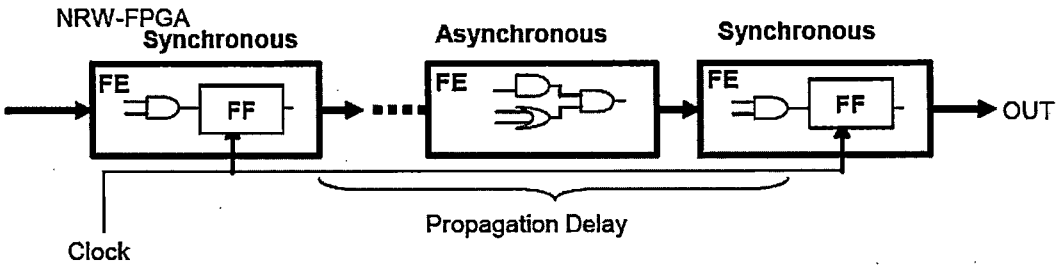


Figure II-2-3 Timing Delay

Minimizing delay is achieved by designing synchronous instead of asynchronous logic. In synchronous logic, all state changes occur on the same rising edge of the clock signal. The only remaining requirement is to allow enough time between clock pulses for signal propagation through the circuit between synchronizing registers, formed of flip-flops.

Toshiba avoids this type of timing problem discussed above through control of signal propagation delays, and using carefully designed combinations of synchronous and asynchronous functional elements within the FPGA logic. To avoid timing errors, the module supplier established FPGA design rules. According to the rules, the engineer must use synchronous design techniques, by placing synchronous logic at the input and output of all asynchronous sections as shown in Figure II-2-3.

Excessive levels of gates in asynchronous FEs can lead to timing errors. The module supplier

engineers design FPGAs to minimize propagation delays between synchronous FEs. The Toshiba design timing criteria for synchronous circuits state that the input signals should arrive at the gate inputs before the clock period ends, based on the actual clock frequency. In other words, in order to latch the input signal correctly, the input signal to the synchronizing FE shall arrive at the gate inputs far before the next clock signal. Changes due to unequal propagation will have settled out to stable values before the actual operation period elapses, so correct information will be latched into the synchronous FE.

To verify that the FPGAs are designed to minimize propagation delays between synchronous FEs in accordance with this rule, the total timing evaluation for the logic is performed after place and route in the design step. The result of this analysis will be compared to specific design criteria. If the criteria are exceeded, the module supplier will take corrective action as needed.

If the designer of the module supplier implements an incorrect design and the duration for the input signal between synchronizing FEs exceeds the criteria, the signal from the output synchronous FE is likely to not represent the logic associated with the signal from the input synchronous FE. Part of the design simulation activities and FPGA testing activities include actions for the designer to look for such events.

Clock skew within the FPGA can be an issue, depending on the logic design. Clock skew is an important factor in design performance; however, clock skew problems may be independent of operating clock frequency. Clock skew is a key factor in setup and hold time verification of the registers. A large clock skew could lead to hold time violations or incorrect register states. The Microsemi static timing analysis tool performs static timing analysis taking clock skew into account. The clock skew is also evaluated during dynamic timing simulation.

To minimize risks associated with timing, Toshiba performs timing analysis and simulation during their design process. This two-part process includes static timing analysis and dynamic timing simulation. Static timing analysis evaluates the setup and hold times on each path within the FPGA design. The static timing analysis tool evaluates the propagation delay to each element in the code in order to determine each timing path in the code. The results from this static analysis can be interpreted by the FPGA simulation tool program. Engineers of the module supplier then use the FPGA simulation tool on the placed and routed design to validate the design with dynamic simulation, using accurate propagation delays.

Static timing analysis is the most accurate approach to analyze the timing performance of a design. Once static timing analysis is complete, engineers of the module supplier perform dynamic timing analysis using a separate software tool, verifying the results through extensive bench tests.

II-2.1.5.4 Glitches

A glitch is an unwanted fast "spike" in an electronic signal that is produced by timing hazards inherent in a poorly designed circuit. Glitches are undesirable switching activities that occur before a signal settles to its intended value. Glitches can cause incorrect values to be latched by asynchronous circuits within the electronic device. In particular, glitches can cause improper registering of memory values. Therefore, flip-flops are inserted in the logic to implement synchronous logic and avoid timing issues.

Figure II-2-4 shows how a glitch occurs on a basic "static-zero" hazard circuit. During the input transition, the inherent delay of the inverter circuit creates a transient, unintended logical "ON" signal at the inputs of the AND gate for a time equal to the inverter signal propagation delay. This creates a short output glitch from the AND gate, which can cause improper operation of downstream circuits. Complex digital circuits can include embedded circuit element combinations that reduce to the basic static-zero hazard circuit and produce output glitches.

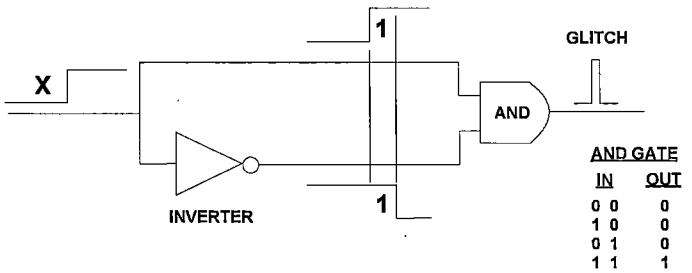


Figure II-2-4 Glitches

Registers are provided as necessary to eliminate glitches. This use of synchronous logic also eliminates other hazard conditions, such as timing errors and metastability. Whenever asynchronous logic is synchronized by a clocked flip-flop, the logic is designed to ensure that the logic has settled to a stable state before clocking the data into the register. Figure II-2-5 shows an example of synchronous design, where the flip-flop in the back-end synchronous FE eliminates a glitch that may be generated in the asynchronous FE.

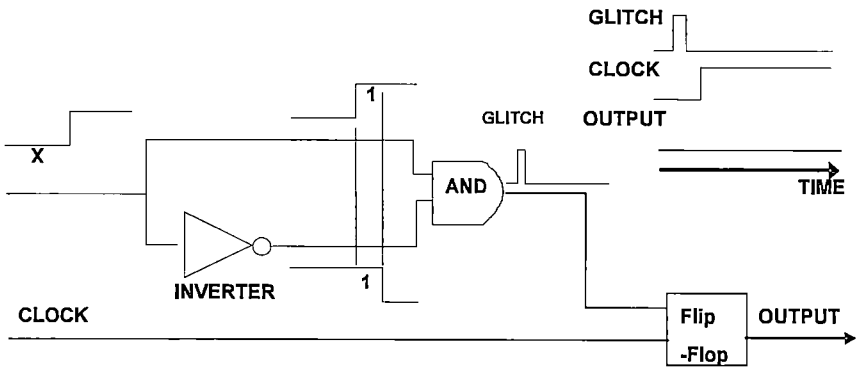


Figure II-2-5 Application of Clocked Flip-Flop

II-2.1.6 Functional Elements

II-2.1.6.1 FE Design and Development

The design and development of an FE starts by reviewing the current FE Library. If the FE necessary for the application is available in the module supplier FE Library, the module supplier makes use of the existing FE. All existing FEs were created using the process outlined below. If a new FE needs to be created, then the module supplier follows the process outlined below as well.

The development activities for each FE consist of the following steps:

1. Define FE requirements and document in an FE Requirements Specification
2. Perform detailed design and document in an FE Specification
3. Prepare an FE Test Procedure
4. Generate a requirements traceability matrix
5. Generate a VHDL source code that implements the FE Specification
6. Perform logic synthesis with optimization and verify that the FE works correctly in simulation
7. Map the FE to an FPGA with appropriate input and output pins and program an FPGA.

8. Perform an FE validation using hardware stimulation of the programmed FPGA, using the same test vector as was used in simulation testing

9. Register the FE into the FE library

Step 1 in developing an FE starts with an FPGA Requirements Specification prepared by NICSD. The FPGA requirements include evaluation of the FPGA-based system Input and Output signals, as well as interfaces and interactions with other FEs. The module supplier develops the FE Requirements Specification based on the FPGA requirements.

The FE Requirements Specification includes functional and interface requirements for the FE. The functional requirements are generally so simple that the requirements are frequently presented in the form of a block diagram. The interface requirements for the FE include the list of input and output signals. The input and output signals of the FE have the data types of "standard logic" and "standard logic vector" as defined in the IEEE Std 1164-1993 "IEEE Standard Multivalue Logic System for VHDL Model Interoperability" (Reference (a41)). The interface description states whether the signal is synchronous or asynchronous. Because most FEs perform a simple function, one FE Requirements Specification may include requirements for multiple FEs.

In Step 2, the design engineer of the module supplier develops the FE Specification (also referred to as a Software Design Description). The FE Specification defines how the requirements specified in the FE Requirements Specification are implemented. In addition, the FE Specification states the criteria to be used for verification and validation of the FE. The FE Specification depicts the FE functions in the form of block diagrams. The block diagrams include the input signals, the internal processes applied on the input signals, and the output signals. The internal processes are implemented with combinatorial logic or sequential logic. The FE Specification includes the code name and code number, which uniquely identifies the FEs. An FE Specification may include specifications for multiple FEs.

In Step 3, a design engineer of the module supplier, who is not the same person who performs the design work for the corresponding FE, prepares the FE Test Procedure for verification and validation. This procedure defines how the requirements defined in the FE Specification are verified, identifies the software tools to be used for embedding the FE logic onto the FPGA chip, and identifies the software tools to be used for exhaustive tests.

In Step 4, the design engineer prepares the Requirements Traceability Matrix, tracing the FE requirements to FE Specification, as well as tracing the FE Test Procedure to the FE

Specification.

In Step 5, the design engineer generates VHDL source code. The FE is coded using text editors to design logic that will implement the specification in FE Specification. The FE coding follows Toshiba's VHDL coding rules established by the module supplier.

In Step 6, the design engineer uses the logic synthesis tool to convert the VHDL source code into optimized gate-level netlists. At this point, the design engineers perform functional testing of the FE to verify that the FE meets the requirements defined in the FE Specification using the FPGA simulation tool. In addition, the design engineer generates the test vectors, the desired output values, and the FE Test Procedure used in Step 8.

Figure II-2-6 is a copy of the graphical output of the FPGA simulation tool for a test of a one-bit full adder, which has three input signals (a_in, b_in, and c_in), and two output signals (s_out and c_out). The left panel shows the three input signals and the two output signals. The line charts drawn on the right show how the signals changed chronologically.

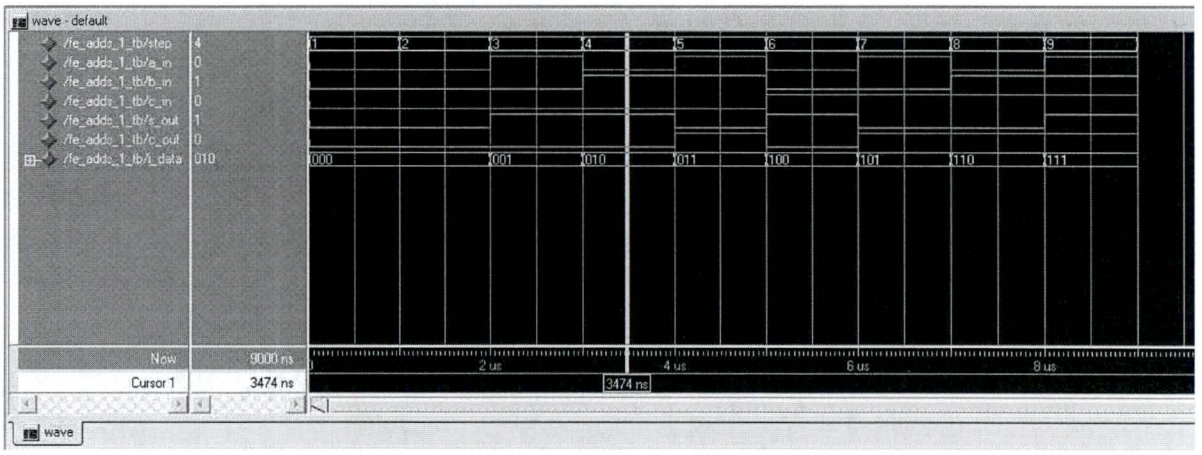


Figure II-2-6 FPGA Simulation Tool Graphical Output for a Test of One Bit Full Adder

In this step, the design engineer verifies correct operation of the FE in the FPGA simulation tool, using the test vectors containing all possible input combinations for functional test coverage. The design engineer verifies that all logic states are correct, and that test coverage is adequate. The test engineer verifies that the test vector toggles each movable digital signal from logic zero to logic one state, and from logic one to logic zero state. The FE validation testing requires a 100% pattern test. That is to say, every possible pattern is applied to the FE, and the outputs from that FE are checked against expected values. Since most FEs are combinational, there is no

issue with memory or states within the FE. For FEs that have internal memoryregisters, test vectors are required to cover all possible patterns including all combinations of internal memory states. The module supplier's engineers create the validation test patterns necessary to test individual FEs. The test vectors contain every possible input combination for the FE. The test vectors are validated on a simulation of the FPGA, using the Microsemi SoC tools provided by Microsemi. The module supplier engineer will then program the FE into an FPGA and validate the configured FPGA using the hardware stimulation tool.

Like FPGAs, FEs are tested in simulation and then embedded in FPGAs, using the same software and hardware that is used on more complex and complete FPGAs. However, testing for FEs is slightly different from testing of FPGAs. For FEs, every possible input combination is applied to the FE, to ensure complete testing. The outputs from that FE are checked against expected values. FEs that implement simple register memories are tested by exhaustive pattern tests. Except in very limited circumstances, feedback is routed through input and output pins outside the FPGA, simplifying testing since the feedback inputs can be set independently as part of the test vector and the feedback outputs verified. Since the remaining FEs are comprised solely of combinatorial logic, there is no need to apply sequences to move through states.

The FE Requirements Specification and the FE Specification will identify one or more logic equations that define the expected output values for all input signal combinations. For very simple logic cells, the test vectors may be generated manually. For logic of any complexity, the test vectors are generated using a spreadsheet. The test vector used for both software- and hardware-based testing is then created from this spreadsheet. For both manually and automatically generated test vectors, the test vectors are generated in a diverse means, and do not depend on the same logic tools used to perform the tests. This alternative means provides checks for the design that would not otherwise exist, if the test vectors were generated by the software tools used to create the FPGAs.

To test the code in the FE, the design engineers prepare an FE Test Procedure prior to testing. The FE Test Procedure includes the desired output values of the FPGA for each test case.

In Step 7, the design engineer embeds the fuse map into an FPGA with the FPGA programming tool.

In Step 8, the design engineer tests the FE in an FPGA integrated circuit using the FPGA adaptor and the hardware stimulation tool. The hardware stimulation tool drives FPGA inputs based on data in the test vectors, which are generated prior to the FE validation testing. The hardware stimulation tool then records the FPGA outputs. The FE test process is detailed in the FE Test

Procedure.

For Steps 6, 7, and 8, software tools are used. The results of software tool errors may not be obvious to the developer. The verification and testing activities and FE Test Reports are carefully reviewed by other design engineers, who are independent of the developer.

In Step 9, each FE is registered into the FE Library after confirming that its FE Test Report is issued and is acceptable. The FE library is controlled using an FE Control Sheet that includes:

- Code number, which uniquely identifies the FE
- Code name
- FE Specification
- FE Test Report
- FE source code file name and the media number
- Netlist file name and the media number
- Name and revision numbers of the software tools used

The design engineers place the FE under configuration control. The FE Control Sheet and electronic media containing the FE and associated design documents are stored in the design group's storage locker.

II-2.1.6.2 FE Verification and Validation

In order to simplify peer review and test design, the module supplier design engineers do not allow the software tools to perform any automatic optimization on the logic circuits built from FEs. However, optimization is allowed on the FEs. The optimized FEs are captured, peer reviewed, tested, and registered in the FE library with this specific optimization.

The verification process for the FEs provides a more traceable, understandable process than would be possible if one verified only when all FEs were integrated into the complete FPGA logic. Because of the simplicity of the FEs, shorter simulations are possible, with thorough verification. By using more thoroughly verified FEs in the complete logic, Toshiba eliminates the need for starting complete verification with more complex, unverified logic. Note that FEs are 100% tested as well as reviewed. The connections of FEs are verified in the design of the FPGA, as described later in the LTR. This extensive testing approach at the FE level minimizes the risk of unobserved problems within the total logic in the FPGA. Toshiba believes that by creating good engineering practices and designs for the FEs and by extensive testing of these designs, the

verification process for the total FPGA improves by finding errors sooner in less complex logic and thus reducing the number of problems from low-level functional errors in more complex logic.

The module supplier verification and validation processes for the FEs include peer reviews and pattern testing. All tests are performed in accordance with the FE Test Procedure. Results and deviations are recorded in the FE Test Report.

The design engineers document any test failures, any product or configuration nonconformance, or any errors in the test procedure itself in accordance with the steps defined in module supplier procedure. The design engineers resolve the problems by modifying design documentation, logic, testing plans, procedures, and test vectors as necessary. The design engineers revise all previous materials and perform reviews as necessary to incorporate the changes, document the amount of retest required for these changes, and perform retests as needed to resolve the problems.

II-2.1.6.3 Unused FPGA Cells

As defined in the Actel (now Microsemi) CDR report (Reference (d33)), the FPGA programming tool is used to program the FPGA and to verify the correct connections of FPGA cells within the FPGA. There are checks that are performed by the FPGA programming tool when the FPGA is first inserted, while the fusemap is being loaded into the FPGA, and while programming is being performed. These checks include the following:

- Verify that the file provided to the FPGA programming tool has a valid checksum.
- Prior to programming, the FPGA programming tool verifies that no antifuses are connected in the FPGA.
- The FPGA programming tool verifies that the file provided was compiled for the type of device installed in the programming port.
- Prior to programming, the FPGA programming tool verifies that the standby current is within specified limits for the device type installed in the programming port.
- While programming, the tool measures the impedance and current of each fuse programmed to verify that the programming succeeded.
- The tool anneals the antifuse using controlled-shape current pulses to enhance quality, reliability, and life. The FPGA programming tool verifies the current flow during the annealing to validate the connection's impedance.

- While programming the FPGA, the FPGA programming tool periodically checks all unprogrammed antifuses within the FPGA and verifies that only the expected antifuses have been programmed, and that the unprogrammed antifuses were not inadvertently programmed by integrated circuit hardware failures.
- While programming the FPGA, the FPGA programming tool periodically checks the quality of the already programmed antifuse connections.
- After programming the FPGA, the FPGA programming tool measures the standby current and verifies that it is still within specified limits to show that the programming did not damage the FPGA.
- After programming the FPGA, the FPGA programming tool verifies that the FPGA outputs work correctly, to ensure that outputs are not shorted together.
- After programming the FPGA, the FPGA programming tool verifies that the checksum read from the FPGA matches that provided by the fuse map file, using proprietary methods.

When one of the tests described above finds an error on an FPGA, the design engineer of the module supplier or the technician of the printed circuit board fabricator who embeds FPGA logic into chip for production discards the FPGA. If the tests succeed, the FPGA is used for testing or stored for future module manufacturing.

II-2.1.7 FPGA Simulation Testing and Creating Test Vector

Toshiba performs simulation testing, using the FPGA simulation tool, on the netlist to create a 100% toggle coverage test vector. The test vectors are prepared so that the FPGA is tested functionally and every operative connection between FEs is tested.

The module supplier design engineer, who is not the same person who performs the design work for the corresponding FPGA logic, is responsible for creating the test vector and FPGA Test Procedure. The design engineer creates the test vector, which is used later for both simulation testing and hardware-based testing. The test vector design starts with testing the complete functional requirements of the logic, including any transitions such as alarm limits. After the design engineer has created an initial test vector to verify all functional requirements, additional test vectors are added repeatedly to verify that each non-static logical connection can toggle from logic zero state to logic one state as well as from logic one state to logic zero state completing the development of the 100% toggle coverage test vector. This toggle testing is performed on simulated logic. The FPGA simulation tool verifies the test coverage percentage for all

non-static connections. The design engineer uses the toggle coverage percentage computed by the tool to judge if the test cases are sufficient and will add test cases until 100% toggle test coverage is achieved. Figure II-2-7 shows a flowchart for developing the 100% toggle test vector.

For simple logic cells, the test vector may be generated manually. For complex logic cells, the test vector may be generated using formulas in a spreadsheet. Both manually and automatically generated test vectors are prepared separate from the FPGA simulation tool.

The FPGA simulation tool is used to simulate the internal operation of the logic, providing the design engineer with the capability to watch individual signals within the FPGA and validate that the FPGA logic works as the design engineer intended.

In order to reduce the occurrence of design flaws, NICSD performs an independent review of the FPGA Test Procedure. The FPGA Test Procedures specify the test equipment used in the FPGA testing as well as the test cases.

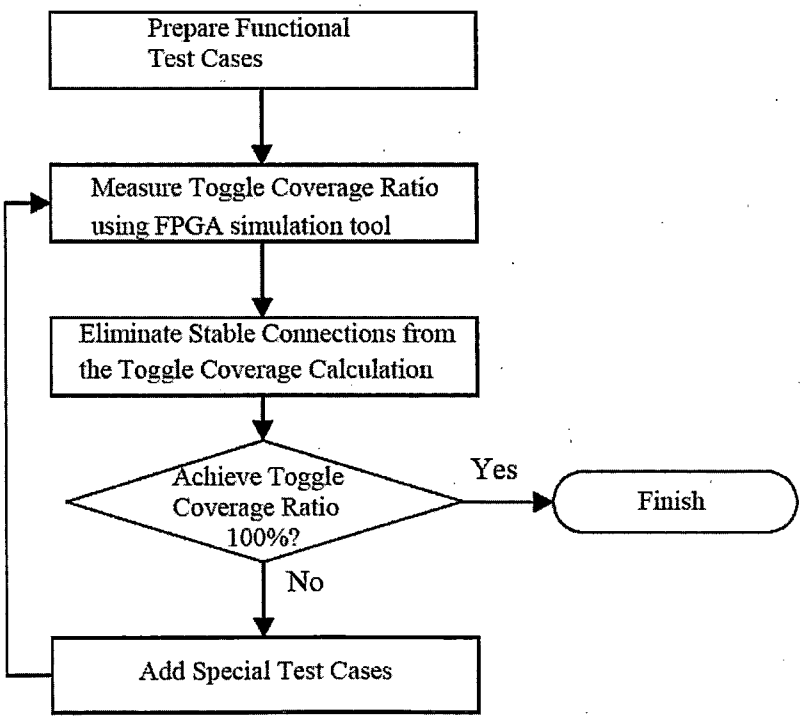


Figure II-2-7 Flowchart for Developing a 100% Toggle Coverage Test Vector

The FPGAs are also toggle tested to verify that the antifuse interconnections between FEs are correct. The toggle tests verify that each of the logic connections that can change between logic zero and one states (i.e., the logic connections that are not forced to logic zero or logic one), can be set into both zero and one states. Due to the large number of possible inputs to the FPGA circuit, it is impractical to test 100% of possible input combinations. Therefore, the design engineer develops a set of test patterns, known as a test vector, which will be used to validate the FPGA.

The design engineer measures the toggle coverage ratio resulting from the functional test cases. Toggle coverage ratio is defined as the number of toggled connections during testing divided by the number of all used non-static connections. Toggle testing is used to ensure that every non-constant connection between FEs toggles and is thus tested in logic zero and one states.

Figure II-2-8 is a copy of graphical output that shows partial results of a toggle test.

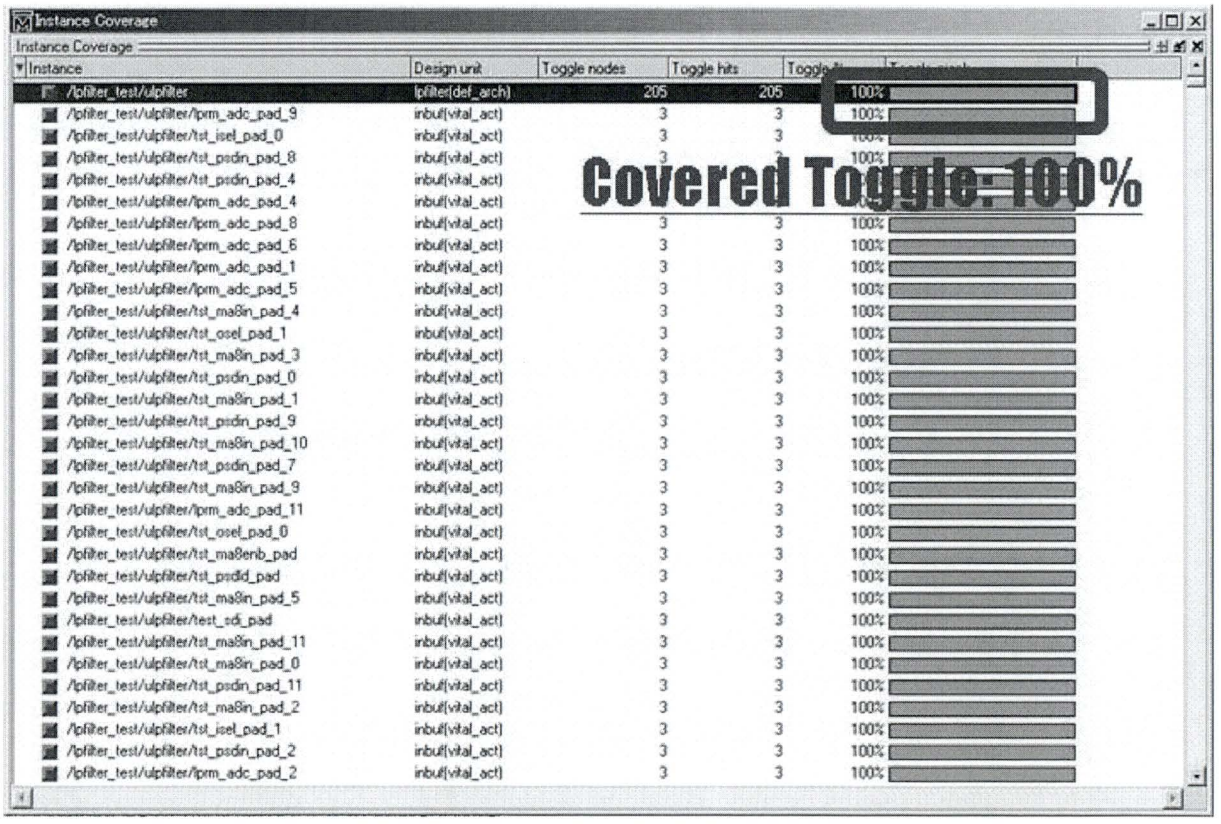


Figure II-2-8 Graphical Output that Shows Partial Results of a Toggle Test

The final test vector is fully verified to ensure the completeness of the logic testing of the FPGA circuit design. NICSD reviews the results of the toggle coverage. NICSD may ask for additional tests, as necessary for both functional test completeness and toggle coverage. NICSD verifies that the functional and toggle tests were sufficient, using the same test vectors applied for both simulation testing of an FPGA and for testing of a programmed FPGA.

II-2.2 Scope of Applications

The PRM for BWRs and OPRM for ABWR are discussed in the following subsections.

II-2.2.1 [Unused]

Figure II-2-9 [Unused]

Figure II-2-10 [Unused]

Figure II-2-11 [Unused]

Table II-2-1 [Unused]

II-2.2.2 Neutron Monitoring System

In this section, the functions, response time, system configuration, Unit/Module configuration, and important design features, are described for the PRM and OPRM systems. PRM and OPRM are both part of the Neutron Monitoring System (NMS).

Section II-2.2.2.1 describes the general functions of the PRM and the OPRM.

Section II-2.2.2.2 provides the response time requirements.

Section II-2.2.2.3 describes the system configuration of the PRM and the OPRM. System configurations for various BWR types are described in Appendix II-A.

Section II-2.2.2.4 describes the Unit/Module configuration of the PRM and the OPRM.

Section II-2.2.2.5 describes design features of the PRM and the OPRM in accordance with Section II-2.2.2.4.

II-2.2.2.1 System Function

The Neutron Monitoring System (NMS) monitors the core neutron flux during shutdown, during fuel loading, and from the startup source range to beyond rated power. The NMS monitors power generation and provides trip signals to the Reactor Protection System (RPS) to initiate

reactor scram under excessive neutron flux (and power) condition (high level), core oscillation, or fast rising neutron flux (short period) conditions.

The PRM and the OPRM systems are discussed in this LTR. The PRM has the following safety-related subsystems:

- Local Power Range Monitor (LPRM)
- Average Power Range Monitor (APRM)

The LPRM monitors local neutron flux at a single in-core detector in the power range between 1 % and 125 % of the rated power. LPRM provides the local neutron flux to APRM and OPRM.

The APRM averages the local power detected by its assigned LPRMs. The averaging circuit automatically corrects for the number of unbypassed LPRMs providing input signals. The APRM also includes a flow measurement function. The flow measurement function receives signals from transmitters, and converts them to the reactor recirculation flow rate. APRM provides a simulated thermal power value in each APRM channel, using a first order time delay to the averaged power. Reactor core flow or recirculation flow signals are used in the APRM to provide the flow biasing for the APRM rod block and simulated thermal power trip setpoint functions.

The OPRM receives the same LPRM signals as the corresponding APRM channel. The OPRM determines whether there is thermal hydraulic instability and provides trip signals to the RPS to trip the plant and thus suppress neutron flux oscillation, prior to violation of safety thermal limits. The LPRMs and APRM combine to form the Power Range Neutron Monitor (PRM). The OPRM algorithm to detect thermal hydraulic oscillation for BWR-3, BWR-4, BWR-5, and BWR-6 is the same as the OPRM for an ABWR. Differences between the ABWR OPRM and the OPRM for older BWR designs are the assignment of LPRM signals to OPRM cells and the parameter setpoint. Therefore, the ABWR OPRM can be applied to OPRM for an older BWR design with only the FPGA logic changes required for the change of the number of LPRM signals used in the calculation and the change of the setpoint.

II-2.2.2.2 Response Time

II-2.2.2.2.1 Power Range Neutron Monitor (PRM)

The response time of the PRM shall be as follows.

1. APRM Upscale Flux Trip

The APRM Upscale Flux Trip response time from the change of the LPRM input signal above the setpoint limit to the occurrence of trip from Relay unit shall not exceed 40 ms.

2. Simulated Thermal Power Upscale Trip
   The Simulated Thermal Power Upscale Trip response time from the simulated thermal power exceeding the setpoint limit to the occurrence of trip from Relay unit shall not exceed 40 ms.

II-2.2.2.2.2 Oscillation Power Range Monitor (OPRM)

The response time of the OPRM shall be as follows.

- The OPRM trip response time from when the core oscillation is detected by LPRM detectors through LPRM subsystem to when the OPRM trip function is initiated from the Relay unit shall not exceed [ ]^{a,c}ms.
- The OPRM trip response time from when the core oscillation initiation detected by LPRM detector is input to the OPRM unit to when the OPRM trip function is initiated from the OPRM unit shall not exceed [ ]^{a,c}ms.

II-2.2.2.3 System Configuration

The LPRM and APRM are configured in multiple divisions in BWRs. The LPRMs provide data to specific, assigned divisions of APRM and OPRM. Each LPRM detector can be individually bypassed, with a minimum required number of LPRMs in each division. Each LPRM detector assembly contains four LPRM detectors, monitoring four distinct levels in the reactor core. Each LPRM detector assembly provides one LPRM input to each APRM and OPRM channel in the same division. LPRM detectors are mapped to divisions to ensure that each APRM and OPRM channel has a representative view of the reactor core. In large core designs, each LPRM detector in each assembly is mapped to a different division.

There are six or eight channels of APRM in some BWR designs, with each channel providing a trip signal to the RPS. In other BWR designs, the APRMs are divided into two groups. In other designs, there is an APRM and OPRM in each of the four divisions. When more than one APRM provides trip signals in the appropriate groups, the Reactor Protection System (RPS) initiates a reactor scram. The redundancy criteria are met so that in the event of a single failure under permissible APRM channel bypass conditions, a scram signal will still be generated in the RPS as required. Thus, the IEEE Std 603 Single Failure Criterion (Clause 5.1) is satisfied.

There are independent and redundant channels of OPRM. The above APRM channel redundancy condition also applies to OPRM channels. Bypassing a division of APRM bypasses the same division of OPRM. The OPRM trip outputs are separate from the APRM trips to RPS, satisfying the IEEE Std 603 Single Failure Criterion (Clause 5.1). The arrangement and assignment of LPRMs provides core region monitoring by redundant OPRM channels.

Figure II-2-13 shows a typical configuration of the PRM and OPRM for some BWR designs.

Figure II-2-12 [Deleted]

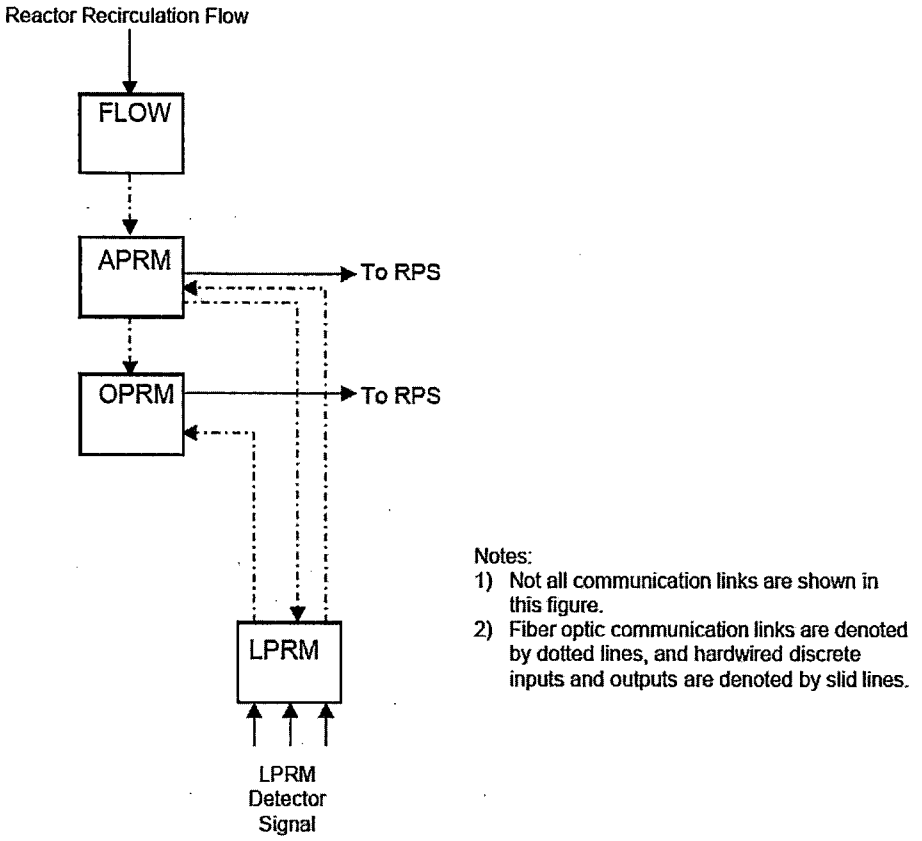


Figure II-2-13 Overview of System Configuration of PRM and OPRM (BWR)

II-2.2.2.4 Unit/Module Configuration

This section describes Unit/module configuration of the PRM and OPRM. Figure II-2-14 shows the typical Module and Unit configurations of the PRM in a BWR-5. Figure II-2-16 shows the configuration for an OPRM in an Advanced Boiling Water Reactor (ABWR). Table II-2-2 lists modules used in the BWR-5 PRM system. Table II-2-4 lists modules used in the ABWR OPRM. The table is consistent with the Module and Unit configuration shown in Figure II-2-14 and Figure II-2-16.

Appendix II-A describes the detailed configuration for the application of PRM and OPRM in various other BWR designs.

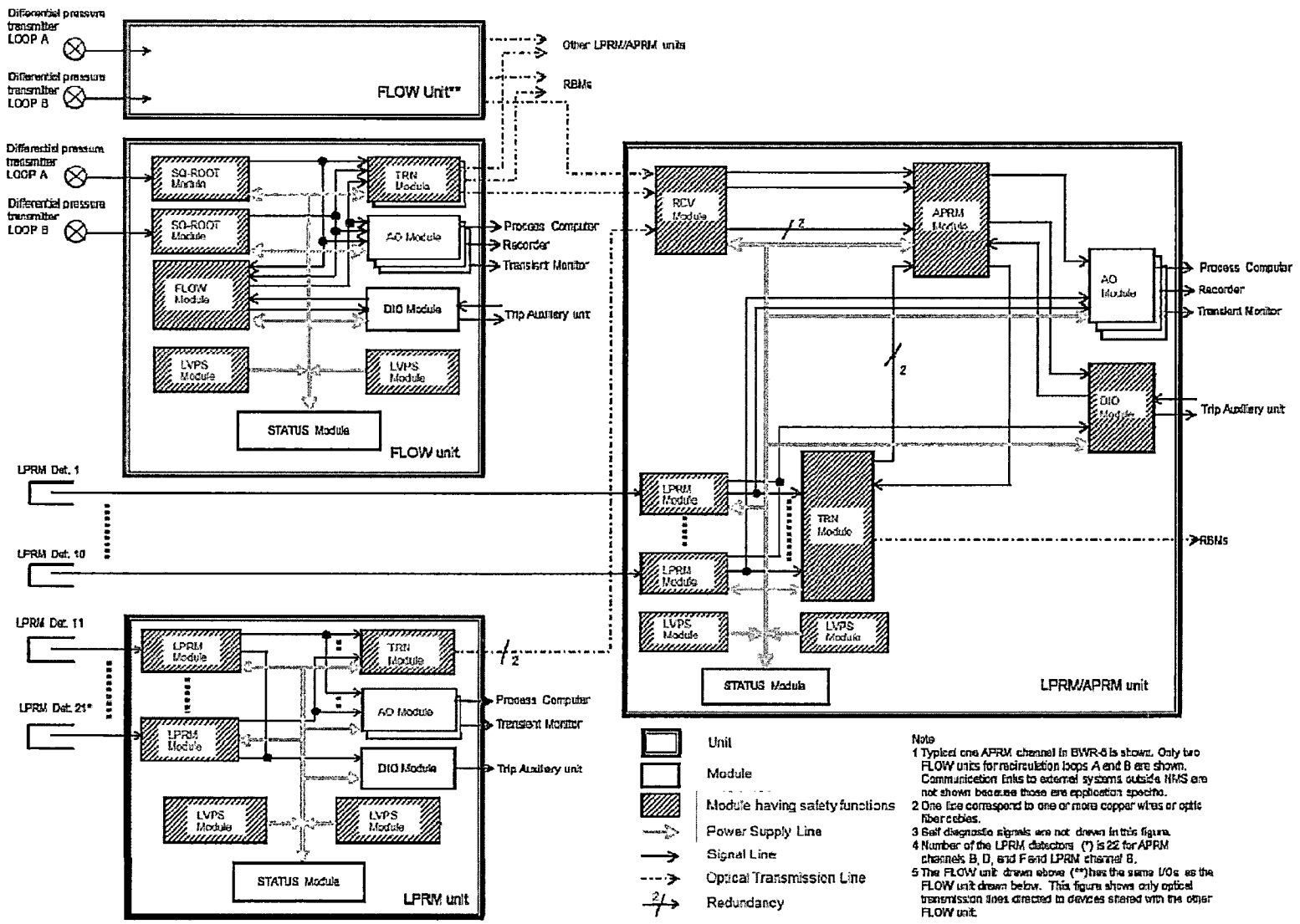


Figure II-2-14 Module and Unit Configuration of PRM for BWR-5 (OPRM Not Shown)

Figure II-2-15 [Deleted]

Table II-2-2 Module List for a BWR-5 PRM (OPRM Not Shown)

Module Name	Module Model Number*1	Number of Applied Module for System Configuration shown in Figure II-2-14		Functional Description
		Total Number	Description Note: The system consists of 6 APRM channels (A through F) with 1 LPRM/APRM unit and 1 LPRM unit in each APRM channel, 2 LPRM channels (A and B) with 2 LPRM units in each LPRM channel, and 4 FLOW units. There are 6 APRM/LPRM units, 10 LPRM units and 4 FLOW units in the system.	
LPRM Module	HNS013 B00000	172	- 11 modules in an LPRM unit and 10 modules in an LPRM/APRM unit for APRM A, C, and E channel - 12 modules in an LPRM unit and 10 modules in an LPRM/APRM unit for APRM B, D, and F channels - 11 modules in the first LPRM unit and 10 modules in the second LPRM unit in LPRM A channel - 12 modules in the first LPRM unit and 10 modules in the second LPRM unit in LPRM B channel	LPRM function
APRM Module	HNS020 B00000	6	- 1 module in an LPRM/APRM unit	APRM function
SQ-ROOT Module	HNS030 B00000	8	- 2 modules in a FLOW unit	Square root arithmetic function
FLOW Module	HNS040 B00000	4	- 1 module in a FLOW unit	Recirculation-flow calculation, trip and alarm functions
STATUS Module	HNS091 B00000	6	- 1 module in an LPRM/APRM unit	Data reception status and power supply voltage monitoring status indications.
STATUS Module	HNS093 B00000	14	- 1 module in an LPRM unit - 1 module in a FLOW unit	Power supply voltage monitoring status indication
MUX Module	HNS260 B00000	2	- 1 module in one of the 2 LPRM units in an LPRM channel	Multiplexing module for LPRM data transmission
BLANK Module	HNS490 B00000	12	- 2 modules in an LPRM unit for APRM A, C, and E channels - 2 modules in one of the 2 LPRM units in LPRM A channel - 1 module in an LPRM unit for APRM B, D, and F channels - 1 module in one of the 2 LPRM units in LPRM B channel	Dummy LPRM modules fill the open slots when there are not 13 installed LPRM Modules.
LVPS Module	HNS500 B00000	40	- 2 modules in each unit in the system	+5V and ±15V power supply to each module
AO Module	HNS515 B00000	16	- 1 module in an LPRM/APRM unit - 1 module in an LPRM unit	Analog outputs to the Transient Monitor

Module Name	Module Model Number*1	Number of Applied Module for System Configuration shown in Figure II-2-14		Functional Description
		Total Number	Description Note: The system consists of 6 APRM channels (A through F) with 1 LPRM/APRM unit and 1 LPRM unit in each APRM channel, 2 LPRM channels (A and B) with 2 LPRM units in each LPRM channel, and 4 FLOW units. There are 6 APRM/LPRM units, 10 LPRM units and 4 FLOW units in the system.	
AO Module	HNS516 B00000	10	- 1 module in an LPRM/APRM unit - 1 module in a FLOW unit	Analog outputs to recorders
AO Module	HNS517 B00000	4	- 1 module in a FLOW unit	Analog outputs to the Transient Monitor
AO Module	HNS518 B00000	20	- 1 module in each unit in the system	Analog outputs to the process computer
DIO Module	HNS520 B00000	20	- 1 module in each unit in the system	Discrete signal input and output module
TRN Module	HNS0531 B00001	24	- 1 module in an LPRM/APRM unit - 1 module in an LPRM unit - 2 modules in a FLOW unit	Optical data transmission module
RCV Module	HNS0541 B00001	8	- 1 module in an LPRM/APRM unit - 1 module in one of the 2 LPRM units in an LPRM channel	Optical data reception module

*1: Each Module has a Type number for configuration control. When a module design is changed, a type number of each module is changed to a new revised, unique type number.

Table II-2-3 [Deleted]

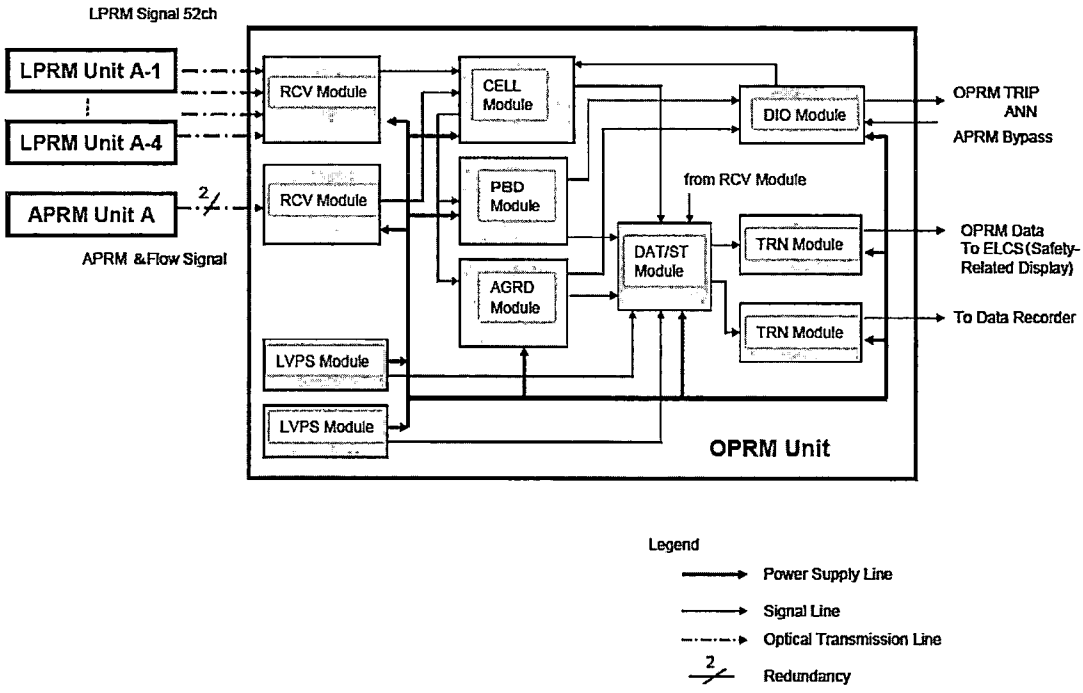


Figure II-2-16 Module and Unit Configuration of OPRM for ABWR

Table II-2-4 Module List for an ABWR OPRM

Module Name	Module Model Number*1	Number of Applied Module for OPRM System Configuration shown in Figure II-2-16		Functional Description
		Total number	Description Note: The system has 4 divisions with 1 OPRM unit in each division.	
CELL Module	HNS0400 B00000	4	- 1 module in each OPRM unit	LPRM Levels are converted to Normalized Oscillation Signal
DAT/ST Module	HNS0410 B00000	4	- 1 module in each OPRM unit	Power status and Input status indications OPRM data are multiplexed
AGRD Module	HNS0420 B00000	4	- 1 module in each OPRM unit	Amplitude-Based Detection Algorithm is performed. Growth Rate-Based Detection Algorithm is performed.
PBD Module	HNS0430 B00000	4	- 1 module in each OPRM unit	Period-based Detection Algorithm is performed.

Module Name	Module Model Number*1	Number of Applied Module for OPRM System Configuration shown in Figure II-2-16		Functional Description
		Total number	Description Note: The system has 4 divisions with 1 OPRM unit in each division.	
LVPS Module	HNS0500 B00000	8	- 2 modules in each OPRM unit	+5V and ±15V power supply to each module
DIO Module	HNS0520 B00000	4	- 1 module in each OPRM unit	Discrete signal input and output module
TRN Module	HNS0531 B00001	8	- 2 modules in each OPRM unit	Optical data transmission module
RCV Module	HNS0541 B00001	8	- 2 modules in each OPRM unit	Optical data reception module

*1: Each Module has a Type number for configuration control. When a module design is changed, a type number of each module is changed to a new revised, unique type number.

Figure II-2-17 [Unused]

Table II-2-5 [Unused]

II-2.2.2.5 Design Features of PRM and OPRM

II-2.2.2.5.1 Interface with Field Sensors and Actuators

(1) LPRM UNIT in PRM

a. Analog Input Interface
The LPRM unit has analog input interface to receive one low level analog signal representing nuclear flux at the detector. The analog interface also provides power to the sensor. This interface also provides high voltage to bias the detector.

b. Optical Transmission Output Interface
The LPRM unit has a fiber optic transmitter interface to provide broadcast data to external safety or non-safety systems, such as the Engineered Safety Features System and the Transient Data Recorder, respectively. However, these interfaces are plant specific and vary depending on the application.

(2) LPRM/APRM Unit in PRM

a. Analog Input Interface
The APRM unit has a low level analog input interface to receive analog signals.

b. Analog Output Interface
The APRM unit has an analog output interface to generate analog signals.

c. Discrete Input Interface
The APRM unit has a discrete input interface to receive digital signals.

d. Discrete Output Interface
The APRM unit has a discrete output interface to generate digital signals. The output interface requires external power.

e. Optical Transmission Input Interface
The APRM unit has fiber optic receivers to accept LPRM and FLOW data within a division.

f. Optical Transmission Output Interface
The APRM unit has fiber optic transmitter interfaces to provide broadcast data to the OPRM and other external safety or non-safety systems. However, these interfaces are plant specific and vary depending on the application.

(3) FLOW Unit in PRM

a. Analog Input Interface
The FLOW unit has an analog input interface to receive analog signals.

b. Analog Output Interface
The FLOW unit has an analog output interface to generate analog signals.

c. Discrete Input Interface
The FLOW unit has a discrete input interface to receive digital signals.

d. Discrete Output Interface
The FLOW unit has a discrete output interface to generate digital signals. The output interface requires external power.

e. Optical Transmission Output Interface
The FLOW unit has fiber optic transmitter interfaces to provide broadcast data to the Rod Block Monitor (RBM) unit and APRM unit. However, these interfaces are plant specific interface and vary depending on the application.

(4) OPRM Unit in OPRM

a. Discrete Input Interface
The OPRM unit has a discrete input interface to receive digital signal.

b. Discrete Output Interface
The OPRM unit has a discrete output interface to generate digital signals.

c. Optical Transmission Input Interface
The OPRM unit has fiber optic receivers to accept LPRM data within a division.

d. Optical Transmission Output Interface
The OPRM unit has fiber optic transmitter interfaces to provide broadcast data to other external safety or non-safety systems.

II-2.2.2.5.2 Power Supply

The PRM and OPRM have redundant Low Voltage Power Supply (LVPS) modules in the following units:

- Flow Unit

- LPRM Unit
- LPRM/APRM Unit
- OPRM Unit

The redundant LVPS Modules supply +5 V DC and ±15 V DC within the unit.

The requirements for external power source are described in Section II-2.2.3.1.3

II-2.2.2.5.3 Annunciation of Failures

The PRM and OPRM each generate a divisional Inoperative signal when faults occur that affect the execution of the safety functions. The APRM Unit and OPRM Unit have LED indicators on their front panels to show the generation of each Inoperative signal. The LPRM Inoperative signals are transferred to the APRM unit through fiber optic communication links. The APRM Inoperative and the OPRM Inoperative are transferred by relays to the RPS to be used in the voting for a reactor trip.

Each Inoperative Signal is defined in the Equipment Design Specifications for each application.

II-2.2.2.5.4 Boundary between Safety and Non-Safety

The PRM and OPRM provide data to non-safety system through qualified isolators using hardwired relays and unidirectional fiber optic communication links.

Figure II-2-14 and Figure II-2-16 depict these boundary points.

II-2.2.3 FPGA Application Principles

The FPGA-based systems have been designed in large part based on four essential design principles: (1) redundancy, (2) independence, (3) the need for defined determinism in data processing and communication, and (4) implementation of a diversity and defense-in-depth (D3) philosophy, as well as one subjective attribute - simplicity. The four principles and one attribute are embodied in the underlying basis of IEEE Std 603 (Reference (a36)).

The discussion in this section is structured to summarize the key design features of the FPGA-based platform to address each principle above in the design of application systems such as PRM and OPRM.

II-2.2.3.1 Redundancy

The PRM and OPRM implementation in the FPGA based systems conforms to the Single Failure Criterion (Clause 5.1) of IEEE Std 603 (Reference (a36)). To meet this criterion, the redundancy designed into each of these systems is discussed below.

II-2.2.3.1.1 [Deleted]

II-2.2.3.1.2 PRM and OPRM

For the BWR-5 PRM used as an example in this LTR, APRM channels are divided into two groups where each group consists of multiple APRM channels. Because of the different core sizes, APRM channels and groups are application specific for other BWR designs. When more than one APRM channel provides a trip signal in both groups, the Reactor Protection System initiates a reactor scram. The redundancy criteria are met so that in the event of a single failure under permissible APRM channel bypass conditions, a scram signal will still be generated in the RPS as required. Thus, the IEEE Std 603 Single Failure Criterion (Clause 5.1) is satisfied.

There are independent and redundant channels of OPRM. The above APRM channel redundancy condition also applies to OPRM channels. Bypassing a division of APRM bypasses the same division of OPRM. The OPRM trip outputs are separate from the APRM trips to RPS, satisfying the IEEE Std 603 Single Failure Criterion (Clause 5.1). The arrangement and assignment of LPRMs provide core regional monitoring by redundant OPRM channels.

II-2.2.3.1.3 Power Supply Redundancy

Power supply redundancy of the PRM and OPRM is provided through two redundant LVPS power supply modules in each unit. A loss of one LVPS module power supply will neither inhibit protective action nor cause a scram, satisfying the IEEE Std 603 (Reference (a36)) Single Failure Criterion (Clause 5.1).

Divisional Class 1E AC vital power is assumed to be supplied to the cabinet of PRM and OPRM. The AC vital power supplied to the cabinet is converted to 220VDC power by appropriate AC/DC converters and supplied to the LVPS modules in PRM and OPRM units.

II-2.2.3.2 Independence

Each division of PRM and OPRM can accomplish its safety function regardless of the operability or adverse impact of other redundant divisions or other systems. For PRM and OPRM,

functional, physical, electrical, and communication independence exists between redundant safety-related divisions; between each safety-related division and other divisions in other safety-related systems; and between safety-related systems and non-safety-related systems.

Data independence is exhibited in PRM and OPRM by the fact that only votes to trip and status information are provided across divisional boundaries for the PRM and OPRM being evaluated in this topical report. LPRM levels are provided across divisional boundaries in the BWR-3 PRM (see Section II-A-7.3) and the small core OPRM (see Section II-A-7.8). The data link information is transmitted in packets with a fixed length, fixed content, and predefined format. Failures in the communication links do not adversely affect operation of the divisions receiving malformed, incorrect, or inappropriate data messages.

II-2.2.3.2.1 Physical and Electrical Independence

Each of the divisions of PRM and OPRM is physically separated from the other redundant divisions. The PRM and OPRM systems comply with the criteria set forth in IEEE Std 603 (Reference (a36)), Clause 5.6 and follow the guidance of Regulatory Guide 1.75 (Reference (a9), which endorses IEEE Std 384 (Reference (a34)). Class 1E circuits are identified and separated from redundant circuits and non-Class 1E circuits. Qualified electrical isolation devices are provided in the design when an interface exists between redundant Class 1E divisions and between non-Class 1E and Class 1E circuits.

Physical and electrical independence of the instrumentation devices of the system is provided by channel independence for sensors exposed to each process variable. Trip logic outputs are separated in the same manner as the channels. Class 1E isolators, including fiber optic cables, electrically and physically isolate signals between redundant PRM and OPRM divisions.

II-2.2.3.2.2 Communications Independence

The modules used to construct the PRM and OPRM communicate using dedicated communication links internal to the division. Each communication link has its own independent communications buffer.

The communication data links to be provided to systems external to the PRM and OPRM use uni-directional fiber optic communication links from each division. The communication links provide only fixed data sets to the non-safety-related systems, provide Class 1E to non-Class 1E electrical and functional isolation, and offer no possibility of data transfer from the non-safety to safety equipment during normal operation.

The FPGA-based PRM and OPRM system includes self-diagnostic functions that continuously verify proper FPGA and communications performance, and provide outputs used to alert the operator. If a failure is detected, the unit is marked as inoperable (i.e., tripped). When the predetermined divisions or channels are in a tripped state, the voting logic in the RPS will cause the safety function to occur.

Each safety-related PRM and OPRM division communicates data and status to the non-safety-related systems through dedicated communication interfaces in each division's modules. The communication interface for each division consists of uni-directional fiber optic communication links that broadcast fixed data sets from each safety division to the non-safety-related systems. The communication interface is designed to prevent any data transfer from the non-safety systems to the originating safety-related division. The fiber optic cable provides electrical isolation, and the fiber optic transmitter provides the functional isolation.

No other capabilities exist for communication with external devices. Communications information specific to PRM and OPRM is discussed briefly below in the following subsections.

II-2.2.3.2.3 [Unused]

II-2.2.3.2.4 PRM and OPRM

There is no communication between redundant divisions in the PRM or OPRM except sharing LPRM levels between divisions in the BWR-3 PRM (see Section II-A-7.3) and the small core OPRM (see Section II-A-7.8).

The LPRM monitors neutron flux in the power range. For each PRM or OPRM division/channel, the LPRMs monitor neutron flux levels from the hardwired LPRM detector inputs. Each division has a number of LPRM detectors and LPRM modules that provide data to the APRM and OPRM. The number of LPRM detectors is different depending on the BWR model. The LPRM modules in one division communicate internally with the APRM in that division over uni-directional fiber optic communication links, providing fixed data sets of LPRM information.

For each division, the OPRM receives local power level data from the divisional LPRMs and core flow and average power level data from the same divisional APRMs over uni-directional fiber optic communication links. The divisions of the OPRM trip protection algorithm independently detect thermal hydraulic instability and provide hardwired, discrete (vote to trip only) signals to all divisions of the voter logic to be provided in the RPS. The qualified PRM does not include the capability of receiving Gain Adjustment Factors from an external non-safety related computer.

II-2.2.3.3 Determinism

The response time requirement for each PRM and OPRM safety-related function is determined by the safety analysis. The response time must be predictable and repeatable to be considered deterministic. The response time for all PRM and OPRM safety functions is deterministic. A description of the FPGA platform features that make the PRM and OPRM response deterministic is provided below.

The PRM and OPRM designs use multiple FPGAs on some modules. To enhance testability and reduce undesirable circuit behavior, the basic architecture within each FPGA is a clocked sequential circuit, with periodic synchronizing registers within the FPGAs. Each FPGA only starts processing data when data is transferred into that FPGA, and sends data to the next FPGA or module when processing is completed. Thus, the functions in a given module are executed in sequence in a manner that is inherently deterministic, based on the clocked sequence. The first FPGA completes its function, and then provides data to the next FPGA. When that FPGA completes its function, it provides data to the next FPGA. In addition, when all signal processing FPGAs have finished passing data to the next, the signal processing watchdog timer on the module resets and restarts timing. Failure of a signal processing FPGA to complete and pass data to the next FPGA will result in all subsequent FPGAs on that module failing to start. If this occurs in the FPGAs that implement the signal processing and thus the safety functions, the watchdog timer times out and the module is marked as failed. The failed module trips the division and generates an alarm to the operator. A predetermined number of tripped divisions will result in a reactor scram through the RPS voting arrangement.

Because FPGAs are arrays of logic cells and registers, each cell connected in series adds defined delay to the logic circuit. As a result, the logic within each FPGA is designed, verified, and validated to ensure operation within timing constraints, under expected operating conditions. The clocked synchronous design is used within each FPGA to avoid timing errors and to ensure timing constraints are satisfied. For synchronous design, changes of state within the FPGA occur only at selected times, controlled by the clocked timing signal. The logic within each FPGA is designed to ensure that the design provides adequate shaping on the inputs to the FPGA.

To avoid timing errors within FPGAs, analysis and simulation are performed during the design process. This two-part process includes static timing analysis and dynamic timing simulation. Static timing analysis demonstrates that the setup and hold times on each path within the FPGA design are within predetermined parameters. Software tools used to perform the static timing analysis also are used to evaluate the propagation delay to each element in the FPGA to confirm each timing path in the FPGA is within predetermined parameters. In addition, Toshiba uses a

set of dynamic simulation software tools to validate the placed, routed design, using predetermined, accurate FPGA-location specific propagation delays, which Microsemi sets into the software tools based on the characteristics of the cells and paths inside the FPGA. These analyses provide data to the designer to verify that appropriate logic implementation has been achieved, eliminating any potential concerns regarding signal races, signal setup and hold times, and clock skew. A report is generated for implementation including safety analyses.

The communication protocols used in the FPGA platforms are deterministic because they are pre-defined, fixed length, fixed format, and generated at specific times in the FPGA logic execution. The communication links that perform safety functions include data and time out error checking to ensure determinism. All detected errors are alarmed. The communication protocols and logic in the communication receivers include self-diagnostics that will generate module failure signals upon detection of communication failures, alerting operators.

In summary, the FPGA-based PRM and OPRM are deterministic. The PRM and OPRM does not utilize any non-deterministic data communication, non-deterministic computation, interrupts, multitasking, dynamic scheduling, or event driven design. The logic design of the FPGA circuits is fixed and clocked. The response times for the system elements, including architecture, communications (including timing and loading) and processing elements are tested to verify that the systems' performance characteristics are consistent with the safety requirements established in the design basis for these systems. Toshiba performs these analyses to satisfy the design timing requirements in Clause 4.10 of IEEE Std 603 (Reference (a36)). Toshiba generates a report to document the timing analysis.

II-2.2.3.4 Diversity

Diversity is the responsibility of the overall NSSS designer or licensee. The PRM and OPRM do not provide diversity within a given channel.

II-2.2.3.5 Simplicity

The FPGA-based PRM and OPRM were designed for simplicity. The systems have some analog circuits that process detector signals as inputs. The analog signals are converted to digital signals and then processed by FPGA circuits. Toshiba constructs the FPGA circuits in discrete logic blocks that are similar to the analog and discrete relay circuits in existing operating plants. The FPGA-based PRM and OPRM implement the required functionality in fixed gates with deterministic timing that cannot be changed after being programmed at the vendor facility. The FPGA-based PRM and OPRM were designed such that non-safety-related equipment cannot

control or influence the operation of safety-related functions. Non-safety-related functions are not performed in the safety-related equipment, which simplifies the safety-related equipment by elimination of non-essential functionality. Data can only be transferred from each safety division over independent, uni-directional communication links to non-safety-related equipment for several purposes, including diverse display of safety data, preserving data for historical purposes, and performing channel cross checks. This transfer of data shifts these complex activities to the non-safety equipment, preserving simplicity in the safety systems. Thus, the PRM and OPRM design satisfies the subjective attribute of simplicity.

Figure II-2-18 [Unused]

Figure II-2-19 [Unused]

II-2.2.4 Qualified Module List

Table II-2-6 provides the qualified module list for the BWR-5 PRM and ABWR OPRM modules described in this LTR. Modules indicated in Table II-2-6 in bold font with a dot pattern background have been completely qualified are shown. The MUX module (HNS260B00000. shown without the dotted pattern in the table) transmits LPRM levels to external equipment. The MUX module was not included in the BWR-5 PRM equipment qualification testing. If the MUX module is required, the MUX module will be qualified and licensed by the utility. Toshiba will use test results from existing equipment qualification, as applicable. For example, a future module development would require additional electromagnetic compatibility testing but Toshiba might be able to use existing seismic or environmental qualification test results to demonstrate qualification, with Toshiba's justification depending on the significance of the change.

Table II-2-6 also indicates that multiple Input and Output modules are designed and used commonly in multiple units. The TRN module (HNS0531B00001) and the RCV module (HNS0541B00001) with Cyclic Redundancy Check (CRC) functions that were qualified in the OPRM qualification as described in Section III-5.3 can be applied to the BWR-5 PRM. Accordingly, the TRN module (HNS0531B00001) and the RCV module (HNS0541B00001) are also listed as qualified modules for BWR-5 PRM.

Table II-2-7 provides the cross-references that show the systems and the units where each module is used.

Table II-2-6 List of Modules

System	Unit	Module							
		I/O Function		Comunication Function		Signal Processing		Power Supply	
		Module Name	Type Number	Module Name	Type Number	Module Name	Type Number	Module Name	Type Number
BWR-5 PRM	LPRM	DIO	HNS520 B00000	TRN	HNS531 B00001	LPRM	HNS013 B00000	LVPS	HNS500 B00000
		AO	HNS515 B00000	RCV	HNS541 B00001	STATUS	HNS093 B00000		
		AO	HNS518 B00000			BLANK	HNS490 B00000		
						MUX	HNS260 B00000		
	LPRM/APRM	DIO	HNS520 B00000	TRN	HNS531 B00001	LPRM	HNS013 B00000	LVPS	HNS500 B00000
		AO	HNS515 B00000	RCV	HNS541 B00001	APRM	HNS020 B00000		
		AO	HNS516 B00000			STATUS	HNS091 B00000		
		AO	HNS518 B00000						
	FLOW	DIO	HNS520 B00000	TRN	HNS531 B00001	SQ-ROOT	HNS030 B00000	LVPS	HNS500 B00000
		AO	HNS516 B00000			FLOW	HNS040 B00000		
		AO	HNS517 B00000			STATUS	HNS093 B00000		
		AO	HNS518 B00000						
ABWR OPRM	OPRM	DIO	HNS520 B00000	TRN	HNS531 B00001	CELL	HNS0400 B00000	LVPS	HNS500 B00000
				RCV	HNS541 B00001	AGRD	HNS0420 B00000		
						PBD	HNS0430 B00000		
						DAT/ST	HNS0410 B00000		

Table II-2-7 Cross Reference Table of Modules

Module Name	Type Number	Module Has FPGA ?	System used	Unit used
LPRM	HNS013 B00000	yes	PRM(BWR-3,4,5,6)	LPRM, LPRM/APRM, FLOW, SRNM
APRM	HNS020B00000	yes	PRM(BWR-3,4,5,6)	LPRM/APRM
SQ-ROOT	HNS030B00000	yes	PRM(BWR-3,4,5,6)	FLOW
FLOW	HNS040B00000	yes	PRM(BWR-3,4,5,6)	FLOW
STATUS	HNS091B00000	yes	PRM(BWR-3,4,5,6)	LPRM/APRM
STATUS	HNS093B00000	yes	PRM(BWR-3,4,5,6)	LPRM, FLOW
MUX	HNS260B00000	yes	PRM(BWR-3,4,5)	LPRM
TRN	HNS0531B00001	yes	OPRM, PRM(BWR-3,4,5,6)	OPRM, LPRM, LPRM/APRM, FLOW
RCV	HNS0541B00001	yes	OPRM, PRM(BWR-3,4,5,6)	OPRM, LPRM, LPRM/APRM
LVPS	HNS500B00000	no	PRM, OPRM	LPRM, LPRM/APRM, FLOW, OPRM
AO	HNS515B00000, HNS516B00000, HNS517B00000, HNS518B00000	no	PRM(BWR-3,4,5,6)	LPRM, LPRM/APRM, FLOW
DIO	HNS520 B00000	no	PRM(BWR-3,4,5,6), OPRM	LPRM, LPRM/APRM, FLOW, OPRM
BLANK	HNS490 B00000	no	PRM(BWR-3,4,5,6)	LPRM
CELL	HNS0400 B00000	yes	OPRM	OPRM
DAT/ST	HNS0410 B00000	yes	OPRM	OPRM
AGRD	HNS0420 B00000	yes	OPRM	OPRM
PBD	HNS0430 B00000	yes	OPRM	OPRM

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II-A-1 Introduction

This application guide provides generic guidelines and data for applying the Toshiba Non-Rewritable Field Programmable Gate Array (NRW-FPGA) based safety-related equipment in a nuclear power plant. The guidance provided in this document is intended to simplify use and application by consolidating design requirements, operational limitations, and other important data derived from the generic qualification program. Toshiba has used the NRW-FPGA-based equipment to build a Boiling Water Reactor-5 (BWR-5) Power Range Neutron Monitoring (PRM) system as well as an Advanced Boiling Water Reactor (ABWR) Oscillation Power Range Monitor (OPRM) system. Using the hardware and modified programmable logic, the PRM system or OPRM system can be supplied for BWR-3, BWR-4, BWR-5, BWR-6, and ABWR designs.

The requirements and limitations of each system shall be considered when the system is applied to a plant-specific application. Where a Toshiba NRW-FPGA-based system is installed to replace existing equipment in multiple channels (divisions), the existing channel independence and separation can be retained, shall not be compromised, and, depending on rules and regulations, additional independence and separation can be supported in the Toshiba-supplied systems.

Guidelines are provided for design, licensing, installation, operation, and maintenance of the system. Many of the guidelines in this document are interrelated. As an example, consider the generation of fault alarms. The fault alarm has implications in design, operating and maintenance procedures, plant interface, main control room impacts, and several other seemingly unrelated topics, including system power supply and core damage frequency. Therefore, the guidelines should be considered as a whole, rather than in separate, individual pieces.

In addition to the guidelines presented in this document, the system specific manufacturer's recommendations in the User's Manuals and/or System Operations and Maintenance (O&M) manuals provided by Toshiba shall be implemented.

II-A-2 System Design Guidance

The system-specific and plant-specific User's Manual and/or System O&M Manual provide technical information on the application, operation, and maintenance of the systems. This application guide provides generic guidelines and data for applying these systems in nuclear power plants.

II-A-2.1 Power Supply

Each system has been validated to operate from redundant AC sources operating between 90 to 150V AC and over a frequency range of 57 to 63 Hz.

During system startup, the power on the reset circuit for each module monitors the input voltages, and the FPGAs are held in a reset state until the DC power supply voltages are within specified bounds. This prevents spurious signals on the device outputs from occurring before stable module performance is achieved.

The User's Manual and/or System O&M Manual provide power supply requirements specific to the system based on each system's System Design Description (SDD) and Equipment Design Specification (EDS) or Equipment Requirements Specification (ERS).

II-A-2.2 NRW-FPGA-Based System Configuration

The User's Manual and/or System O&M Manual provide system configuration information for each system, based on the set of SDD, IED, IBD, EDS, and ERS for each system.

II-A-2.3 NRW-FPGA-Based System Interfaces

The User's Manual and/or System O&M Manual provide the interface specification for each unit in the system and provide detailed information on the human-system interface (HSI). Each system has specific interface details based on the system EDS or ERS.

II-A-2.4 Failure Analysis

(1) A Failure Modes and Effects Analysis (FMEA) Report specific to each system is provided to the customer. The FMEA documents identify all failure modes that affect the safety-related functions. Through the analysis activities, all

identified failures are shown to be unlikely and detectable. This result conforms to the failure state and FMEA requirements shown in the EDS or ERS for each system.

The FMEA for the BWR-5 PRM system was conducted and documented in the Requirements Definition Phase Preliminary Hazard Analysis Report (Reference (d11)).

The FMEA for the ABWR OPRM was conducted and documented in the NICSD Software Safety Analysis Report for Safety-Related Oscillation Power Range Monitor (OPRM) (Design Phase) (Reference (c24)).

(2) An Availability and Reliability Analysis Report specific to each system is provided to the customer. This report is generated using MIL-HDBK-217F (Reference (a24)). The reliability values are calculated by summing the failure rates of each device.

The reliability and availability analysis for the BWR-5 PRM system configured with the LPRM, LPRM/APRM, and FLOW units was conducted and documented in the PRM Availability/Reliability Analysis Report (Reference (d30)).

The reliability and availability analysis for the ABWR OPRM was documented in the Availability/Reliability Analysis Report for Safety-Related Oscillation Power Range Monitor (OPRM) (Reference (c23)).

(3) Each NRW-FPGA-based system is designed and tested to minimize the possibility of programmable logic common cause failure (CCF). However, should a CCF occur, it would likely result in a complete loss of system function, incorrect indications, or incorrect outputs. Toshiba recommends that operational procedures include instructions for operator actions in the unlikely event of a CCF, including complete loss of system function, incorrect indications, or incorrect outputs.

II-A-2.5 Diversity and Defense-in-Depth

There is no attempt to design diversity or defense-in-depth into a NRW-FPGA-based system. Diversity and defense-in-depth analyses are a plant-specific evaluation of overall system

considerations and general characteristics of devices rather than the specifications of any individual device in the system. The qualification of NRW-FPGA-based systems provides assurance of a qualified device and logic.

II-A-2.6 Setpoint Support Analysis

Each Setpoint Support Analysis for the NRW-FPGA-based PRM and OPRM is performed to meet the requirements of EPRI TR-107330 (Reference (a46)), Section 4.2.4 and RG 1.105 (Reference (a10)).

For the PRM system, the data necessary to perform a setpoint analysis was provided in the system-specific Setpoint Support Analysis Report (Reference (d31)) which is provided to the customer.

For the OPRM, the data necessary to perform a setpoint analysis was provided in the Setpoint Support Analysis Report for Safety-Related Oscillation Power Range Monitor (OPRM) (Reference (c25)) which is provided to the customer.

II-A-2.7 Self-Diagnostic Capabilities

Each module of PRM and OPRM provides self-test and self-diagnostic capabilities. These capabilities are documented in the PRM FMEA Report and the OPRM FMEA Report. Each FMEA Report is based on the system's design documents, which document the self-diagnostic capability of modules making up the system as well as the overall system's self-check capabilities. Details of the indications for self-diagnostics are provided in the user's manuals.

Each module of PRM and OPRM includes operator-initiated surveillance test and calibration features. Failures detected by hardware and surveillance testing are consistent with the assumptions made concerning detection of failures in the single-failure analysis and the FMEA.

When the PRM or OPRM is operating, a module or unit will detect improper operation of any module in a few seconds, based on module continuous self-diagnostics.

Table II-A-2-1 summarizes self-diagnostics for communication errors, FPGA failures, and other hardware errors.

If only a single value is being communicated, data update checks using refresh counts and timeout checks are provided. For communication errors in multiplexed data frames, parity check and Cyclic Redundancy Checks (CRC) are provided in addition to timeout checks. See Section II-2.1.4 for further information.

For FPGA failures, watchdog timers are used. Section II-2.2.3.3 describes how the watchdog timers work to detect FPGA failures.

Each module using EEPROMs to store constants for the setpoint values, stores two copies of each value. In one copy, the value is stored in the original binary form. In the other copy, the data is stored in inverted form. The module verifies the stored values in the EEPROM by bitwise comparison of the two copies.

For EPROM, Toshiba uses One Type Programmable (OTP) EPROM, which has no window usually used for erasing its data by exposing the chip to ultraviolet (UV) light. Since UV light is shielded, the data in OTP EPROMs is reliable. Accordingly, Toshiba believes that no additional diagnostic measures are required for the OTP EPROM. However, the NICSD hazards analysis in the SSAR (Reference (c24)) reported a possibility that data corruption of EPROM may lead to a single spurious trip or loss of one division trip, when a single failure is assumed. Specifically, the EPROM stores the following values in the OPRM:

- Filter constant table for conditioning and time average filters, and
- Conversion table, which assigns LPRM detectors to each OPRM cell.

To address the concern from the hazards analysis, Toshiba will provide the following methods to check the EPROM data:

- For the conditioning and time average filters constants, enter test LPRM levels, which oscillate at specified frequencies and check whether the resulting Normalized Oscillation Signals match the expected signal values. If they match, the values in EPROM are not corrupted.

- For the conversion table, enter a unique value as each LPRM level, and check that the Normalized Oscillation Signal outputs match the expected values. If they match, the values in EPROM are not corrupted.

The Table II-A-2-2 lists the modules that contain EEPROM and/or EPROM.

The Low Voltage Power Supply (LVPS) diagnostic monitors the voltage of the LVPS output.

The Unit Type check and the ID check are performed by the RCV module that receives communication data from other units to check the unit configuration. The RCV module checks whether the unit type and identification data in the received data frame matches the expected and required unit type, which is hardwired into the unit's middle plane connector, and identification set by module's rotary switches. If an error is detected, a minor failure alarm or inoperable alarm signal is generated. Since the self-diagnostic features are integrated in the modules, the features meet all safety-related requirements.

If a failure is detected during a self-diagnostic, a fault indicator LED is lit on the front panel of the affected module and a dedicated dry contact fault indication signal changes state. Each unit provides a dry contact output, which the utility can wire into the annunciator system in the Main Control Room. Operator notification of detected failures complies with the system status indication requirements in IEEE Std 603-1991 (Reference (a36)). The utility can provide instructions in plant procedures to ensure consistency with, and support of, plant technical specifications, operating procedures, and maintenance procedures.

Table II-A-2-1 Summary of Self-Diagnostic

Failure Type	Failure	Detection	Compensatory Action Taken and Indication	Possible Resultant Effects
Communication Error	Errors of a single value, such as the LPRM levels	[redacted]		
	Errors of multiplexed data frames.			
FPGA Failure	One of the signal processing FPGAs halts			
	One of the human-machine interface FPGAs halts			
Other Hardware Error	EEPROM data error			
	LVPS failure			
	Unit Configuration Error			

* Fiber Optic Link only

Table II-A-2-2 Summary of Self-Diagnostic

Module	EEPROM	EPROM
LPRM module	X	Not used
APRM module	X	X
SQ-ROOT module	Not used	X
CELL module	X	X
AGRD module	X	Not used
PBD module	X	Not used

II-A-2.8 Surveillance Capabilities

This section discusses considerations for changes to existing plant surveillance test procedures, based on the design features incorporated in the PRM and OPRM (including the self-test features discussed above). These considerations are provided here to assist plants in identifying areas in which use of the PRM and OPRM will have a beneficial effect on the surveillance program.

Modifications to the existing surveillance tests and licensing commitments will be required, as is identified in USNRC Standard Review Plan, Chapter 7, Branch Technical Position (BTP) 7-17 (Reference (a6)). Self-tests capabilities in the new NRW-FPGA-based system should be used to reduce the surveillance testing requirements from those required with the existing systems. The self-test capabilities of the systems could be credited with some of the test functions for channels and devices currently provided by manual surveillance tests. The systems provide at least as much test coverage as the existing surveillance tests, through the fault tolerance and detection capabilities inherent in the system design.

(1) Because of design and architectural differences between analog and digital systems, traditional surveillance test provisions for analog systems may not be adequate or appropriate for digital systems. The required surveillance test capabilities to be included in this design will have to be evaluated to assure adequacy to fulfill the requirements and the intent of the surveillance tests. The replacement system design should provide the ability to conduct periodic testing consistent with the modified technical specifications and plant procedures.

(2) The PRM and OPRM were designed to provide surveillance test capabilities, in accordance with the requirements established in the regulatory guidance referenced in BTP 7-17.

There is nothing inherent in the NRW-FPGA-based system design that does not comply with the requirements of IEEE Std 603 (Reference (a36)), as required in BTP 7-17. The NRW-FPGA-based system design also complies with the recommendations made in IEEE Std 7-4.3.2 (Reference (a30)).

(3) Plant procedures should specify manual compensatory actions for recovery from PRM and OPRM equipment problems.

(4) Utility surveillance tests shall be designed to validate correct operation of each system and the system's self-tests, to the extent practical. For the BWR-5 PRM system, a method of failure detection for each of the failure modes listed in the appendix of the Requirements Definition Phase Preliminary Hazard Analysis Report (Reference (d11)) should be considered while developing the required content for surveillance testing. For the OPRM, a method of failure detection for each of the failure modes is listed in the NICSD Software Safety Analysis Report for Safety-Related Oscillation Power Range Monitor (OPRM) (Design Phase) (Reference (c24))

(5) Surveillance test frequency in a nuclear plant is based on the expected reliability of the installed system. The technology used in the PRM and OPRM should enhance the reliability and reduce the possibility of undetected in-service degradation. This should support longer surveillance test intervals. For the BWR-5 PRM and ABWR OPRM, Toshiba will work with the customer to determine an adequate surveillance testing frequency, based on the FMEAs and reliability evaluation for each failure mode that could not be found by self-diagnostic capabilities and that have significant effects on the plant.

II-A-3 System Configuration

This section describes the configuration of PRM and OPRM that have been qualified.

II-A-3.1 PRM System Configuration

The PRM Qualification Project used a test specimen composed of units like those that would be used in the PRM system for a BWR-5 design. The logic inside each FPGA was identical to what would be shipped to a BWR-5. The PRM system consists of LPRM units, APRM/LPRM units, FLOW units, and RBM units. Each unit is comprised of modules and a unit chassis specific to each unit's design. The non-safety-related RBM unit was not included in the PRM Qualification Project.

The Unit/Module configuration for the equipment qualification activities is shown in Table II-A-3-1.

Table II-A-3-1 Unit/Module Configuration Qualified in PRM Qualification Project

(Slot ID) Module Name	Module Model Number	Functional Description
LPRM Unit (HNU100B00000)		
(FSL01) LPRM Module	HNS013B00000	LPRM function for LPRM Detector CH 11
(FSL02) LPRM Module	HNS013B00000	LPRM function for LPRM Detector CH 12
(FSL03) LPRM Module	HNS013B00000	LPRM function for LPRM Detector CH 13
(FSL04) LPRM Module	HNS013B00000	LPRM function for LPRM Detector CH 14
(FSL05) LPRM Module	HNS013B00000	LPRM function for LPRM Detector CH 15
(FSL06) LPRM Module	HNS013B00000	LPRM function for LPRM Detector CH 16
(FSL07) LPRM Module	HNS013B00000	LPRM function for LPRM Detector CH 17
(FSL08) LPRM Module	HNS013B00000	LPRM function for LPRM Detector CH 18
(FSL09) LPRM Module	HNS013B00000	LPRM function for LPRM Detector CH 19
(FSL10) LPRM Module	HNS013B00000	LPRM function for LPRM Detector CH 20
(FSL11) LPRM Module	HNS013B00000	LPRM function for LPRM Detector CH 21
(FSL12) LPRM Module	HNS013B00000	LPRM function for LPRM Detector CH 22
(FSL13) BLANK Module	HNS490B00000	When the unit is not filled with 13 LPRM Modules, this dummy module is used to fill the open slots to provide necessary connections and signals simulating the LPRM Module operation in the open slots.
(FSL14) STATUS Module	HNS093B00000	Power supply voltage monitoring status indication
(PSSL01) LVPS Module	HNS500B00000	+5V and ±15V power supply to each module
(BSL01) AO Module	HNS518B00000	Analog output (AO) of LPRM levels (Ch. 11 to 22) to the process computer
(BSL02) Blank Panel	---	Blank panel

(Slot ID) Module Name	Module Model Number	Functional Description
(BSL03) AO Module	HNS515B00000	Analog output of LPRM levels (Ch. 11 to 22) to the Transient Monitor or OPRM
(BSL04) DIO Module	HNS520 B00000	Digital Input / Output (DIO) used for digital output of LPRM Upscale, Downscale, and Inoperable signals to the trip auxiliary unit
(BSL05) Blank Panel	---	Blank Panel
(BSL06) Blank Panel	---	Blank Panel
(BSL07) Blank Panel	---	Blank Panel
(BSL08) TRN Module	HNS530B00000	Optical data transmission (TRN) of LPRM level (Ch.11-22), Inoperable and LVPS failure information to LPRM/APRM unit
(PSSL02) LVPS Module	HNS500 B00000	+5V and ±15V power supply to each module
LPRM/APRM Unit (HNU200B00000)		
(FSL01) LPRM Module	HNS013B00000	LPRM function for LPRM Detector CH 1
(FSL02) LPRM Module	HNS013B00000	LPRM function for LPRM Detector CH 2
(FSL03) LPRM Module	HNS013B00000	LPRM function for LPRM Detector CH 3
(FSL04) LPRM Module	HNS013B00000	LPRM function for LPRM Detector CH 4
(FSL05) LPRM Module	HNS013B00000	LPRM function for LPRM Detector CH 5
(FSL06) LPRM Module	HNS013B00000	LPRM function for LPRM Detector CH 6
(FSL07) LPRM Module	HNS013B00000	LPRM function for LPRM Detector CH 7
(FSL08) LPRM Module	HNS013B00000	LPRM function for LPRM Detector CH 8
(FSL09) LPRM Module	HNS013B00000	LPRM function for LPRM Detector CH 9
(FSL10) LPRM Module	HNS013B00000	LPRM function for LPRM Detector CH 10
(FSL11) APRM Module	HNS020B00000	APRM function
(FSL13) Blank Panel	---	Blank Panel
(FSL14) STATUS Module	HNS091B00000	Data reception status, power supply voltage monitoring status indications
(PSSL01) LVPS Module	HNS500B00000	+5V and ±15V power supply to each module
(BSL01) AO Module	HNS518B00000	Analog outputs of LPRM levels (Ch. 1 to 10), APRM level, APRM Upscale (High) setpoint, Simulated Thermal Power level, and Simulated Thermal Power Upscale setpoint to the process computer
(BSL02) AO Module	HNS516B00000	Analog outputs of APRM level and APRM Upscale (High) setpoint to the recorder
(BSL03) AO Module	HNS515B00000	Analog outputs of LPRM levels (Ch. 1 to 10) and APRM level to the Transient Monitor or OPRM
(BSL04) DIO Module	HNS520B00000	Digital outputs of LPRM Upscale, Downscale, Inoperable, and APRM trip signals to the trip auxiliary unit Digital inputs of reactor mode and APRM bypass signal
(BSL05) RCV Module	HNS540B00000	Optical data reception of the recirculation flow values from the Flow units Optical data reception of LPRM levels (Ch. 11 to 22), Inoperable, and LVPS failure information from the LPRM unit
(BSL06) Blank Panel	---	Blank panel
(BSL07) Blank Panel	---	Blank panel
(BSL08) TRN Module	HNS530B00000	Optical data transmission of LPRM level (Ch. 1 to 22), APRM level, APRM Upscale (High) setpoint, Simulated Thermal Power level, Simulated Thermal Power Upscale setpoint, and Recirculation Flow values to RBM unit
(PSSL02) LVPS Module	HNS500B00000	+5V and ±15V power supply to each module

(Slot ID) Module Name	Module Model Number	Functional Description
FLOW Unit Configuration (HNU300B00000)		
(FSL01) Blank Panel	---	Blank Panel
(FSL02) Blank Panel	---	Blank Panel
(FSL03) Blank Panel	---	Blank Panel
(FSL04) Blank Panel	---	Blank Panel
(FSL05) Blank Panel	---	Blank Panel
(FSL06) Blank Panel	---	Blank Panel
(FSL07) Blank Panel	---	Blank Panel
(FSL08) Blank Panel	---	Blank Panel
(FSL09) Blank Panel	---	Blank Panel
(FSL10) SQ-ROOT Module	HNS030B00000	Square root arithmetic function for Recirculation Loop "a"
(FSL11) SQ-ROOT Module	HNS030B00000	Square root arithmetic function for Recirculation Loop "b"
(FSL12) FLOW Module	HNS040B00000	Recirculation-flow calculation, trip and alarm functions
(FSL14) STATUS Module	HNS093B00000	Flow unit status indication function
(PSSL01) LVPS Module	HNS500B00000	+5V and ±15V power supply to each module
(BSL01) AO Module	HNS518B00000	Analog outputs to the process computer
(BSL02) AO Module	HNS516B00000	Analog outputs to the recorders.
(BSL03) AO Module	HNS517B00000	Analog outputs to the Transient Monitor
(BSL04) DIO Module	HNS520B00000	Digital outputs of the trip signals to the trip auxiliary unit Digital input of Bypass signal
(BSL05) Blank Panel	---	Blank Panel
(BSL06) Blank Panel	---	Blank Panel
(BSL07) TRN Module	HNS530B00000	Optical serial transmission to RBM unit
(BSL08) TRN Module	HNS530B00000	Optical serial transmission to APRM unit
(PSSL02) LVPS Module	HNS500B00000	+5V and ±15V power supply each module

II-A-3.2 OPRM Configuration

Toshiba originally designed the OPRM for an ABWR. The OPRM test specimen that Toshiba used in the equipment qualification testing was configured for an ABWR. The OPRM Qualification used the test specimen composed of one OPRM unit with two Power Factor Correction modules (PFCs) as external modules for the OPRM unit. The logic inside each FPGA in the OPRM test specimen for the qualification testing was identical to what would be shipped to an ABWR, and the number of LPRMs would need to be adjusted in the logic for use in other BWR types. The OPRM unit consists of a unit chassis and 11 modules comprising eight different functional modules: two RCV, one CELL, one AGRD, one PBD, one DAT/ST, two TRN, one DIO, and two LVPS modules.

Each PFC receives AC voltage from an external AC power supply. Each PFC converts AC voltage into about 220 V DC. Each PFC supplies DC voltage to one of the two LVPS modules.

The test specimen configuration for equipment qualification testing is shown in Table II-A-3-2.

The PFC is included in the OPRM test specimen as shown in Table II-A-3-2 and qualified with the OPRM unit in the OPRM qualification testing.

Table II-A-3-2 Test Specimen Configuration during Equipment Qualification Testing of ABWR OPRM

(Slot ID) Module Name	Model Number	Functional Description
OPRM Unit (HNU12000B00000)		
(FSL01) Blank Panel	---	Blank Panel
(FSL02) Blank Panel	---	Blank Panel
(FSL03) Blank Panel	---	Blank Panel
(FSL04) Blank Panel	---	Blank Panel
(FSL05) to (FSL07) CELL Module	HNS0400B00000	LPRM Levels are converted to Normalized Oscillation Signal
(FSL08) to (FSL09) AGRD Module	HNS0420B00000	Amplitude-Based Detection Algorithm judgment is performed. Growth Rate-Based Detection Algorithm judgment is performed
(FSL10) to (FSL11) PBD Module	HNS0430B00000	Period-Based Detection Algorithm judgment is performed
(FSL12) Blank Panel	---	Blank Panel
(FSL13) Blank Panel	---	Blank Panel
(FSL14) DAT/ST Module	HNS0410B00000	Power status is indicated on the front panel Input status is indicated on the front panel Data are multiplexed.
(PSSL01) LVPS Module	HNS0500B00000	+5V and ±15V power supply to each module
(BSL01) Blank Panel	---	Blank Panel
(BSL02) Blank Panel	---	Blank Panel
(BSL03) Blank Panel	---	Blank Panel
(BSL04) DIO Module	HNS520B00000	Digital inputs are received from the Relay unit Digital outputs are provided to the Relay unit.
(BSL05) RCV Module	HNS0541B00000	Optical data reception of the LPRM unit data from LPRM unit
(BSL06) RCV Module	HNS0541B00000	Optical data reception of the APRM unit data from APRM unit
(BSL07) TRN Module	HNS0531B00000	Optical data transmission of OPRM unit data to the Engineered Safety Features and Plant Computer
(BSL08) TRN Module	HNS0531B00000	Optical data transmission of OPRM unit data to transient data recorder, sequence of events recorder, etc..
(PSSL02) LVPS Module	HNS500B00000	+5V and ±15V power supply to each module
Power Factor Correction module (PFC)		
(External) Power Factor Correction module (PFC)	BPC-10	Input line filter and power conversion from ac to dc, for one LVPS module

II-A-4 Environment and Location

This section provides the equipment qualification limits for the safety-related NRW-FPGA-based systems. These limits for temperature, humidity, radiation, seismic, and electromagnetic compatibility can be compared to plant conditions to determine plant location requirements. The limits are based on recommendations in the User's Manual, recommendations in the System O&M Manual, and the results of the equipment qualification testing.

All temperature, humidity, radiation, seismic, and EMC conditions were verified by type test or by analysis. Additional system-specific environment and location requirements derived from qualification testing are documented in this application guide.

II-A-4.1 Mounting

Each chassis shall be installed in a cabinet. The cabinet shall provide access for both the front and the rear of each chassis. The cabinet shall be provided with locking doors on the front and rear. The front door may be equipped with a window allowing visual access to the module fronts. Opening any door shall provide annunciation in the main control room. For cyber security purposes, provision shall be made for separate annunciation in one or more physical security locations.

A chassis acts as the enclosure for each unit. The chassis mounts in a standard 19" rack. The chassis hole spacing shall be compatible with the EIA standard. A chassis is fixed in the rack with four M5 screws tightened to 3.0 ± 0.4 N-m in the front and eight M4 screws tightened to 1.5 ± 0.2 N-m in the back.

During normal plant operation, no access is required to the modules mounted on the rear of the unit.

II-A-4.2 Temperature, Humidity and Radiation

The NRW-FPGA-based systems shall be located in an area that controls temperature, humidity, and radiation within the performance requirements defined by the environmental conditions shown in Table II-A-4-1. Toshiba performed type testing in a temperature and humidity test chamber in accordance with the methods defined in EPRI TR-107330 (Reference (a46)). Toshiba performed radiation exposure testing in accordance with the methods defined in EPRI TR-107330. Type testing was performed on individual units; the units were not mounted in

cabinets.

Table II-A-4-1 Environmental Conditions

	Normal Environmental Basic Requirements	Abnormal Environmental Basic Requirements
Temperature Range	16 to 40°C (60 to 104°F)	4 to 50°C (40 to 120 °F)
Humidity Range	40 to 95% (non-condensing)	10 to 95% (non-condensing)
Radiation Exposure	Up to 10 Gy (10^3 RADS) with 10% testing margin	Up to 10 Gy (10^3 RADS) with 10% testing margin

(1) Environmental Test Profiles for BWR-5 PRM System

The BWR-5 PRM system has been type tested to the temperature and humidity limits shown in Figure II-A-4-1 and Figure II-A-4-2. The testing complied closely, but not identically, to the test curves shown in Figure 4-4 of EPRI TR-107330, due to test equipment limitations.

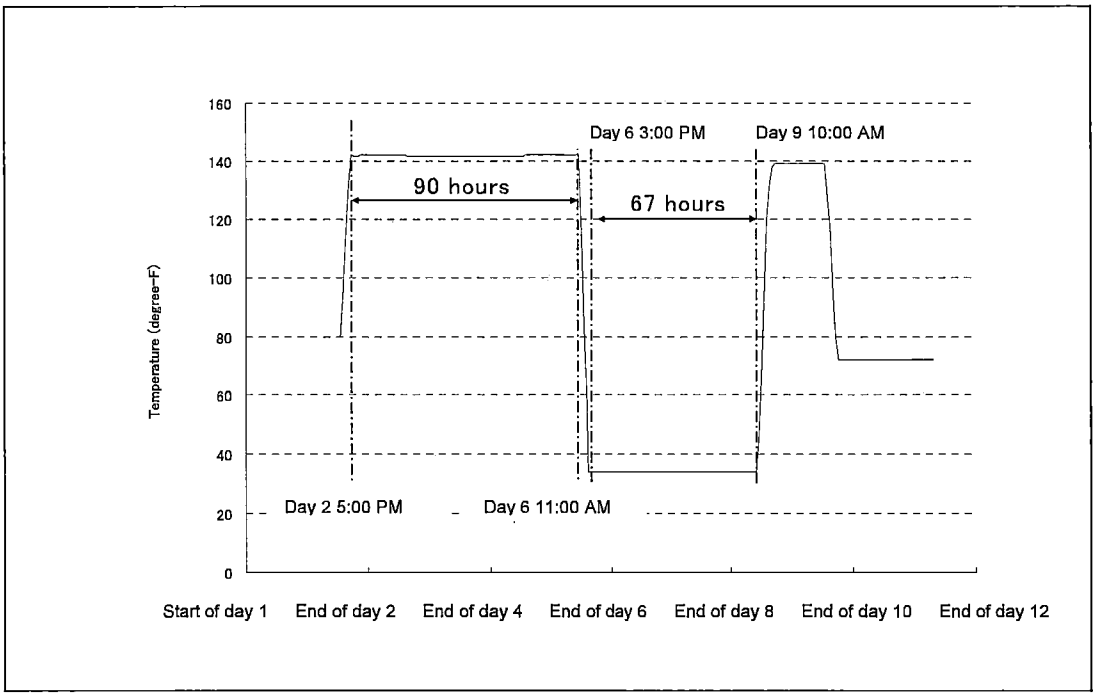


Figure II-A-4-1 Environmental Test Temperature Profile

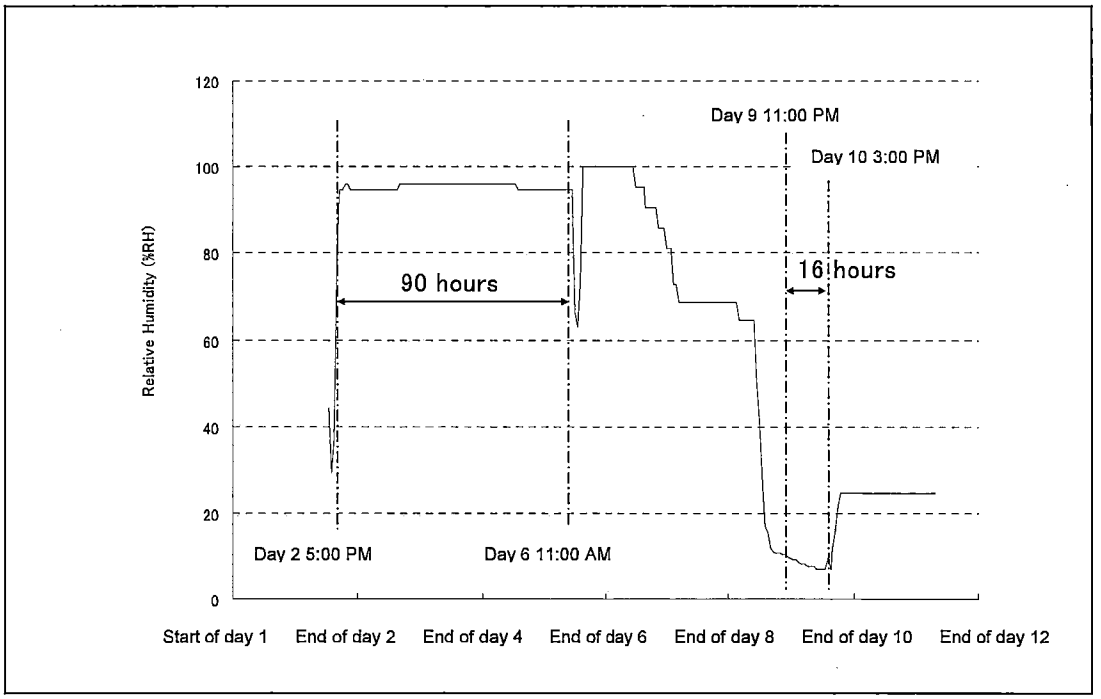


Figure II-A-4-2 Environmental Test Humidity Profile

The test facility could not achieve the low relative humidity at the low temperature condition required by EPRI TR-107330. Toshiba performed the low temperature test independently of the low humidity test. This is acceptable because EPRI TR-107330 states that if the specified relative humidity cannot be achieved for the specified temperature, then the test can be performed for the specified time at the lowest relative humidity that can be achieved at the specified temperature followed by performing the test at the lowest temperature where the specified relative humidity can be achieved.

Details of the tests results and test data from the PRM Environmental Test are reported in the PRM Qualification Test Summary Report (Reference (d16)). The test achieved the objective of exposing the tested equipment to a wide range of humidity conditions and verifying that the PRM operated correctly during the test. Review of the data collected during the test shows that the Test Specimen operated as intended.

At the end of the High Temperature and High Humidity Exposure, a Performance Proof Test was performed, and at the end of the environmental test an Operability Test was performed. These tests showed that all safety functions were confirmed to be within the required tolerance after subjecting the Test Specimen to temperature and humidity extremes. The evaluation concludes that this exposure will not prevent the PRM System from performing its safety-related function.

The type test performed during the PRM Qualification Project demonstrated that the PRM system survives and operates correctly throughout temperature and humidity testing.

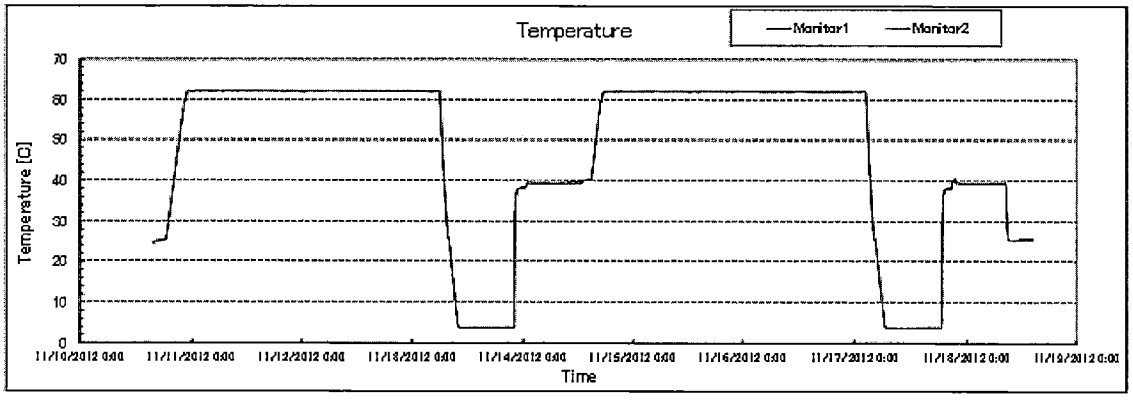
The PRM systems were qualified, based on EPRI TR-107330 Figure 4-4 and Section 4.3.6:

a. High Temperature and Humidity: 140 °F and 95% relative humidity, which meets EPRI TR-107330 Section 4.3.6 and Figure 4-4 requirements (Toshiba notes that adding 5% margin to the relative humidity would most likely induce condensation, which is not included in Toshiba's qualification envelope).

b. Low Temperature and Humidity: 35 °F and 10% relative humidity, which meets EPRI TR-107330 Section 4.3.6 requirements (Figure 4-4 requirements for humidity could not be met in this chamber, even with relaxation for non-simultaneous temperature and humidity, and Toshiba notes that the OPRM is constructed of similar components and had no issues at 40 °F and 5% relative humidity which could be achieved in the environmental test chamber used for testing the OPRM).

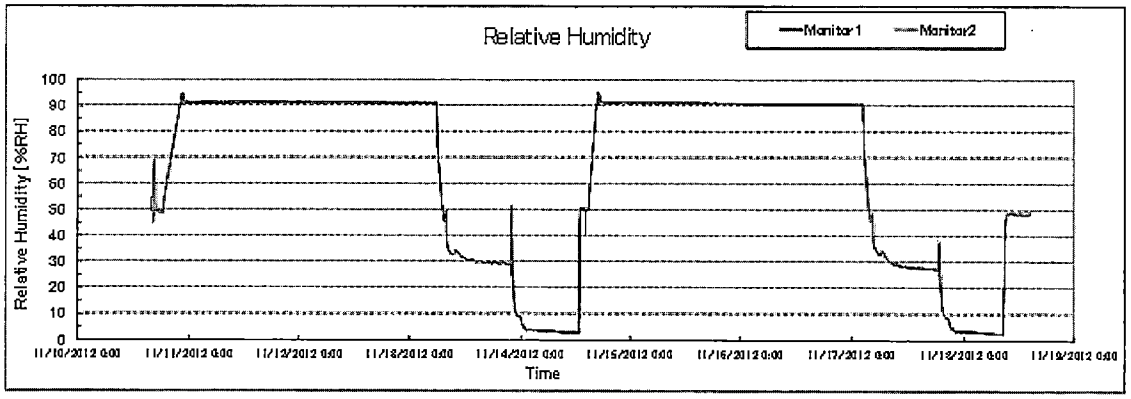
(2) Environmental Test Profiles for ABWR OPRM

The ABWR OPRM has been type tested to the temperature and humidity limits shown in Figure II-A-4-3 and Figure II-A-4-4. During the test, the temperature and humidity test conditions were successfully controlled as planned and there was no condensation in the test chamber during the test. The testing complied closely, but not identically, to the test curves in Figure 4-4 EPRI TR-107330, due to test equipment limitations.



Note: The monitor 1 is master and the monitor 2 is back up

Figure II-A-4-3 Environmental Test Temperature Profile (OPRM)



Note: The monitor 1 is master and the monitor 2 is back up

Figure II-A-4-4 Environmental Test Humidity Profile (OPRM)

Details of the tests results of the temperature and humidity test are reported in the OPRM Environmental Qualification Report (Reference (c20)).

The test results demonstrated that exposure to the temperature and humidity test conditions had no adverse effect on the OPRM performance.

The OPRM systems were qualified as follows, based on EPRI TR-107330 Figure 4-4 and Section 4.3.6:

OPRM:

a. High Temperature and Humidity: 140 °F and 90% relative humidity, which meets EPRI TR-107330 Figure 4-4 requirements (Section 4.3.6 requirements for humidity were met in separate testing at Toshiba, see Note below).

b. Low Temperature and Humidity: 40 °F and 5% relative humidity, which meets EPRI TR-107330 Section 4.3.6 and Figure 4-4 requirements.

Note: OPRM testing with 140 °F and 95% relative humidity profile was successfully met in the factory test which was performed under Toshiba's ISO 9001 program separately from the EQ test.

(3) Radiation Exposure for BWR-5 PRM System

The gamma irradiation on the Test Specimen was performed to 11 Gy to provide 10% margin above the requirement of 10 Gy per Section 4.3.6.1 of EPRI TR-107330 (Reference (a46)). The test was performed in accordance with the guidance provided on IEEE Std 323-1983 (Reference (a31)). The irradiation was performed at a high level radiation effects test facility. For this irradiation, a[ ]^{a,c}curie (Ci) Co-60 source was used.

Details of the tests results and test data of Environmental Test are reported in the Qualification Test Summary Report (Reference (d16)). During this test, the equipment was not powered and was not monitored. At the end of the test and before the environmental test, an Operability Test was performed. This test showed that all safety functions were confirmed to be within the required tolerance after subjecting the Test Specimen to the aging and integrated circuit damage from this exposure. The evaluation concludes that this exposure will not prevent the PRM System from performing its safety-related function.

(4) Radiation Exposure for ABWR OPRM System

Toshiba performed Radiation Testing of the BWR-5 PRM. Toshiba did not perform radiation testing for the ABWR OPRM, since the equipment is designed to be installed in a mild environment, and radiation exposure had already demonstrated that the components used were not susceptible to small doses.

(5) Heat Loads in Cabinets and Rooms

Heat Loads in the cabinets and the rooms are as follows.

(a) When mounting each NRW-FPGA-based system chassis into enclosures, heat management calculations shall be made to avoid exceeding the qualified ambient temperature ratings of each system. Required heat load data of PRM and OPRM components installed in the enclosures will be provided in plant application.

(b) If the room temperature plus any heat rise within the cabinet exceeds the limits supplied in Table II-A-4-1, additional provision must be made for temperature control to ensure that temperature remains within the qualified temperature condition.

(c) The system temperature range must be computed with cabinet doors open and with cabinet doors closed.

II-A-4.3 [Deleted]

II-A-4.4 Seismic Acceleration Limits

All safety-related NRW-FPGA-based systems shall be qualified as Category I seismic devices within the test levels shown on Figure II-A-4-5 and Table II-A-4-2. A plant-specific evaluation shall be needed to determine whether the as-tested limits bound the plant seismic acceleration requirements. If not, additional evaluation or seismic testing is required.

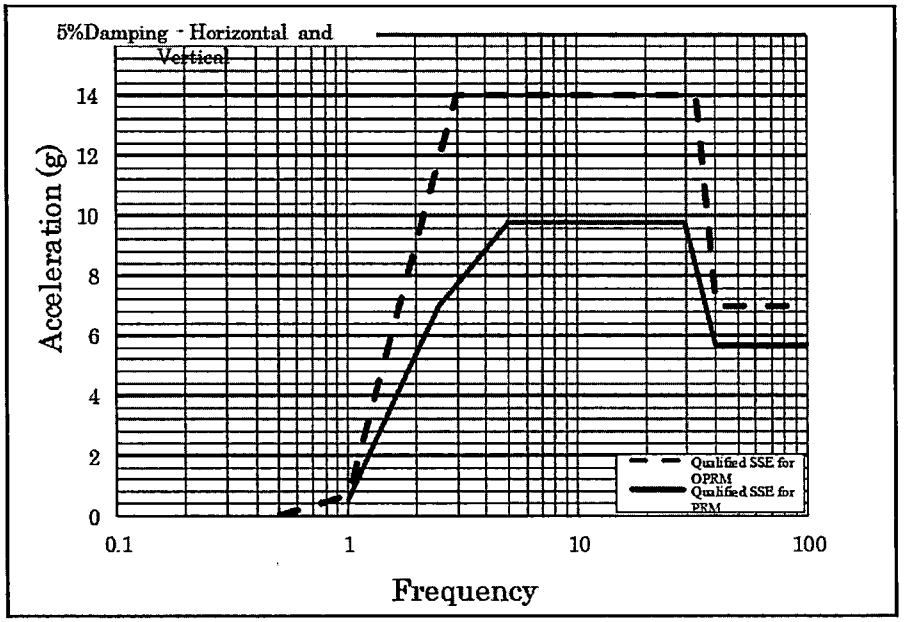


Figure II-A-4-5 Qualified Response Spectrum

Table II-A-4-2 Seismic Levels

Seismic Event	Maximum Acceleration Requirement	Reference Spectrum
OBE	9.8 g	EPRI TR-107330 Figure 4-5
SSE	14g (9.8 g was applied to type test for PRM Qualification Project due to the limitation of test facility)	EPRI TR-107330 Figure 4-5

II-A-4.4.1 Seismic Test of BWR-5 PRM

For the BWR-5 PRM System, the type test was performed during the PRM Qualification Project. The required peak amplitude of the SSE is 14g according to Figure 4-5 of EPRI-TR-107330. Due to the limitation of the test facility's vibration table, the peak amplitude of the SSE was 9.8 g. The following tests were performed.

(1) Resonance Search

A low-level (approximately 0.2g) single-axis sine sweep from 1 to 100 Hz at one octave/minute sweep rate was performed in each of the three orthogonal axes to determine major resonance of the Test Specimen Units. There was no major resonance below 100 Hz.

(2) Random Multi-Frequency Tests (5 OBEs and 1 SSE)

The Test Specimen was subjected to 30 second duration triaxial multi-frequency, random motion which was amplitude-controlled in one-sixth octave bandwidth spaced one-sixth octave apart over the frequency range of 1 to 100 Hz. The test response spectrum (TRS) obtained is shown in the Qualification Test Summary Report (Reference (d16)).

Figure II-A-4-6 is a representative figure showing the TRS for the first OBE for Horizontal Axis. The figure is based on a damping value of 5% used in the data analysis. See the Qualification Test Summary Report Appendix A for the remaining test figures.

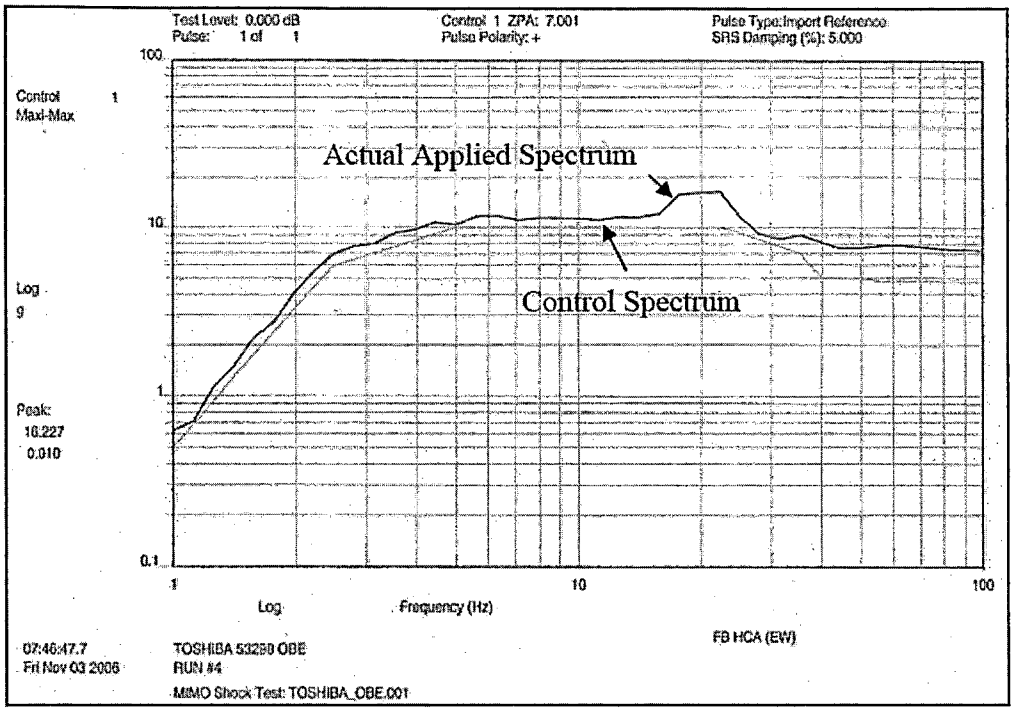


Figure II-A-4-6 TRS for 1st OBE for Horizontal Axis (East to West)

Details of the test results and test data of the Seismic Test are reported in the PRM Qualification Test Summary Report (Reference (d16)). Data collected during and after each OBE and SSE test demonstrate that the Test Specimen operated as intended throughout the testing. The Test Specimen was visually inspected for damage or degradation following each OBE and SSE test. Results of these inspections showed no physical damage or functional degradation of the Test Specimen.

The type test performed during the PRM Qualification Project demonstrated that the PRM system survives and operates correctly during and after seismic event up to the tested accelerations. The test specimen maintained structural integrity, and the test system did not detect any errors during and after the OBE and SSE tests.

II-A-4.4.2 Seismic Test of ABWR OPRM

For the ABWR OPRM, the following tests were performed as type testing.

(1) Resonance Search

The resonance search was conducted in each of the three principal orthogonal directions (front-to-back (Y), side-to-side (X), and vertical (Z)) with a 0.2g input peak sinusoidal acceleration from 1 to 100 Hz at one octave/minute sweep rate. Following the 1 to 100 Hz sweep, a 100 to 1 Hz sweep was also conducted for each principal direction.

(2) Random Multi-Frequency Tests (5 OBEs and 1 SSE)

The seismic test was performed on the triaxial vibration table, using random, multi-frequency acceleration time-history inputs to the vibration table at the seismic test area in the test facility in US. The vibration table drive signal was a multi-frequency, random input and was at least 30 seconds in duration with a minimum of 20 seconds of strong motion. The test response spectrum (TRS) obtained is shown in the Dynamic Qualification Report (Reference (c22)).

Figure II-A-4-7 is a representative figure showing the TRS for the first OBE for Horizontal Axis (Front to Back) at 5% critical damping. See the OPRM Dynamic Qualification Report Appendix C for the remaining TRSs.

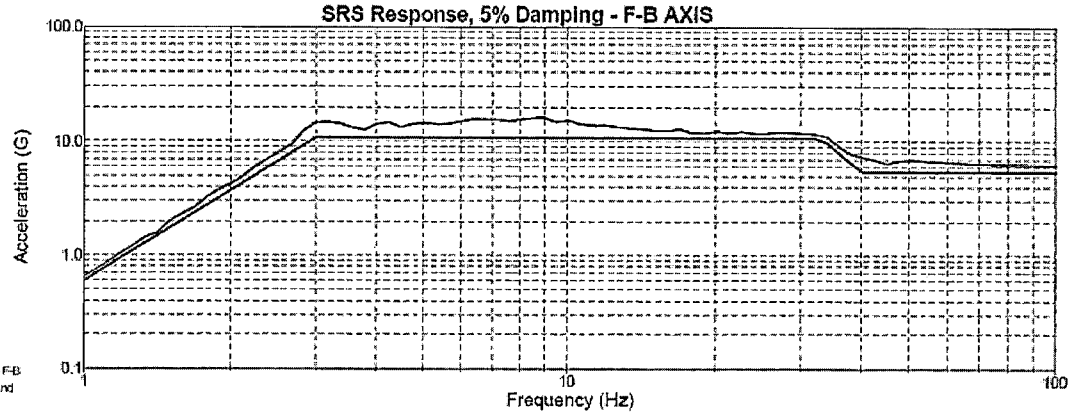


Figure II-A-4-7 TRS for 1st OBE for Horizontal Axis (Front to Back)

Details of the tests results of the Seismic tests are reported in the Dynamic Qualification

Report (Reference (c22)).

The resonance search results stated above demonstrate that the fixture was appropriately designed and fabricated for testing, the mounting of the test specimen was successful, and the test specimen had no major resonances from 1 to 100 Hz.

The test specimen maintained structural integrity, all the OPRM safety-related functions correctly operated, and no error was detected by the test system during and after the OBE and SSE tests.

II-A-4.5 Electro-Magnetic Compatibility (EMC)

An understanding of the electromagnetic susceptibility of a device is necessary to ensure that its operation will not be adversely affected by EMI/RFI or surge levels already present or permitted in the area where the device will be located. An understanding of the electromagnetic emissions of a device is necessary to ensure that operation of the device being tested would not result in adverse effects on other systems installed electrically close to the device being tested. Toshiba performs type testing of systems prior to making them available for installation in plants. The EMC environmental requirements documented in this section are based on the results of the equipment qualification type tests for the PRM and OPRM. The utility must evaluate the environmental data to ensure that the qualification envelope is sufficient for the planned location. This may require the utility to perform one or more of the following:

(1) Conduct an EMI/RFI survey to evaluate the EMI/RFI levels to ensure that the environment is within the assumptions of USNRC Regulatory Guide 1.180, Revision 1 (Reference (a19)).

(2) Recommend actions to mitigate unacceptable EMI/RFI sources. Toshiba does not perform qualification testing using a secondary enclosure, additional cable and wire shielding, or power line filtering beyond the devices installed during type testing. Mitigating actions to address system susceptibility levels would likely incorporate these common in-plant installation features. Mitigating actions might also include administrative controls on the EMI/RFI sources.

(3) Require additional qualification testing to address those cases where the recorded EMI/RFI test data provides inconclusive evidence of the susceptibility of particular modules, and therefore the modules are assumed to be susceptible. Additional testing may demonstrate that some modules are not actually susceptible to the applied EMI/RFI test levels.

The test methods for EMC qualification testing are summarized in Table II-A-4-3 and Table II-A-4-4. Test types listed in the tables comply with USNRC Regulatory Guide 1.180, Revision 1. The test methodologies were established to meet the requirements in each military or International Electrotechnical Commission (IEC) standard listed in the table.

Table II-A-4-5 shows the results of EMC tests for BWR-5 PRM; Table II-A-4-8 shows the result of EMC tests for ABWR OPRM.

Table II-A-4-3 EMI/RFI Test Method

Test Type	MIL-STD-461E Test Method
(a) Low-Frequency Conducted Susceptibility (Power):	CS101
(b) High-Frequency Conducted Susceptibility (Power):	CS114
(c) High-Frequency Conducted Susceptibility (Signal):	CS114
	CS115
	CS116
(d) Radiated Susceptibility, Magnetic Field:	RS101
(e) Radiated Susceptibility, Electric Field:	RS103
(f) Low-Frequency Conducted Emissions:	CE101
(g) High-Frequency Conducted Emissions:	CE102
(h) Radiated Emissions, Magnetic Field:	RE101
(i) Radiated Emissions, Magnetic Field:	RE102

Table II-A-4-4 Surge, EFT/B Test Method

Test Type	Applicable IEC Standard
(a) Ring Wave Surge (±2 kV) (Power)	IEC 61000-4-12
(b) Combination Wave (±2 kV) (Power)	IEC 61000-4-5
(c) EFT/B (±2 kV) (Power)	IEC 61000-4-4

Table II-A-4-5 EMC Test Results (BWR-5 PRM)

Test Item	Test Method	Test Level	Test Results
Conducted Emissions Low Frequency	MIL-STD-461E/CE101	60 Hz to 10 kHz	Comply with limited scope and/or condition (For CE101 test, choke coil should be added for mitigation.)
Conducted Emissions High Frequency	MIL-STD-461E/CE102	10 kHz to 2 MHz	Comply
Radiated Emissions Magnetic Field	MIL-STD-461E/RE101	30 Hz to 100 kHz	Comply
Radiated Emissions Electric Field	MIL-STD-461E/RE102	2 MHz to 1 GHz	Comply
Conducted Susceptibility Low Frequency	MIL-STD-461E/CS101	120 Hz to 150 kHz	Comply
Conducted Susceptibility High Frequency	MIL-STD-461E/CS114	10 kHz to 30 MHz	Comply
Conducted Susceptibility Bulk Cable Injection	MIL-STD-461E/CS115	2A	Comply
Conducted Susceptibility Damped Sinusoidal Transients	MIL-STD-461E/CS116	10 kHz to 100 MHz	Comply
Radiated Susceptibility Magnetic Field	MIL-STD-461E/RS101	30 Hz to 100 kHz	Comply
Radiated Susceptibility Electric Field	MIL-STD-461E/RS103	30 MHz to 1 GHz	Comply (Note 1)
Surge 100 kHz Ring Wave	IEC 61000-4-12/Ring Wave	2 kV	Comply
Surge Combination Wave	IEC 61000-4-5/Combination Wave	2 kV	Comply (Note 2)
Electrical Fast Transient /Burst	IEC 61000-4-4/EFT/B	2 kV	Comply
Electrostatic Discharge	IEC 61000-4-2/ESD	15 kV (Air Discharge) 8 kV (Contact Discharge)	Comply (Note 3)
Class 1E to Non-1E Isolation	---	600VAC 250VDC	Comply

Note 1: Toshiba did not test for radiated susceptibility (RS103) above 1 GHz for the PRM, and thus accepts that either a utility employing this equipment must preclude the use of cell phones and radios near this equipment or accept an open issue from the USNRC in the SER requiring an evaluation by the utility.
Note 2: The application of one repetition each second is described in IEC 61000-4-12. However, the Test Lab's equipment could not operate this rapidly. This is only an issue in the application period and has no adverse effect on the equipment qualification envelope. Toshiba and the Test Lab cannot find the record of the coupling impedance value used 12 Ω or 30 Ω for the ring wave test.
Note 3: Some test points in the back panel of the Test Specimen Units showed susceptibilities but recovered without degradation. These results complied with the requirement of the ESD Test. The Application Guide is updated with the requirement that all contact with the back panel requires use of grounded ESD wrist straps.

Table II-A-4-6 [Deleted]

Table II-A-4-7 [Deleted]

Table II-A-4-8 EMC Test Results (ABWR OPRM)

Test Item	Test Method	Test Level	Test Results
Conducted Emissions Low Frequency	MIL-STD-461E/CE101	60 Hz to 10 kHz	Comply
Conducted Emissions High Frequency	MIL-STD-461E/CE102	10 kHz to 2 MHz	Comply
Radiated Emissions Magnetic Field	MIL-STD-461E/RE101	30 Hz to 100 kHz	Comply
Radiated Emissions Electric Field	MIL-STD-461E/RE102	2 MHz to 10 GHz	Comply
Conducted Susceptibility Low Frequency	MIL-STD-461E/CS101	120 Hz to 150 kHz	Comply
Conducted Susceptibility High Frequency	MIL-STD-461E/CS114	10 kHz to 30 MHz	Comply
Conducted Susceptibility Bulk Cable Injection	MIL-STD-461E/CS115	2A	Comply
Conducted Susceptibility Damped Sinusoidal Transients	MIL-STD-461E/CS116	10 kHz to 100 MHz	Comply
Radiated Susceptibility Magnetic Field	MIL-STD-461E/RS101	30 Hz to 100 kHz	Comply
Radiated Susceptibility Electric Field	MIL-STD-461E/RS103	30 MHz to 10 GHz	Comply
Surge 100 kHz Ring Wave	IEC 61000-4-12/Ring Wave	2 kV	Comply
Surge Combination Wave	IEC 61000-4-5/Combination Wave	2 kV	Comply
Electrical Fast Transient /Burst	IEC 61000-4-4/EFT/B	2 kV	Comply
Electrostatic Discharge	IEC 61000-4-2/ESD	15 kV (Air Discharge) 8 kV (Contact Discharge)	Comply

II-A-4.5.1 EMI/RFI Test for BWR-5 PRM System

Toshiba type tested the BWR-5 PRM System. Details of the EMI/RFI test results and test data are reported in the PRM Qualification Test Summary Report (Reference (d16)). Susceptibility test results show that the Test Specimen continued to function correctly throughout all test exposure levels. The transfer of input and output data was not interrupted. There were no interruptions or inconsistencies in the operation of the system.

For the emissions tests, the Test Specimen was found to comply with the allowable equipment emissions levels for radiated magnetic field emissions from 30 Hz to 100 kHz (RE101). A specific exceedance was found during the first CE101 tests for the power leads. From approximately 100 Hz to 700 Hz, emissions exceed the limit shown in Regulatory Guide 1.180 Revision 1. This excess comes from the waveform distortion due to the AC/DC power supply (i.e. LVPS module) in the PRM system. To suppress this emission, Toshiba inserted a filter into the AC power line to the LVPS module, and confirmed that the test results satisfy the requirement with this corrective measure as shown in Table II-A-4-5. Systems supplied for use in the US would either use this power line filter or the PFC module used for the OPRM type testing. Either approach would successfully mitigate the LVPS emissions peaks.

II-A-4.5.2 Surge Withstand Capability (SWC) Test for BWR-5 PRM System

For the BWR-5 PRM System, the SWC Test was performed to ensure that the PRM System withstands the surge limits given in Table 22 of Regulatory Guide 1.180. Surges were applied in accordance with IEC 61000-4-12 (for Ring Wave) (Reference (a29)) and IEC 61000-4-5 (for Combination Wave) (Reference (a28)). Details of the SWC test results and test data are reported in the PRM Qualification Test Summary Report (Reference (d16)). The surges were applied to the test points, and the Test Specimen operated normally during the surge application. Based on the results reported in the PRM Qualification Test Summary Report, the Test Specimen continued to operate in accordance with the test acceptance criteria following application of the surge test voltages. The repetition rate for the ring wave was 12 per minute. The application of one repetition each second is described in IEC 61000-4-12. However, the Test Lab's equipment could not operate this rapidly. This is only an issue in the application period, and has no adverse effects on the equipment qualification envelope.

II-A-4.5.3 EFT/B Test for BWR-5 PRM System

For the BWR-5 PRM System, Toshiba performed EFT/B Testing to ensure that the PRM Test

Specimen withstands the EFT/B waveforms given in Table 22 of Regulatory Guide 1.180 and IEC 61000-4-4 (Reference (a27)). Details of the EFT/B test results and test data are reported in the PRM Qualification Test Summary Report (Reference (d16)). The EFT/B waveforms were applied to the defined test points. Results of the EFT/B testing show that the Test Specimen continued to operate in accordance with the test acceptance criteria.

II-A-4.5.4 ESD Test for BWR-5 PRM System

For the BWR-5 PRM System, the ESD Test was performed to assure that the Test Specimen withstands the ESD levels given in Section 4.3.8 of EPRI TR-107330 (Reference (a46)) and IEC 61000-4-2 (Reference (a26)). Details of the test results and test data for the ESD test are reported in the Qualification Test Summary Report (Reference (d16)).

Results of the ESD test show temporary degradation/loss of function occurred when ESD was applied to back panels. System functionality is recoverable. These back panels in the units are kept in cabinets and are not generally exposed to ESD during normal operation. For this PRM system, risk of ESD can be mitigated by minimizing access to the back panel during plant operation and by requiring personnel to wear anti-ESD wristbands when accessing the equipment back panel during plant operation. The back panels in the units are accessible only when locked cabinet doors are opened. In normal use at a US plant, the cabinet doors are unlocked and opened only when work is to be done on the panels, such as maintenance or calibration, which is done with the unit bypassed. The equipment behind the plane of the door on the back panels should not be touched unless the technician or engineer is wearing a grounded ESD wriststrap.

II-A-4.5.5 EMI/RFI Test for ABWR OPRM

Toshiba conducted EMI/RFI testing as a type test for the ABWR OPRM. Details of the test results of EMI/RFI testing are reported in the OPRM EMC Qualification Report (Reference (c21)).

The EMI/RFI emission test results show that the conducted and electromagnetic emissions from the test specimen satisfied the limit level specified in Regulatory Position 3 of Regulatory Guide 1.180, Revision 1 (Reference (a19)).

The EMI/RFI susceptibility test results show that the test specimen did not exhibit any malfunction, degradation of performance, or deviation from the specified limits when subjected to an immunity test signal specified in Regulatory Position 4 of Regulatory Guide 1.180, Revision 1.

II-A-4.5.6 Surge Withstand Test for ABWR OPRM

For the ABWR OPRM, the Surge Withstand Test was performed to ensure that the OPRM System withstands the surge limits given in Table 22 of Regulatory Guide 1.180 Revision 1. Surges were applied in accordance with IEC 61000-4-12 (Reference (a29)) (for Ring Wave) and IEC 61000-4-5 (Reference (a28)) (for Combination Wave). Details of the test results are reported in the OPRM EMC Qualification Report (Reference (c21)).

The surge withstand test results show that the test specimen did not exhibit any malfunction, degradation of performance, or deviation from the specified limits, when subjected to an immunity test signal in Regulatory Position 5 of Regulatory Guide 1.180, Revision 1.

II-A-4.5.7 EFT/B Test for ABWR OPRM

The EFT/B Test was performed to assure that the OPRM Test Specimen withstands the EFT/B waveforms given in Table 22 of Regulatory Guide 1.180 Revision 1. EFT/B waveforms were applied in accordance with IEC 61000-4-4 (Reference (a27)). Details of the test results are reported in the OPRM EMC Qualification Report (Reference (c21)).

The EFT/B test results show that the test specimen did not exhibit any malfunction, degradation of performance, or deviation from the specified limits, when subjected to the immunity test signal defined in Regulatory Position 5 of Regulatory Guide 1.180, Revision 1.

II-A-4.5.8 ESD Test for ABWR OPRM

The ESD Test was performed to assure that the Test Specimen withstands the ESD levels given in Section 4.3.8 of EPRI TR-107330 (Reference (a46)). ESD events were applied in accordance with IEC 61000-4-2 (Reference (a26)). Details of the test results are reported in the EMC Qualification Report (Reference (c21)).

Results of the ESD testing of OPRM show that the Test Specimen did not present any temporary degradation or loss of function or performance when the ESD was applied to all accessible points during normal operation. Thus, the test specimen was demonstrated the ESD withstand capability required in Section 4.3.8 of EPRI TR-107730 (Reference (a46)).

II-A-4.6 Class 1E to Non-Class 1E Isolation

Isolation features of the NRW-FPGA-based system conform to IEEE Std 384-1992 (Reference (a34)).

- Each isolation device prevents shorts, grounds, and open circuits on the Non-Class 1E side from unacceptably degrading the operation of the circuits on the Class 1E side.
- Each isolation device prevents application of the maximum credible voltage on the Non-Class 1E side from unacceptably degrading the operation of the Class 1E circuits.

For the BWR-5 PRM system, the communication data link provided in each PRM system has a one-way fiber optic communication link, providing fixed data sets from each safety-related PRM division individually to the non-safety-related Rod Block Monitor (RBM), providing Class 1E to non-Class 1E isolation, and offering no possibility of data transfer from the non-safety related to the safety related equipment. This design eliminates any potential for data from one division being supplied to another division. Based on this system design, only the devices installed in the main chassis are required to provide Class 1E to non-Class 1E electrical isolation capability (if these modules are used to interface to non-Class 1E equipment). Accordingly, the following devices that are used to provide analog output signals to non-Class 1E portion were tested for Class 1E isolation capability:

- HNS518 and HNS515 AO modules installed in LPRM Units
- HNS518, HNS516, and HNS515 AO modules installed in LPRM/APRM Units
- HNS518, HNS517, and HNS516 AO modules installed in Flow Unit

For the BWR-5 PRM System, the type test was performed. Details of the test results and test data of the Class 1E to Non-Class 1E test are reported in the Qualification Test Summary Report (Reference (d16)). Test level voltages were applied to the test points and the safety-related portion of the Test Specimen operated normally during and after the application. As expected, damage occurred to the non-Class 1E AO module, which did not propagate to the Class 1E equipment.

When the DIO module in the PRM or OPRM interfaces with non-safety equipment, qualified electrical isolation devices (such as relays) outside the unit are required.

II-A-4.7 Electrostatic Discharge (ESD)

ESD features of NRW-FPGA-based systems conform to IEC 61000-4-2 (Reference (a26)). The ESD levels comply with the levels of EPRI TR-107330 and EPRI TR-102323 ($\pm$8 kV for contact discharge and $\pm$15 kV for air discharge).

This testing was performed with modules grounded to the unit and units grounded to the chassis,

which reduces the potential for ESD damage in properly designed equipment. To reduce the possibility of undetected ESD damage resulting in shortened equipment life or decreased reliability, Toshiba requires use an anti-ESD wristband when maintenance is performed on any equipment. Toshiba also requires all modules and power supplies to be handled using ESD protection, including ESD pads and ESD packing materials.

Toshiba included ESD testing in the BWR-5 PRM System equipment qualification testing. Details of the test results and test data for the ESD test are reported in the PRM Qualification Test Summary Report (Reference (d16)). The ESD testing demonstrates that the Test Specimen did not present any temporary degradation or loss of function or performance when the ESD was applied to the front panels, components on the front panels, and side panels, which can all be touched during normal operation. However, testing showed temporary degradation/loss of function when ESD was applied to back panels. System functionality was recoverable. These panels are not generally exposed to ESD during normal operation. For the PRM System, ESD can be mitigated by preventing access to the back panel during plant operation, or by requiring personnel to wear anti-ESD wristbands when accessing the equipment back panel during plant operation. Therefore, plant administrative controls (e.g., procedures requiring use of static discharge control devices such as grounding straps) will be required to prevent or reduce exposure to electrostatic discharges.

During normal plant operation, administrative procedures should restrict maintenance access to the rear of the rack in which the PRM system units are installed.

Toshiba included ESD testing in the ABWR OPRM equipment qualification testing. Details of the test results are reported in the OPRM EMC Qualification Report (Reference (c21)). Results of the OPRM ESD testing demonstrate that the Test Specimen did not present any temporary degradation or loss of function or performance when the ESD was applied to accessible locations during normal operation. Thus, the test specimen demonstrated the ESD withstand capability required in Section 4.3.8 of EPRI TR-107730 (Reference (a46)).

II-A-5 Plant Interface

II-A-5.1 Response Time

The PRM and OPRM are validated during System Validation Tests to assure meeting the response time requirements described in the EDS or ERS for each system. The data for the EDS or ERS is based on the standard BWR requirements for trip or action times.

For the BWR-5 PRM, response time testing was performed as reported in the Part V of this LTR. The test results confirmed that the response times of the APRM Upscale (High-High) and the Simulated Thermal Power Upscale trips were less than the required 40 ms.

For the ABWR OPRM, response time testing was performed as reported in the Part VI of this LTR. The test confirmed that the OPRM system generates a trip when a normalized oscillation signal is introduced to the system within required [ ]^{a,c} ms.

II-A-5.2 Loss of Power Fault Indication

The NRW-FPGA-based units generate an inoperable signal from the DIO module when power loss occurs, which is treated as an inoperable channel and, therefore, initiates a single-channel vote to the trip signal. This capability is validated during the System Validation Tests.

For the BWR-5 PRM, loss of power testing was performed as reported in the Verification and Validation Final Report (included in the Part V of this LTR). The loss of power testing demonstrated that the PRM system generates an inoperable signal from the DIO module when power loss occurs.

For the ABWR OPRM, loss of power testing was performed in the system validation test in the same manner as the BWR-5 PRM. As reported in the Part VI of this LTR, the system validation test result was satisfactory, in that the OPRM generates an inoperable signal from the DIO module when power loss occurs.

II-A-6 Installation, Commissioning, and Maintenance

This section discusses considerations for installation, commissioning, and long term maintenance of the safety-related NRW-FPGA-based systems.

II-A-6.1 Required Testing

After a safety system is commissioned, no changes to the system can be performed without Toshiba redesigning the affected portions of the system and Toshiba and the utility re-commissioning the system.

The utility shall perform periodic testing to the requirements established by Toshiba in the User's Manual and/or System O&M Manual. Credit for self-tests can be used to reduce the requirement for surveillance testing, based on utility changes to the unit's Technical Specifications.

II-A-6.2 Operations Procedures

Operating procedures for the safety system being replaced will have to be modified to accommodate the NRW-FPGA-based systems. Procedures for any new fault alarms will have to be created. Procedures for entry and performance of maintenance and surveillance testing procedures will have to be modified to account for the differences between analog systems and the NRW-FPGA-based systems.

II-A-6.3 Maintenance Procedures

Specific maintenance considerations for the NRW-FPGA-based systems include the following:

- The User's Manual and/or System O&M Manual contain recommendations for maintenance.
- The utility should revise their maintenance procedures in accordance with the guidance from Toshiba User's Manual and/or the System O&M Manual.
- For the BWR PRM and ABWR OPRM, an adequate surveillance testing frequency will be determined, based on the FMEAs and reliability evaluation for each failure modes that could not be found by self-diagnostic capabilities and that have significant effects on the plant.

II-A-6.4 Maintenance and Bypass Capabilities

Existing safety-related systems in nuclear power plants typically include bypass capabilities for maintenance and testing. Implementation of these capabilities in a digital system requires particular attention to prevent undesired bypass of the system or incomplete bypass when a bypass is intended. Generic guidance on the implementation of bypass capabilities is provided in Toshiba's User's Manual and/or the System O&M Manual.

The PRM provides bypass features that allow the operator to bypass any one of the APRM channels for one RPS division during normal plant operation. The APRM channel bypass status is displayed on the PRM front panel and provided to the main control room.

The OPRM is bypassed automatically when either or both of the following conditions occur:

- When the APRM Level is less than the OPRM Region APRM Level Setpoint
- When the Core Flow Level is more than the OPRM Region Core Flow Level Setpoint

Bypassing a division of APRM bypasses the same division of OPRM.

II-A-7 PRM System Configuration for BWRs (BWR-3, BWR-4, BWR-5, BWR-6)

The number of units required for a specific BWR varies based on the size of the core and the number of LPRMs installed to monitor the core. This section provides a comparison between the PRM and/or PRNM system that would be used for the various types of BWRs designs.

This guidance provides a method to apply the modules and units qualified for BWR-5 PRM system and a method to modify and customize the neutron monitoring system for other BWR types.

Since the configurations of the BWR-3, BWR-4, and BWR-6 PRM are bounded by the BWR-5 PRM, no additional type testing will be performed. The ABWR PRNM system has a sufficiently different configuration from the BWR PRM systems to require complete type testing.

Specifically, the table below shows the number of units for the typical BWR-5 PRM system. The table also shows the equivalent information for other BWR types, namely, BWR-3, BWR-4, and BWR-6 designs.

Table II-A-7-1 provides typical system configurations for BWR-5, BWR-3, BWR-4, and BWR-6 designs.

The PRM systems provide the LPRM power signals to the OPRM system through analog outputs or fiber optic communication links. The analog signals are identical to the signals that are provided to the existing OPRM and the transient monitor. Replacement of the LPRM, APRM, and OPRM together is best performed using fiber optic communication and modules that have already been type tested. When the fiber optic communication is applied, a TRN module, which provides the LPRM level data using the same data provided to RBM, is added to the LPRM unit and LPRM/APRM unit, as defined in Section II-A-3.1.

Table II-A-7-1 PRM Configuration of BWR-3, BWR-4, BWR-5 and BWR-6

BWR	Number of LPRM Units	Number of LPRM/APRM Units	Number of FLOW Units	Number of OPRM Units
BWR-3 with 88 LPRM signals	4	6	2	4
BWR-4 with 124 LPRM signals	10	6	2	4
BWR-5 with 172 LPRM signals	10	6	4	4
BWR-6 with 132 LPRM signals	8	8	4	4

The following sections describe the individual PRM systems.

II-A-7.1 System Configuration for BWR-5 with 172 LPRM Signals

Figure II-A-7-1 shows a typical PRM system configuration for BWR-5 with 172 LPRM signals. Table II-A-7-2 lists the modules for this configuration.

The PRM system for a BWR-5 design consists of six APRM channels, two LPRM channels, and four Recirculation Flow Measurement (FLOW) channels. The LPRM detector sensors are divided into six APRM channels and two LPRM channels. APRM channels, LPRM channels, and FLOW channels are divided into two groups. Each group consists of three APRM channels, one LPRM channel, and two FLOW channels. Each APRM channel contains one LPRM unit and one LPRM/APRM unit. Each LPRM channel contains two LPRM units. Each FLOW channel contains one FLOW unit. Trip auxiliary units, which have no FPGAs, are used for relaying trip signals to other systems. Therefore, FPGA-based safety-related equipment in a typical BWR-5 with 172 LPRM detectors consists of ten LPRM units, six LPRM/APRM units, and four FLOW units. The PRM System provides the LPRM levels to the OPRM system using fiber optic serial communication links as shown in Section II-A-7.7.

When the PRM system is applied to a BWR-5, the LPRM channels (A) and (B) both transmit LPRM data to the Rod Block Monitor (RBM). Since the LPRM unit described in Section II-A-3 has no function to collect LPRM data from another LPRM unit, the MUX module needs to be applied to provide the required data transmission. The MUX module was not part of the BWR-5 PRM qualification. The MUX modules will be subjected to appropriate equipment qualification before being used (see also Section II-2.2.4).

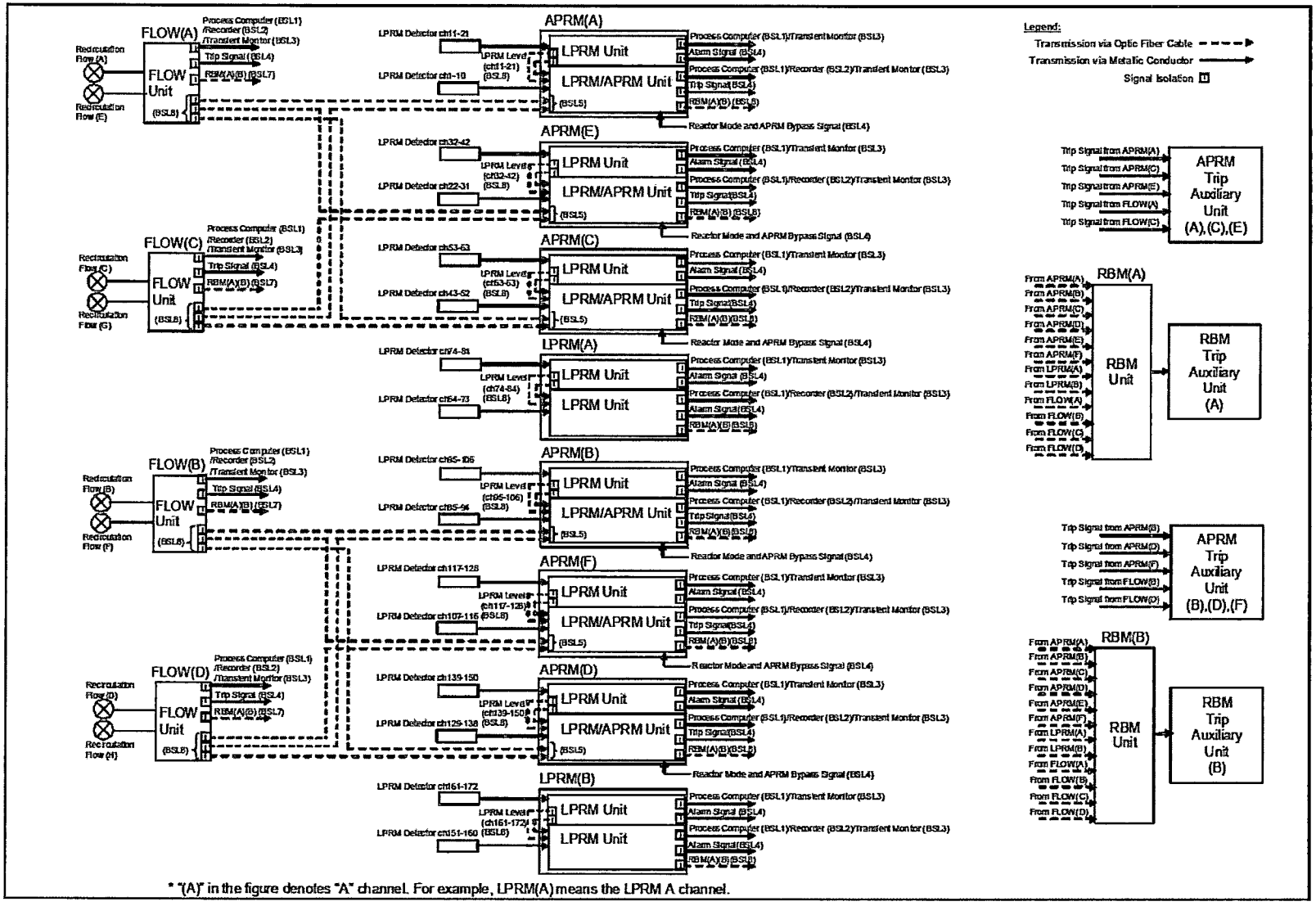


Figure II-A-7-1 Typical PRM System Configuration for BWR-5 with 172 LPRM Signal

Table II-A-7-2 Applied Module for BWR-5 PRM system

Module Name	Module Model Number*1	Number of Applied Module for System Configuration shown in Figure II-A-7-1		Functional Description
		Total Number	Description Note: The system consists of 6 APRM channels (A through F) with 1 LPRM/APRM unit and 1 LPRM unit in each APRM channel, 2 LPRM channels (A and B) with 2 LPRM units in each LPRM channel, and 4 FLOW units. There are 6 APRM/LPRM units, 10 LPRM units and 4 FLOW units in the system accordingly.	
LPRM Module	HNS013 B00000	172	- 11 modules in an LPRM unit and 10 modules in an LPRM/APRM unit for APRM A, C, and E channels - 12 modules in an LPRM unit and 10 modules in an LPRM/APRM unit for APRM B, D, and F channels - 11 modules in the first LPRM unit and 10 modules in the second LPRM unit in LPRM A channel - 12 modules in the first LPRM unit and 10 modules in the second LPRM unit in LPRM B channel	LPRM function
APRM Module	HNS020 B00000	6	- 1 module in an LPRM/APRM unit	APRM function
SQ-ROOT Module	HNS030 B00000	8	- 2 modules in a FLOW unit	Square root arithmetic function
FLOW Module	HNS040 B00000	4	- 1 module in a FLOW unit	Recirculation-flow calculation, trip and alarm functions
STATUS Module	HNS091 B00000	6	- 1 module in an LPRM/APRM unit	Data reception status and power supply voltage monitoring status indications
STATUS Module	HNS093 B00000	14	- 1 module in an LPRM unit - 1 module in a FLOW unit	Power supply voltage monitoring status indication
MUX Module	HNS260 B00000	2	- 1 module in one of the 2 LPRM units in an LPRM channel	Multiplexing module for LPRM data transmission
BLANK Module	HNS490 B00000	12	- 2 modules in an LPRM unit for APRM A, C, and E channels - 2 modules in one of the 2 LPRM units in LPRM A channel - 1 module in an LPRM unit for APRM B, D, and F channels - 1 module in one of the 2 LPRM units in LPRM B channel	Dummy LPRM module to fill open slots when the LPRM unit is not filled with 13 LPRM Modules
LVPS Module	HNS500 B00000	40	- 2 modules in each unit in the system	+5V and ±15V power supply to each module
AO Module	HNS515 B00000	16	- 1 module in an LPRM/APRM unit - 1 module in an LPRM unit	Analog outputs to the Transient Monitor
AO Module	HNS516 B00000	10	- 1 module in an LPRM/APRM unit - 1 module in a FLOW unit	Analog outputs to recorders

Module Name	Module Model Number*1	Number of Applied Module for System Configuration shown in Figure II-A-7-1		Functional Description
		Total Number	Description Note: The system consists of 6 APRM channels (A through F) with 1 LPRM/APRM unit and 1 LPRM unit in each APRM channel, 2 LPRM channels (A and B) with 2 LPRM units in each LPRM channel, and 4 FLOW units. There are 6 APRM/LPRM units, 10 LPRM units and 4 FLOW units in the system accordingly.	
AO Module	HNS517 B00000	4	- 1 module in a FLOW unit	Analog outputs to the Transient Monitor
AO Module	HNS518 B00000	20	- 1 module in each unit in the system	Analog outputs to the process computer
DIO Module	HNS520 B00000	20	- 1 module in each unit in the system	Discrete signal input and output module
TRN Module	HNS0531 B00001	24	- 1 module in an LPRM/APRM unit - 1 module in an LPRM unit - 2 modules in a FLOW unit	Optical data transmission module
RCV Module	HNS0541 B00001	8	- 1 module in an LPRM/APRM unit - 1 module in one of the 2 LPRM units in each LPRM channel	Optical data reception module

*1: Each Module has a Type number for configuration control. When a module design is changed, a type number of each module is changed to a new revised, unique type number.

II-A-7.2 [Deleted]

Figure II-A-7-2 [Deleted]

Table II-A-7-3 [Deleted]

II-A-7.3 Configuration for BWR-3 with 88 LPRM Signals

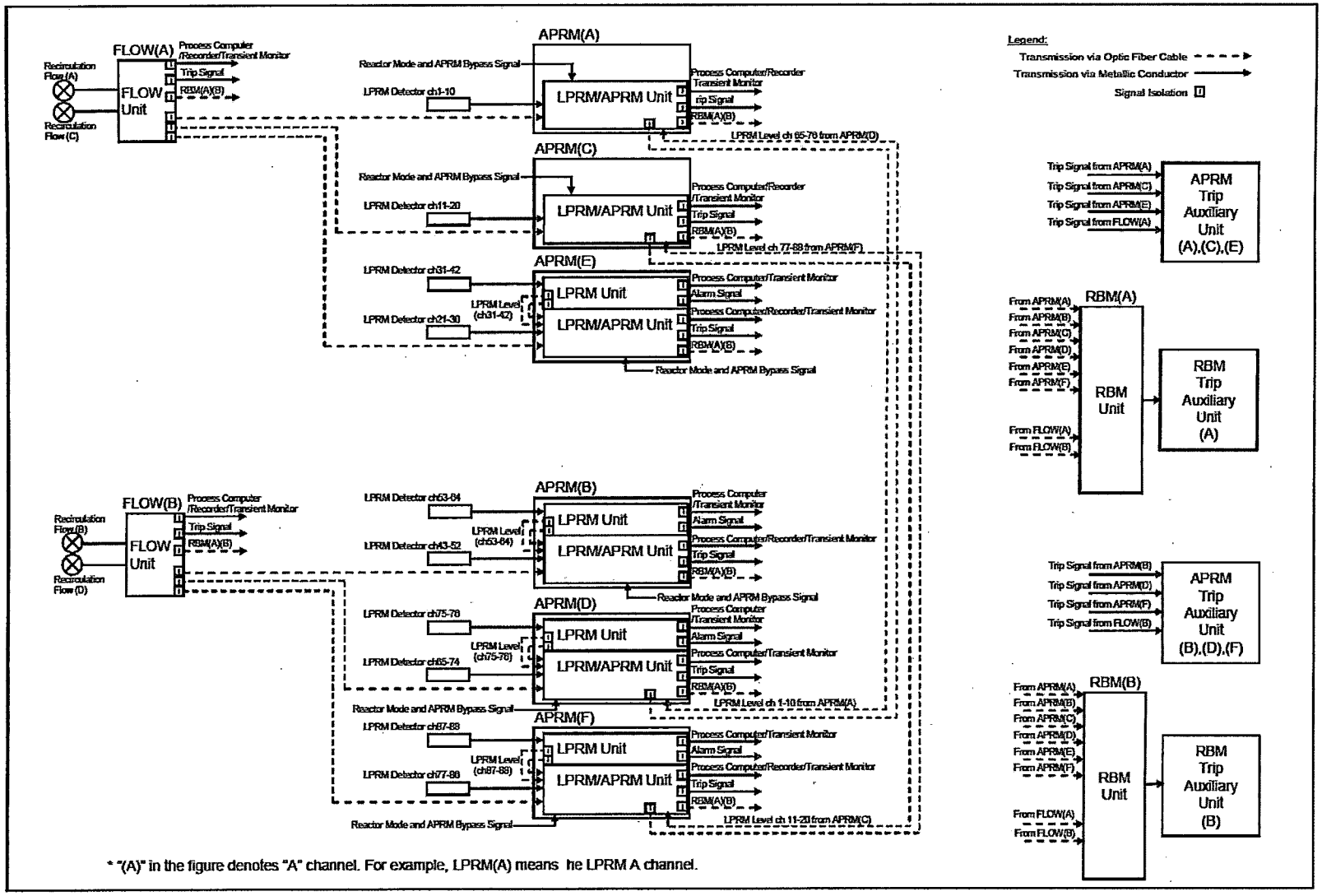
Figure II-A-7-3 shows a typical PRM system configuration for a BWR-3 design with 88 LPRM signals. The applied modules for this configuration are listed in Table II-A-7-4.

The PRM system provides the analog signals of the LPRM levels to the OPRM system through a fiber communication link as described in Section II-A-7.8.

When the PRM system is applied to a BWR-3 with 88 LPRM signals, some LPRM detector signals are shared between two common APRM channels as shown in Figure II-A-7-3. To adapt for this signal sharing, the chassis and APRM module for LPRM/APRM unit of APRM Channels A, C, D, and F need to be modified from the hardware identified in Section II-A-3 of this guide as follows:

- The middle plane of the chassis for the LPRM/APRM unit is modified to achieve following functions:
  - An additional TRN module sends common LPRM detector signals to another PRM/APRM unit in common channels.
  - A DIO module sends inoperable status signal of the unit to one of the LPRM/APRM units in the common channels.
  - The APRM module receives inoperable status signal from another LPRM/APRM unit the in common channels through a DIO module.
- The APRM module is modified to change allowable LPRM bypass number in accordance with the inoperative status signal from another LPRM/APRM unit in common channels.

The modifications described above are minor changes from the hardware identified in Section II-A-3 of this guide and use hardware that has already been type tested and qualified, so additional qualification tests are not required for the modified BWR-3 PRM system.



* "(A)" in the figure denotes "A" channel. For example, LPRM(A) means he LPRM A channel.

Figure II-A-7-3 Typical PRM System Configuration for BWR-3 with 88 LPRM Signals

Table II-A-7-4 Applied Module for BWR-3 PRM system

Module Name	Module Model Number*1	Number of Applied Module for System Configuration shown in Figure II-A-7-3		Functional Description
		Total number	Description Note: The system consists of 6 APRM channels (A through F) and 2 FLOW units. The APRM channels E, B, D, and F have 1 LPRM/APRM unit and 1 LPRM unit. The APRM channels A and C have 1 APRM/LPRM unit. There are 6 APRM/LPRM units, 4 LPRM units and 2 FLOW units in the system.	
LPRM Module	HNS013 B00000	88	- 12 modules in an LPRM unit and 10 modules in an LPRM/APRM unit for APRM B and E channels - 10 modules in an LPRM/APRM unit for APRM A and C channels - 2 modules in an LPRM unit and 10 modules in an LPRM/APRM unit for APRM D and F channels	LPRM function
APRM Module	HNS020 B00000	6	- 1 module in an LPRM/APRM unit	APRM function
SQ-ROOT Module	HNS030 B00000	4	- 2 modules in a FLOW unit	Square root arithmetic function
FLOW Module	HNS040 B00000	2	- 1 module in a FLOW unit	Recirculation-flow calculation, trip and alarm functions
STATUS Module	HNS091 B00000	6	- 1 module in an LPRM/APRM unit	Data reception status, power supply voltage monitoring status indications
STATUS Module	HNS093 B00000	6	- 1 module in an LPRM unit - 1 module in a FLOW unit	Power supply voltage monitoring status indication
BLANK Module	HNS490 B00000	24	- 1 module in an LPRM unit for APRM B and E channels - 11 modules in an LPRM unit for APRM D and F channels	Dummy LPRM module to fill open slots
LVPS Module	HNS500 B00000	24	- 2 modules in each unit in the system	+5V and ±15V power supply to each module
AO Module	HNS515 B00000	10	- 1 module in an LPRM unit - 1 module in an LPRM/APRM unit	Analog outputs to the Transient Monitor
AO Module	HNS516 B00000	8	- 1 module in an LPRM/APRM unit - 1 module in a FLOW unit	Analog outputs to recorders
AO Module	HNS517 B00000	2	- 1 module in a FLOW unit	Analog outputs to the Transient Monitor
AO Module	HNS518 B00000	12	- 1 module in each unit in the system	Analog outputs to the process computer
DIO Module	HNS520 B00000	12	- 1 module in each unit in the system	Discrete signal input and output module

Module Name	Module Model Number*1	Number of Applied Module for System Configuration shown in Figure II-A-7-3		Functional Description
		Total number	Description Note: The system consists of 6 APRM channels (A through F) and 2 FLOW units. The APRM channels E, B, D, and F have 1 LPRM/APRM unit and 1 LPRM unit. The APRM channels A and C have 1 APRM/LPRM unit. There are 6 APRM/LPRM units, 4 LPRM units and 2 FLOW units in the system.	
TRN Module	HNS0531 B00001	20	- 1 module in an LPRM unit and 2 modules in an LPRM/APRM unit for APRM B, D, E and F channels - 2 modules in an LPRM/APRM unit for APRM A and C channels - 2 modules in a FLOW unit	Optical data transmission module
RCV Module	HNS0541 B00001	8	- 1 module in an LPRM/APRM unit for APRM A, B, C and E channels - 2 module in an LPRM/APRM unit for APRM D and F channels	Optical data reception module

*1: Each Module has a Type number for configuration control. When a module design is changed, a type number of each module is changed to a new revised, unique type number.

II-A-7.4 Configuration for BWR-4 with 124 LPRM Signals

Figure II-A-7-4 shows a typical PRM system configuration for BWR-4 with 124 LPRM signals. The applied modules for this configuration are listed in Table II-A-7-5.

The PRM system provides the LPRM levels to the OPRM system through a fiber communication link as described in Section II-A-7.7.

When the PRM system is applied to a BWR-4 with 124 LPRM signals, LPRM channel (A) and LPRM channel (B) transmit the LPRM data to the Rod Block Monitor (RBM). Since the LPRM unit described in Section II-A-3 has no function to collect LPRM data from another LPRM unit, the MUX module needs to be applied to provide the required data transmission. The MUX module was not part of the BWR-5 PRM qualification. The MUX modules will be subjected to appropriate equipment qualification before being used (see also Section II-2.2.4).

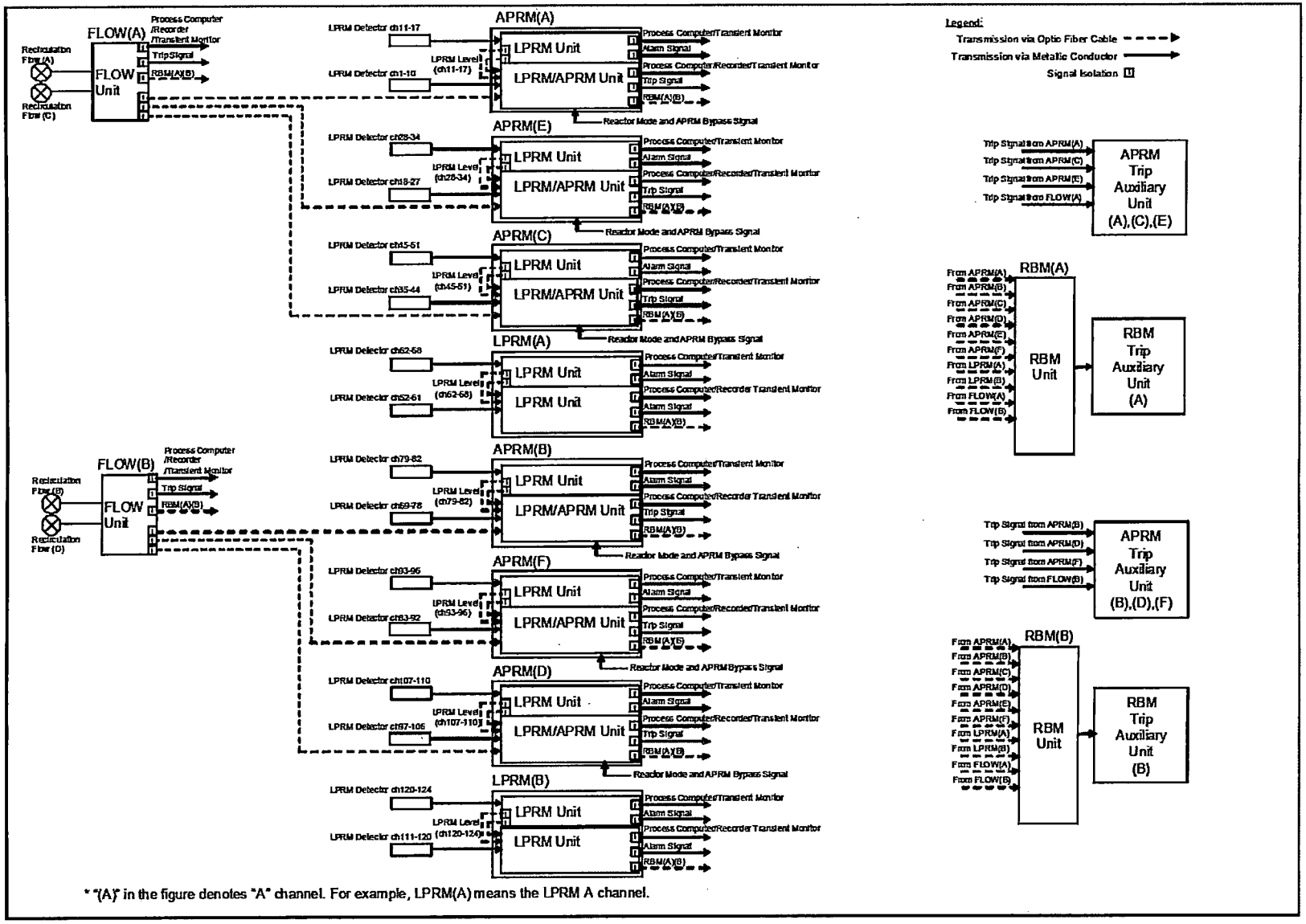


Figure II-A-7-4 Typical PRM System Configuration for BWR-4 with 124 LPRM Signal

Table II-A-7-5 Applied Module for BWR-4 PRM system

Module Name	Module Model Number*1	Number of Applied Module for System Configuration shown in Figure II-A-7-4		Functional Description
		Total Number	Description Note: The system consists of 6 APRM channels (A through F) with 1 LPRM/APRM unit and 1 LPRM unit in each APRM channel, 2 LPRM channels (A and B) with 2 LPRM units in each LPRM channel, and 2 FLOW units. There are 6 APRM/LPRM units, 10 LPRM units and 2 FLOW units in the system accordingly.	
LPRM Module	HNS013 B00000	124	- 7 modules in an LPRM unit and 10 modules in an LPRM/APRM unit for the APRM A, C, and E channels - 4 modules in an LPRM unit and 10 modules in an LPRM/APRM unit for the APRM B, D, and F channels - 7 modules in the first LPRM unit and 10 modules in the second LPRM unit in the LPRM A channel - 4 modules in the first LPRM unit and 10 modules in the second LPRM unit in the LPRM B channel	LPRM function
APRM Module	HNS020 B00000	6	- 1 module in an LPRM/APRM unit	APRM function
SQ-ROOT Module	HNS030 B00000	4	- 2 modules in a FLOW unit	Square root arithmetic function
FLOW Module	HNS040 B00000	2	- 1 module in a FLOW unit	Recirculation-flow calculation, trip and alarm functions
STATUS Module	HNS091 B00000	6	- 1 module in an LPRM/APRM unit	Data reception status, power supply voltage monitoring status indications
STATUS Module	HNS093 B00000	12	- 1 module in an LPRM unit - 1 module in a FLOW unit	Power supply voltage monitoring status indication
MUX Module	HNS260 B00000	2	- 1 module in one of the 2 LPRM units in an LPRM channel	Multiplexing module for LPRM data transmission
BLANK Module	HNS490 B00000	60	- 6 modules in an LPRM unit for the APRM A, C and E channels - 6 modules in one of the 2 LPRM units in the LPRM A channel - 9 modules in an LPRM unit for the APRM B, D and F channels - 9 modules in one of the 2 LPRM units in the LPRM B channel	Dummy LPRM module to fill open slots when the LPRM unit is not filled with 13 LPRM Modules
LVPS Module	HNS500 B00000	36	- 2 modules in each unit in the system	+5V and ±15V power supply to each module
AO Module	HNS515 B00000	16	- 1 module in an LPRM/APRM unit - 1 module in an LPRM unit	Analog outputs to the Transient Monitor
AO Module	HNS516 B00000	8	- 1 module in an LPRM/APRM unit - 1 module in a FLOW unit	Analog outputs to recorders

Module Name	Module Model Number*1	Number of Applied Module for System Configuration shown in Figure II-A-7-4		Functional Description
		Total Number	Description Note: The system consists of 6 APRM channels (A through F) with 1 LPRM/APRM unit and 1 LPRM unit in each APRM channel, 2 LPRM channels (A and B) with 2 LPRM units in each LPRM channel, and 2 FLOW units. There are 6 APRM/LPRM units, 10 LPRM units and 2 FLOW units in the system accordingly.	
AO Module	HNS517 B00000	2	- 1 module in a FLOW unit	Analog outputs to the Transient Monitor
AO Module	HNS518 B00000	18	- 1 module in each unit in the system	Analog outputs to the process computer
DIO Module	HNS520 B00000	18	- 1 module in each unit in the system	Discrete signal input and output module
TRN Module	HNS0531 B00001	20	- 1 module in an LPRM/APRM unit - 1 module unit in an LPRM unit - 2 modules in a FLOW unit	Optical data transmission module
RCV Module	HNS0541 B00001	8	- 1 module in an LPRM/APRM unit - 1 module in one of the 2 LPRM units in each LPRM channel	Optical data reception module

*1: Each Module has a Type number for configuration control. When a module design is changed, a type number of each module is changed to a new revised, unique type number.

II-A-7.5 Configuration for BWR-6 with 132 LPRM Signals

Figure II-A-7-5 shows a typical PRM system configuration for a BWR-6 design with 132 LPRM signals. The applied modules for this configuration are listed in Table II-A-7-6.

The PRM system provides the signals of the LPRM levels to the OPRM system through a fiber communication link as described in Section II-A-7.7.

When the PRM system is applied to BWR-6 with 132 LPRM signals, the following modifications from the hardware configuration identified in Section II-A-3 are necessary:

- Five unused LPRM modules, which are not required for the BWR-6 application, used for APRM A, E, C, and G channels in the LPRM unit are replaced with five BLANK modules.
- Six unused LPRM modules, which are not required for the BWR-6 application, used for APRM B, F, D, and H channels in the LPRM unit are replaced with six BLANK modules.

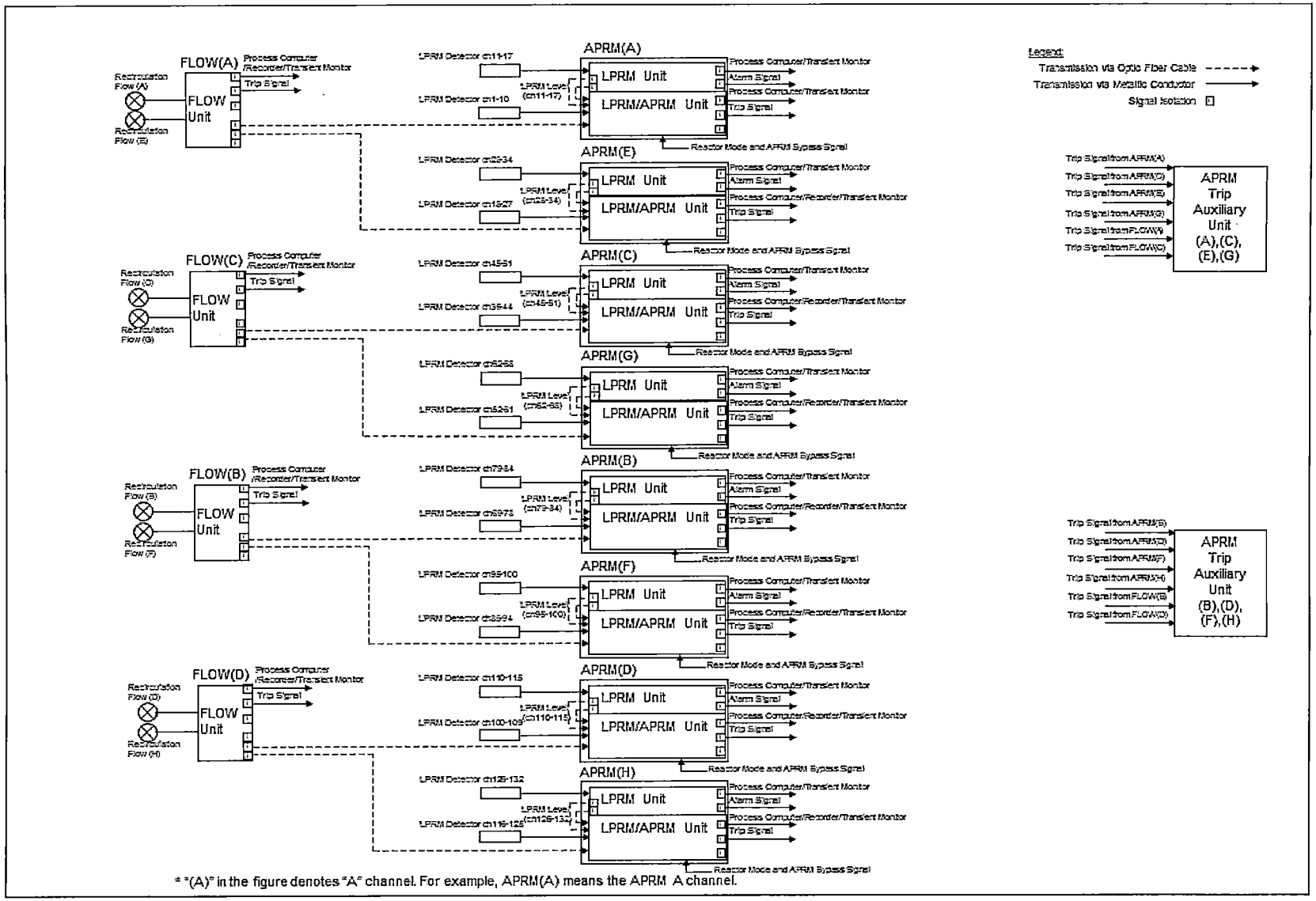


Figure II-A-7-5 Typical PRM System Configuration for BWR-6 with 132 LPRM Signals

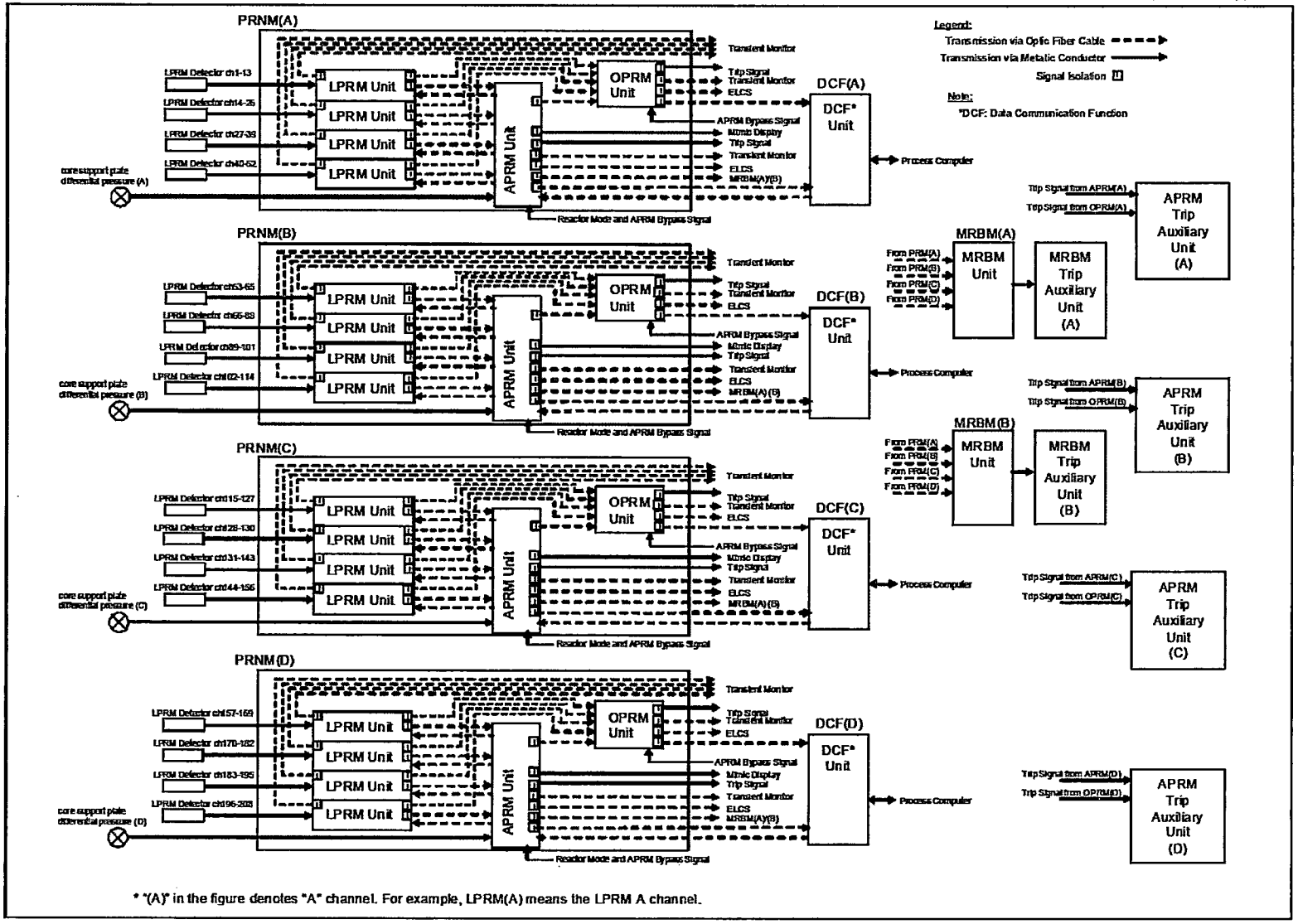
Table II-A-7-6 Applied Module for BWR-6 PRM system

Module Name	Module Model Number*1	Number of Applied Module for System Configuration shown in Figure II-A-7-5		Functional Description
		Total Number	Description Note: The system consists of 6 APRM channels (A through H) with 1 LPRM/APRM unit and 1 LPRM unit in each APRM channel, and 4 FLOW units. There are 8 APRM/LPRM units, 8 LPRM units and 4 FLOW units in the system accordingly.	
LPRM Module	HNS013 B00000	132	- 7 modules in an LPRM unit and 10 modules in an LPRM/APRM unit for the APRM A, C, E, and G channels - 6 modules in an LPRM unit and 10 modules in an LPRM/APRM unit for the APRM B, D, F and H channels	LPRM function
APRM Module	HNS020 B00000	8	- 1 module in an LPRM/APRM unit	APRM function
SQ-ROOT Module	HNS030 B00000	8	- 2 modules in a FLOW unit	Square root arithmetic function
FLOW Module	HNS040 B00000	4	- 1 module in a FLOW unit	Recirculation-flow calculation, trip and alarm functions
STATUS Module	HNS091 B00000	8	- 1 module in an LPRM/APRM unit	Data reception status, power supply voltage monitoring status indications
STATUS Module	HNS093 B00000	12	- 1 module in an LPRM unit - 1 module in a FLOW unit	Power supply voltage monitoring status indication
BLANK Module	HNS490 B00000	52	- 6 modules in an LPRM unit for APRM A, C, E, and G channels - 7 modules in an LPRM unit for APRM B, D, F, and H channels	Dummy LPRM module to fill open slots
LVPS Module	HNS500 B00000	40	- 2 modules in each unit in the system	+5V and ±15V power supply to each module
AO Module	HNS515 B00000	16	- 1 module in an LPRM/APRM unit - 1 module in an LPRM unit	Analog outputs to the Transient Monitor
AO Module	HNS516 B00000	12	- 1 module in an LPRM/APRM unit - 1 module in a FLOW unit	Analog outputs to recorders
AO Module	HNS517 B00000	4	- 1 module in a FLOW unit	Analog outputs to the Transient Monitor
AO Module	HNS518 B00000	20	- 1 module in each unit in the system	Analog outputs to the process computer
DIO Module	HNS520 B00000	20	- 1 module in each unit in the system	Discrete signal input and output module
TRN Module	HNS0531 B00001	24	- 1 module in an LPRM/APRM unit - 1 module in an LPRM unit - 2 modules in a FLOW unit	Optical data transmission module
RCV Module	HNS0541 B00001	8	- 1 module in an LPRM/APRM unit	Optical data reception module

*1: Each Module has a Type number for configuration control. When a module design is changed, a type number of each module is changed to a new revised, unique type number.

II-A-7.6 ABWR OPRM with 208 LPRM Signals

A typical Power Range Neutron Monitoring (PRNM) system configuration for an ABWR having 208 LPRM signals is shown in Figure II-A-7-6. The applied safety-related modules for this configuration are listed in Table II-A-7-7. The PRNM system includes OPRM. Only the OPRM unit is within the scope of this Application Guide. Details of the PRNM are provided to illustrate the expected inputs to an ABWR OPRM system.



* "(A)" in the figure denotes "A" channel. For example, LPRM(A) means the LPRM A channel.

Figure II-A-7-6 Typical PRNM System Configuration for ABWR with 208 LPRM Signals

Table II-A-7-7 Applied Module for ABWR PRNM system

Module Name	Module Model Number*1	Number of Applied Module for System Configuration shown in Figure II-A-7-6		Functional Description
		Total Number	Description Note: The system consists of 4 divisions with 1 APRM unit, 4 LPRM units and 1 OPRM unit in each division.	
LPRM Module	HNS0302 B00000	208	- 13 modules in a LPRM unit	LPRM function
APRM Module	HNS0311 B00000	4	- 1 module in an APRM unit	APRM function
FLOW Module	HNS0321 B00000	4	- 1 module in an APRM unit	Core-flow calculation, trip and alarm functions
CAL/ST Module	HNS0330 B00000	16	- 1 module in an LPRM unit	Power status and Input status indications. LPRM calibration currents are calculated and provided to LPRM modules.
GAF/ST Module	HNS0341 B00000	4	- 1 module in an APRM unit	Power status and Input status indications. Gain Adjustment Factor (GAF) download and output to LPRM units
CELL Module	HNS0400 B00000	4	- 1 module in an OPRM unit	LPRM Levels are converted to Normalized Oscillation Signal
DAT/ST Module	HNS0410 B00000	4	- 1 module in an OPRM unit	Power status and Input status indications OPRM data are multiplexed
AGRD Module	HNS0420 B00000	4	- 1 module in an OPRM unit	Amplitude-Based Detection Algorithm judgment is performed. Growth Rate-Based Detection Algorithm judgment is performed.
PBD Module	HNS0430 B00000	4	- 1 module in an OPRM unit	Period-based Detection Algorithm judgment is performed.
LVPS Module	HNS0500 B00000	48	- 2 modules in each unit	+5V and ±15V power supply to each module
AO Module	HNS0515 B00000	20	- 1 module in LPRM unit - 1 module in APRM unit	Analog outputs to the mimic display on the main control panel and the Transient Monitor
DIO Module	HNS0520 B00000	24	- 1 module in a LPRM unit - 1 module in a APRM unit - 1 module in a OPRM unit	Discrete signal input and output module
TRN Module	HNS0531 B00001	36	- 1 module in a LPRM unit - 3 modules in a APRM unit - 2 modules in a OPRM unit	Optical data transmission module
RCV Module	HNS0541 B00001	32	- 1 module in a LPRM unit - 2 modules in a APRM unit - 2 modules in a OPRM unit	Optical data reception module

*1: Each Module has a Type number for configuration control. When a module design is changed, a type number of each module is changed to a new revised, unique type number.

The OPRM unit configuration for ABWR is shown in Figure II-A-7-7 and described in Table II-A-7-8.

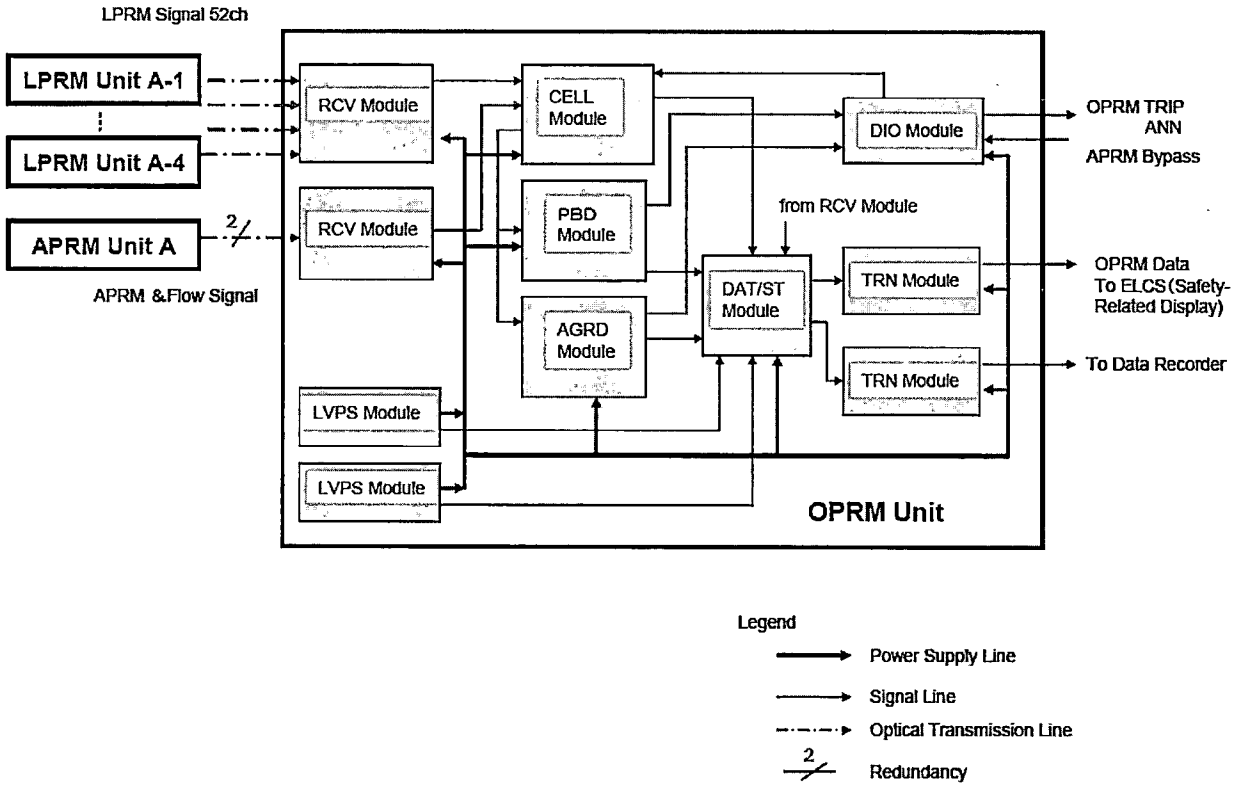


Figure II-A-7-7 Unit/Module Configuration for OPRM for ABWR

Table II-A-7-8 Unit/Module Configuration for OPRM for ABWR

Module Name	Module Model Number*1	Number of Applied Module for OPRM System Configuration shown in Figure II-A-7-7		Functional Description
		Total number	Description Note: The system has 4 divisions with 1 OPRM unit in each division.	
CELL Module	HNS0400 B00000	4	- 1 module in each OPRM unit	LPRM Levels are converted to Normalized Oscillation Signal
DAT/ST Module	HNS0410 B00000	4	- 1 module in each OPRM unit	Power status and Input status indications OPRM data are multiplexed
AGRD Module	HNS0420 B00000	4	- 1 module in each OPRM unit	Amplitude-Based Detection Algorithm judgment is performed. Growth Rate-Based Detection Algorithm judgment is performed.
PBD Module	HNS0430 B00000	4	- 1 module in each OPRM unit	Period-based Detection Algorithm judgment is performed.
LVPS Module	HNS0500 B00000	8	- 2 modules in each OPRM unit	+5V and ±15V power supply to each module
DIO Module	HNS0520 B00000	4	- 1 module in each OPRM unit	Discrete signal input and output module
TRN Module	HNS0531 B00001	8	- 2 modules in each OPRM unit	Optical data transmission module
RCV Module	HNS0541 B00001	8	- 2 modules in each OPRM unit	Optical data reception module

*1: Each Module has a Type number for configuration control. When a module design is changed, a type number of each module is changed to a new revised, unique type number.

Since the OPRM hardware modules to be used in ABWR have passed equipment qualification, and since the VHDL code used in the equipment qualification is the same as that used in this configuration, no additional type testing for OPRM for ABWR is required. The PRNM system for ABWR is outside the scope of this LTR.

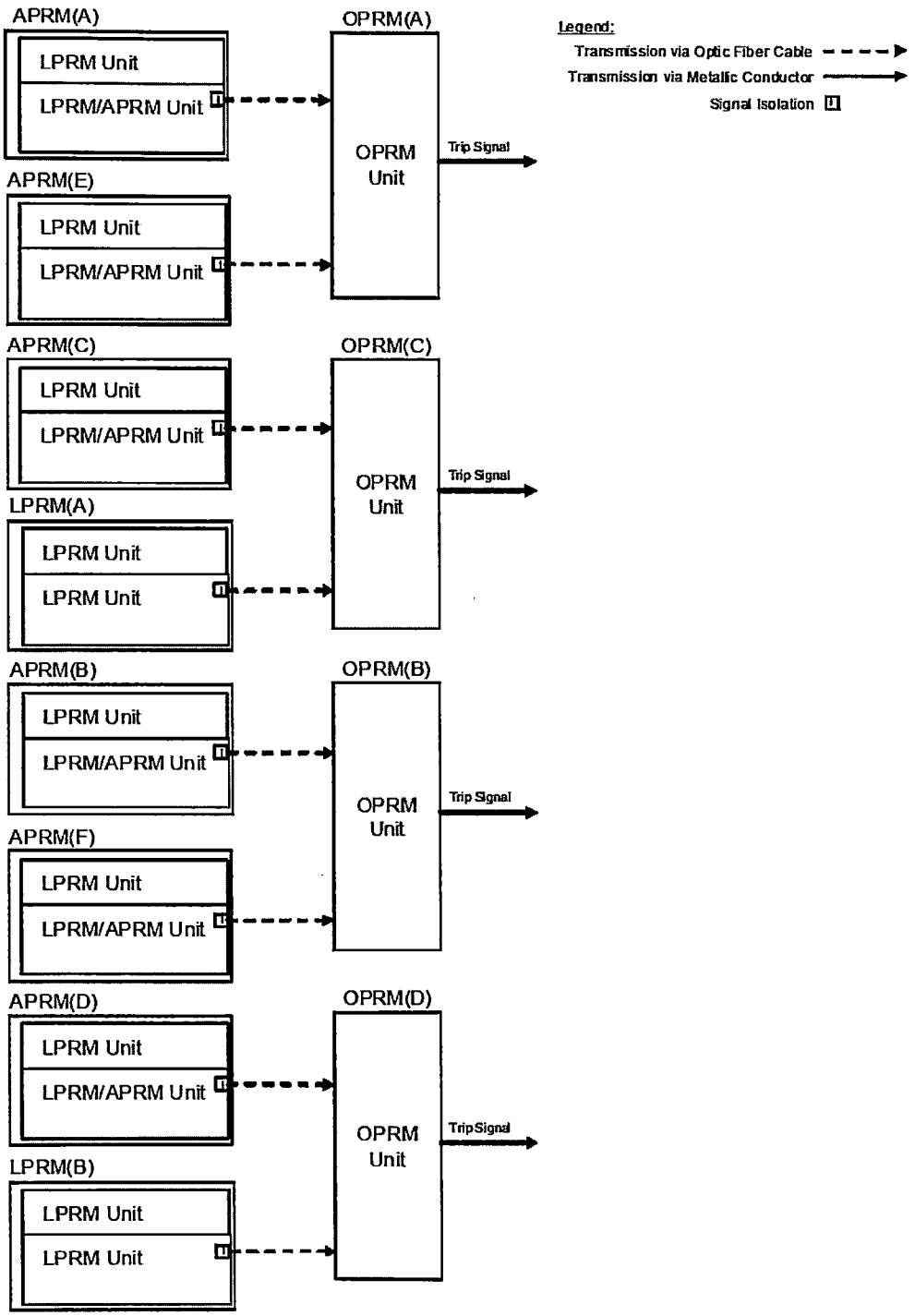
II-A-7.7 Interface Configuration between PRM and OPRM for Large Core BWR

The OPRM algorithm to detect thermal hydraulic oscillation in BWR-3, BWR-4, BWR-5, and BWR-6 designs is the same as the OPRM in an ABWR. Differences between the ABWR OPRM and the BWRs OPRM are in the assignment of LPRM signals to OPRM cell and parameter setpoints. Therefore, the ABWR OPRM can be applied to BWR-3, BWR-4, BWR-5, and BWR-6 designs with only minor logic changes in the FPGAs.

Figure II-A-7-8 shows the typical interface configurations between PRM and OPRM for BWR-4 and BWR-5 designs. The typical interface configuration for a BWR-6 design is shown in Figure II-A-7-9. Table II-A-7-9 lists the OPRM safety-related modules in this configuration. APRM and OPRM connections for an ABWR are shown in Figure II-A-7-6. The same fiber optic communication boards are used in all configurations; although, the connections are different between the large core application and the small core application

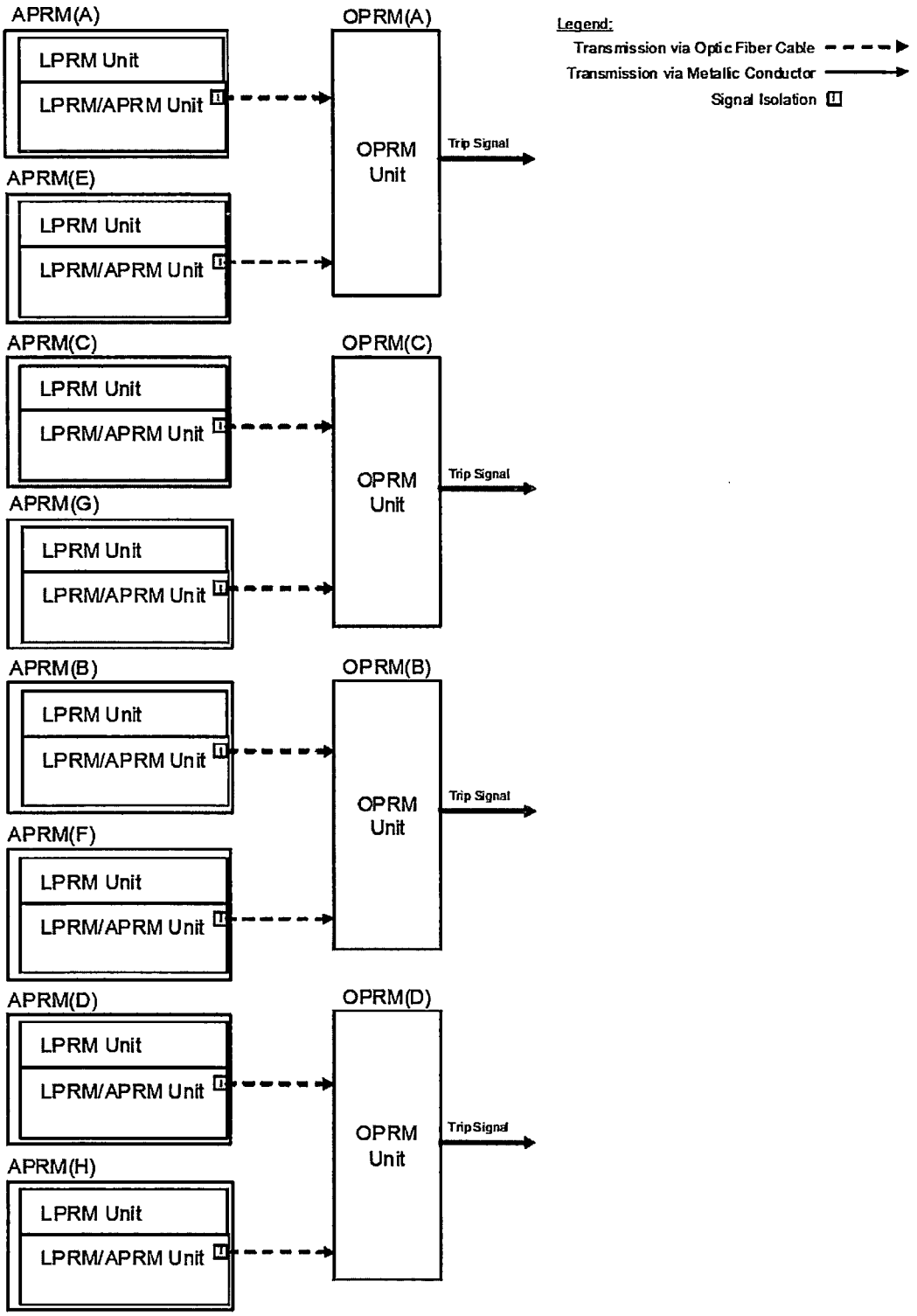
LPRM units transmit their LPRM data to the OPRM units. LPRM/APRM units transmit their LPRM data, APRM data, and FLOW data to the OPRM units.

The interface configuration provided in this guide provides separation and isolation between electrical divisions and channels, based on the existing plant requirements.



* "(A)" in the figure denotes "A" channel. For example, LPRM(A) means the LPRM A channel.

Figure II-A-7-8 Typical Interface Configuration between PRM and OPRM for BWR-4 and BWR-5



* "(A)" in the figure denotes "A" channel. For example, LPRM(A) means the LPRM A channel.

Figure II-A-7-9 Typical Interface Configuration between PRM and OPRM for BWR-6

Table II-A-7-9 Applied Module for Large Core OPRM

Module Name	Module Model Number*1	Number of Applied Module for OPRM System Configuration shown in Figure II-A-7-8 and Figure II-A-7-9		Functional Description
		Total number	Description Note: The system has 4 OPRM units.	
CELL Module	HNS0400 B00000	4	- 1 module in each OPRM unit	LPRM Levels are converted to Normalized Oscillation Signal
DAT/ST Module	HNS0410 B00000	4	- 1 module in each OPRM unit s	Power status and Input status indications OPRM data are multiplexed
AGRD Module	HNS0420 B00000	4	- 1 module in each OPRM unit	Amplitude-Based Detection Algorithm judgment is performed. Growth Rate-Based Detection Algorithm judgment is performed.
PBD Module	HNS0430 B00000	4	- 1 module in each OPRM unit	Period-based Detection Algorithm judgment is performed.
LVPS Module	HNS0500 B00000	8	- 2 modules in each OPRM unit	+5V and ±15V power supply to each module
DIO Module	HNS0520 B00000	4	- 1 module in each OPRM unit	Discrete signal input and output module
TRN Module	HNS0531 B00001	8	- 2 modules in each OPRM unit	Optical data transmission module
RCV Module	HNS0541 B00001	8	- 2 modules in each OPRM unit	Optical data reception module

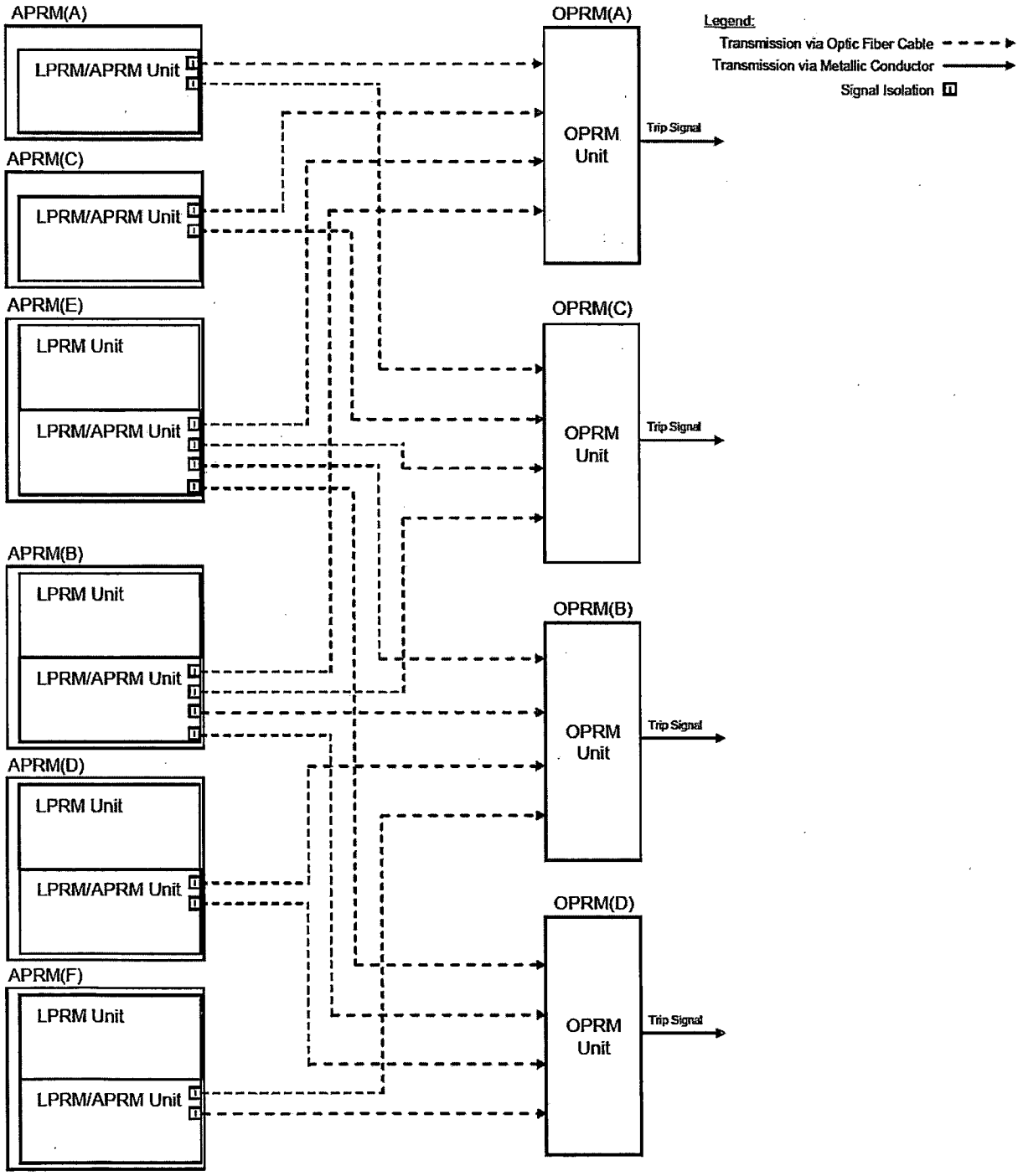
**1: Each Module has a Type number for configuration control. When a module design is changed, a type number of each module is changed to a new revised, unique type number.

II-A-7.8 Interface Configuration between PRM and OPRM for Small Core BWR

Figure II-A-7-10 shows a typical interface configuration between PRM and OPRM for BWR designs with less than 120 LPRM signals (small core) Table II-A-7-10 lists the OPRM modules in this configuration.

LPRM units transmit their LPRM data to the OPRM units. LPRM/APRM units transmit their LPRM data, APRM data, and FLOW data to the OPRM units.

The interface configuration provided in this guide provides separation and isolation between electrical divisions and channels, based on the existing plant requirements.



* "(A)" in the figure denotes "A" channel. For example, LPRM(A) means the LPRM A channel.

Figure II-A-7-10 Typical Interface Configuration between PRM and OPRM for Small Core BWR

Table II-A-7-10 Applied Module for Small Core OPRM

Module Name	Module Model Number*1	Number of Applied Module for OPRM System Configuration shown in Figure II-A-7-10		Functional Description
		Total number	Description Note: The system has 4 OPRM units.	
CELL Module	HNS0400 B00000	4	1 module in each OPRM unit	LPRM Levels are converted to Normalized Oscillation Signal
DAT/ST Module	HNS0410 B00000	4	1 module in each OPRM unit	Power status and Input status indications OPRM data are multiplexed
AGRD Module	HNS0420 B00000	4	1 module in each OPRM unit	Amplitude-Based Detection Algorithm judgment is performed. Growth Rate-Based Detection Algorithm judgment is performed.
PBD Module	HNS0430 B00000	4	1 module in each OPRM unit	Period-based Detection Algorithm judgment is performed.
LVPS Module	HNS0500 B00000	8	2 modules in each OPRM unit	+5V and ±15V power supply to each module
DIO Module	HNS0520 B00000	4	1 module in each OPRM unit	Discrete signal input and output module
TRN Module	HNS0531 B00001	8	2 modules in each OPRM unit	Optical data transmission module
RCV Module	HNS0541 B00001	8	2 modules in each OPRM unit	Optical data reception module

*1: Each Module has a Type number for configuration control. When a module design is changed, a type number of each module is changed to a new revised, unique type number.

Appendix II-B. Module Summary Description

II-B-1 Introduction

This appendix includes the Module Summary Descriptions (MSDs) for the modules listed in Table II-B-1. The MSDs are in the Attachment to this Appendix.

Table II-B-1 includes the page number of each MSD in the Attachment, for reference.

Table II-B-1 also lists following information:

- Whether the module contains FPGA(s)
- Systems where the module used
- Unit where the module used
- Whether the module was qualified in PRM qualification (original process) or OPRM qualification (current process)

Table II-B-1 Module Summary Description List

Document Number	Module Name	Type Number	Module Has FPGA?	System Where Module Used	Unit Where Module Used	Qualified in	Page on Attachment (bottom right)
MEM-JHS-000108	LPRM	HNS013	yes	PRM (BWR-3,4,5,6)	LPRM, LPRM/APRM, FLOW	PRM Qualification	1-4
MEM-JHS-000110	APRM	HNS020	yes	PRM (BWR-3,4,5,6)	LPRM/APRM	PRM Qualification	5-9
MEM-JHS-000112	SQ-ROOT	HNS030	yes	PRM (BWR-3,4,5,6)	FLOW	PRM Qualification	10-13
MEM-JHS-000113	FLOW	HNS040	yes	PRM (BWR-3,4,5,6)	FLOW	PRM Qualification	14-18
MEM-JHS-000115	STATUS	HNS091	yes	PRM (BWR-3,4,5,6)	LPRM/APRM	PRM Qualification	19-21
MEM-JHS-000116	STATUS	HNS093	yes	PRM (BWR-3,4,5,6)	LPRM, FLOW	PRM Qualification	22-24
MEM-JHS-000105	TRN	HNS0531	yes	OPRM, PRM (BWR-3,4,5,6)	OPRM, LPRM, LPRM/APRM, FLOW	OPRM Qualification	25-29
MEM-JHS-000107	RCV	HNS0541	yes	OPRM, PRM (BWR-3,4,5,6)	OPRM, LPRM, LPRM/APRM	OPRM Qualification	30-33

Document Number	Module Name	Type Number	Module Has FPGA?	System Where Module Used	Unit Where Module Used	Qualified in	Page on Attachment (bottom right)
MEM-JHS-000100	LVPS	HNS500	no	PRM, OPRM	LPRM, LPRM/APRM, FLOW, OPRM	OPRM Qualification	34-36
MEM-JHS-000102	AO	HNS515, 516, 517, 518	no	PRM (BWR-3,4,5,6)	LPRM, LPRM/APRM, FLOW	PRM Qualification	37-38
MEM-JHS-000103	DIO	HNS520	no	PRM (BWR-3,4,5,6), OPRM	LPRM, LPRM/APRM, FLOW, OPRM	OPRM Qualification	39-40
MEM-JHS-000120	BLANK	HNS490	no	PRM (BWR-3,4,5,6)	LPRM	PRM Qualification	41-42
MEM-JHS-000121	CELL	HNS0400	yes	OPRM	OPRM	OPRM Qualification	43-47
MEM-JHS-000122	DAT/ST	HNS0410	yes	OPRM	OPRM	OPRM Qualification	48-51
MEM-JHS-000123	AGRD	HNS0420	yes	OPRM	OPRM	OPRM Qualification	52-56
MEM-JHS-000124	PBD	HNS0430	yes	OPRM	OPRM	OPRM Qualification	57-61

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APPENDIX II-B Attachment

LPRM Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: LPRM module

(2) Module Number: HNS013

(3) Unit and application to be used

LPRM/APRM, LPRM Units for BWR-2, 3, 4, 5 and 6 Application

(4) Number of FPGA on the module: Four

2 Functional Summary

The LPRM module controls the bias voltage applied to the in-core neutron detector, receives the current representing the LPRM power from the LPRM detector in the reactor core, converts the LPRM signal to a digital percent power value called the LPRM level, and provides that power to the APRM and OPRM for further processing.

3 Module Description

3.1 User Interfaces

Figure 1 shows the front panel of the LPRM module.

3.2 Inputs and Outputs

The LPRM module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules

The LPRM module receives an LPRM detector signal.

(2) Input signals via communication modules

N/A

3.2.2 Outputs

(1) Output signals via process input and output modules

The LPRM module provides alarm signals to the external via DIO module.

The LPRM module provides the LPRM level to the external via AO module.

(2) Output signals via communication modules

The LPRM module provides the LPRM level and a status signal to the APRM module via TRN module.

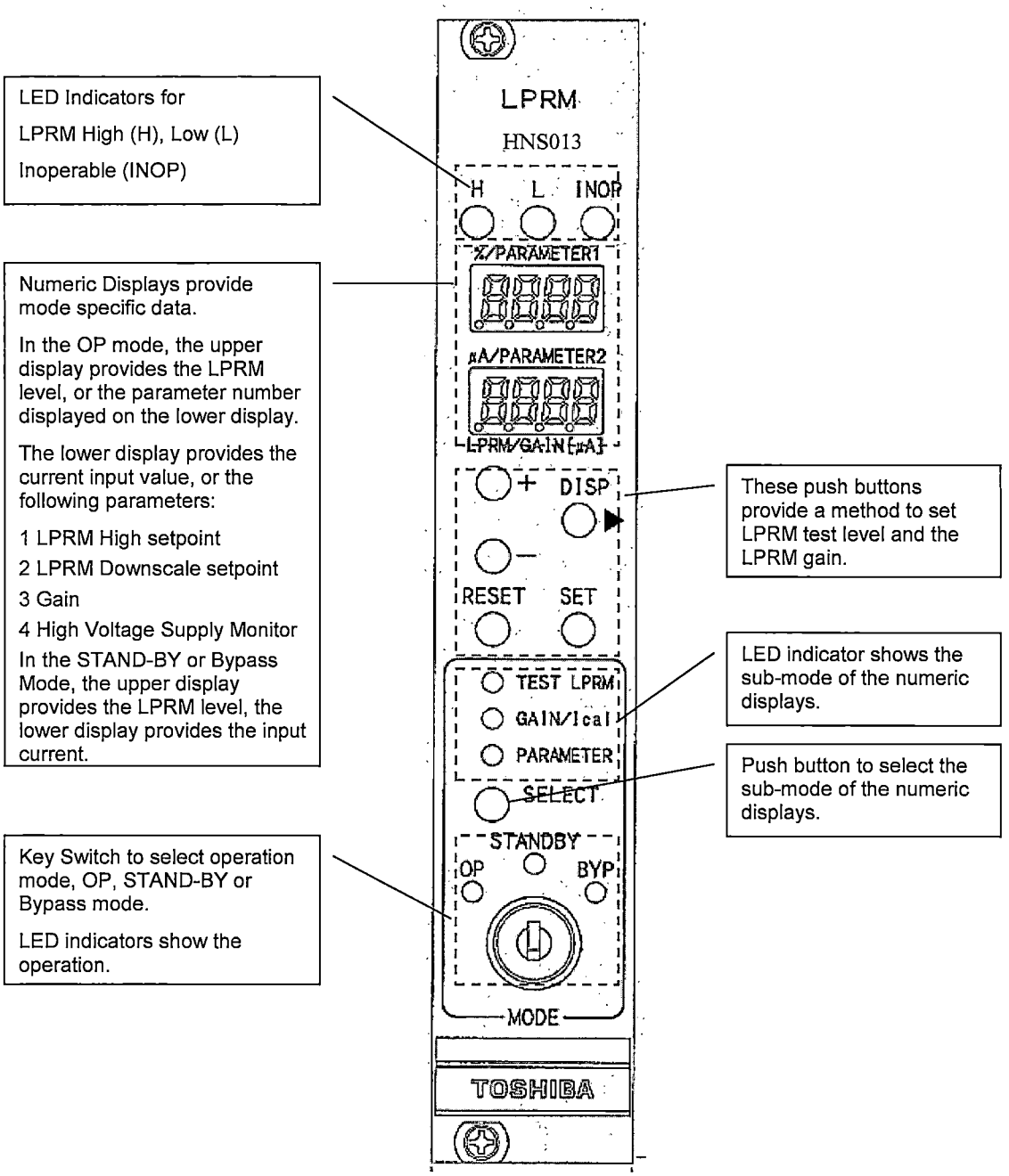

Figure 1 The front panel of the LPRM module

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the LPRM module. Table 1 provides functions of each FPGA.

a,c

Figure 2 Functional Block Diagram of LPRM module

Table 1 FPGA functions in the LPRM module

FPGA	Description

a,c

3.4 Self Diagnosis

3.4.1 Minor Failure Alarm

The LPRM module generates a minor failure alarm if one of the following occurs:

- The high voltage bias supply for the in-core neutron flux detector is not within the specification.
- An FPGA monitoring watchdog timer generates a minor failure alarm if one or more
  a,c
  The watchdog timer is reset by a

a,c
a,c
a,c

3.4.2 Inoperable Trip

N/A

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⓪ Feb.8, 2013	–	First Issue	K.Wakita Feb.8,2013	T.Tarumi Feb.8,2013	H.Ito Feb.8,2013	H.Ito Feb.8,2013
① Feb. 15, 2013	1 2 3	Descriptions in Section 2 and 3 were improved Figure number was changed from 3-1 to 1 Figure number was changed from 3-2 to 2 Table number was changed from 3-1 to 1 Description of self diagnosis was improved.	K.Wakita Feb.15, 2013	T. Tarumi Feb. 15, 2013	N. Ito Feb. 15. 2013	N. Ito Feb. 15. 2013

APRM Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: APRM module

(2) Module Number: HNS020

(3) Unit and application to be used
LPRM/APRM Unit for BWR-2, 3, 4, 5 and 6 Application

(4) Number of FPGA on the module: Eleven

2 Functional Summary

The APRM module collects the LPRM levels from the individual LPRM modules, calculates an APRM level and a Simulated Thermal Power level. If the APRM level or the Simulated Thermal Power level exceeds one or more setpoints, the APRM module generates a trip signal for the reactor trip system to process. The APRM module uses the Flow values collected from the FLOW module to calculate setpoints for the APRM level and the Simulated Thermal Power level.

3 Module Description

3.1 User Interfaces

Figure 1 shows the front panel of the APRM module.

3.2 Inputs and Outputs

The APRM module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules

The APRM module receives Reactor Mode data from the reactor Mode switch installed in the main control panel via a DIO module. The APRM module receives the APRM Bypass state from the bypass switch installed in the Main Control Room Panel via the same DIO module.

(2) Input signals via communication modules

The APRM module receives power levels from up to 22 individual LPRM modules. In BWR-5 configuration 12 LPRM modules are installed in the LPRM unit, while other 10 LPRM modules are installed in the LPRM/APRM unit in which the APRM module is installed. The TRN module in the LPRM unit that is not shown in the figure transmits the 12 LPRM data to LPRM/APRM/ unit. The RCV module in the LPRM/APRM unit receives the 12 LPRM data. The TRN module in the LPRM/APRM unit transmits the LPRM data from 10 LPRM modules in the LPRM/APRM unit. The APLRCV FPGA in the APRM module is responsible for receiving the LPRM data from

the TRN module and the RCV module.

The APRM module receives reactor core flow data and status from two Flow modules via the same RCV module that is used for receiving 12 LPRM data. The [ ]a,c FPGA is responsible for receiving the flow data.

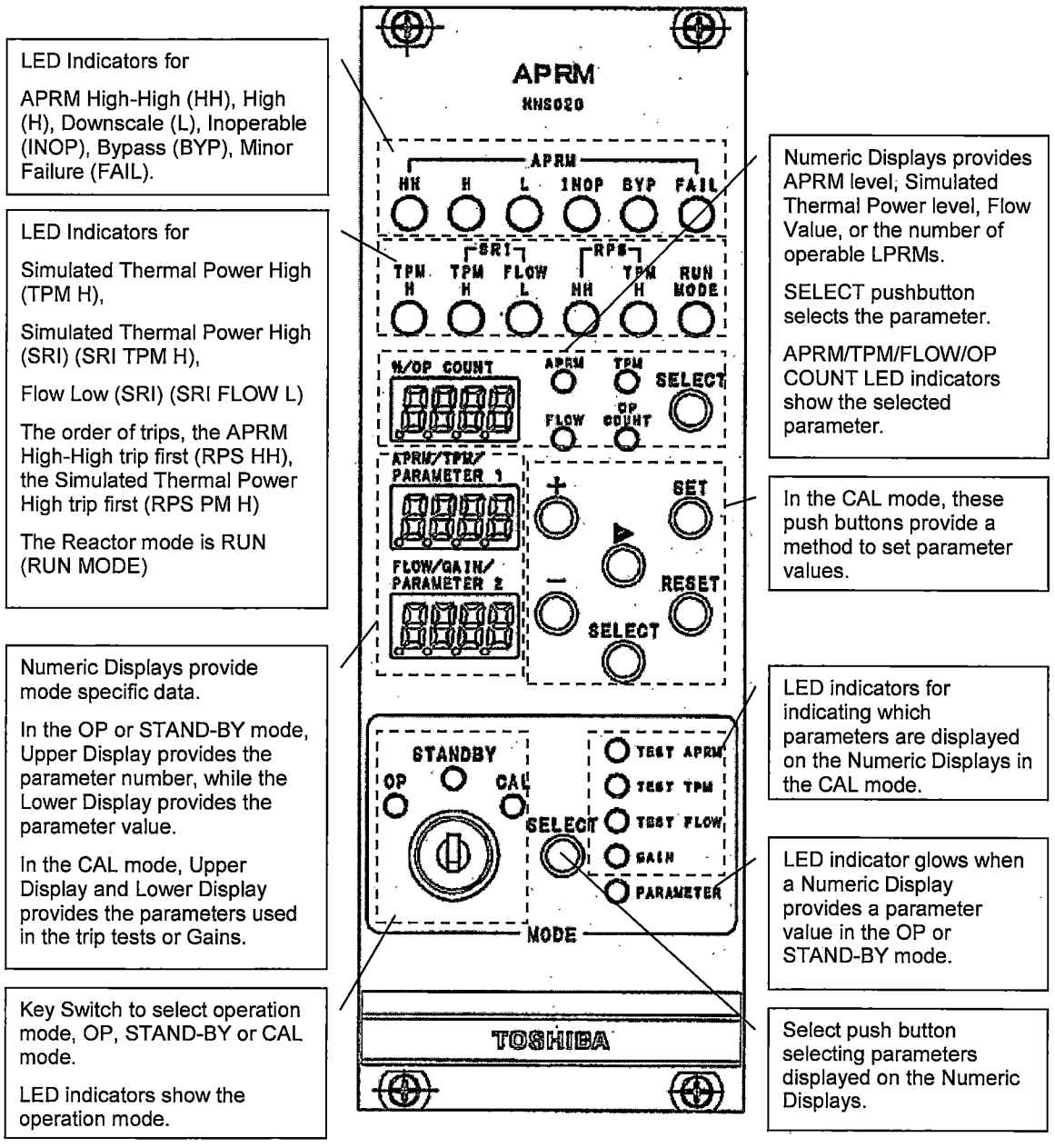

Figure 1 The front panel of the APRM module

3.2.2 Outputs

(1) Output signals via process input and output modules

The APRM provides discrete states and status outputs for APRM High-High trip, APRM High trip, APRM Downscale trip, Simulated Thermal Power High trip, Simulated Thermal Power High (SRI) alarm, Flow Low (SRI) alarm, APRM Inoperable trip, APRM Minor Failure alarm including data transmission line failure alarms, APRM Inoperable trip,. These discrete states and status are transmitted via a DIO module.

The APRM provides analog outputs for APRM level via AO modules.

(2) Output signals via communication modules

In addition, the APRM module includes a fiber optic communication link by TRN module that provides multiplexed APRM data to external equipment, including LPRM data, FLOW data, APRM level, Simulated Thermal Power level, and the trip and alarm signals.

(3) Others to be noted

The APRM module provides communication status signals for( ) a, c

a, c

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the APRM module where each block is an FPGA. Table 1 provides functions of each FPGA.

a, c

Figure 2 Functional Block Diagram of APRM module

Table 1 FPGA functions in the APRM module

FPGA	Description

a, c

3.4 Self Diagnosis

The APRM module generates the following self diagnosis signals.

3.4.1 Minor Failure Alarm

The APRM module generates a minor failure alarm if the
detects an error

a, c
a, c
a, c

3.4.2 Inoperable Trip

An FPGA monitoring watchdog timer generates a inoperable trip if one or more
The watchdog timer is reset by a

a, c
a, c
a, c

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0 Feb.5. 2013	–	First Issue	K.Wakita Feb.5,2013	T.Tarumi Feb.5,2013	H.Ito Feb.5,2013	H.Ito Feb.5,2013
1 Feb.15.2013	1,2 3 3 3 3,4 4	Figure number 3-1 was changed to 1 Inputs and outputs descriptions were revised that "(3) Others to be noted" was added and contents were clarified. Figure number 3-2 was changed to 2. Figure 2 was detailed to clarify. Table number 3-1 was changed to 1. Description on self diagnosis was detailed to clarify.	K.Wakita Feb15,2013	T.Tarumi Feb.15.2013	H.Ito Feb.15.2013	H.Ito Feb.15.2013

SQ-ROOT Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: SQ-ROOT module

(2) Module Number: HNS030

(3) Unit and application to be used

FLOW Unit for BWR-2, 3, 4, 5 and 6 Application

(4) Number of FPGA on the module: Five

2 Functional Summary

The SQ-ROOT module receives a 4-20 mA current loop input from the differential pressure transmitter attached to one of the two recirculation loop, converts the current loop input to a digital value, and calculates a square root of the digital value to obtain a flow value.

3 Module Description

3.1 User Interfaces

Figure 1 shows the front panel of the SQ-ROOT module.

3.2 Inputs and Outputs

The SQ-ROOT module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules

The SQ-ROOT module receives a current loop input of 4-20 mA.

(2) Input signals via communication modules

N/A

3.2.2 Outputs

(1) Output signals via process input and output modules

The SQ-ROOT module provides the raw Flow value and the input current value to the external via AO module.

(2) Output signals via communication modules

N/A

(3) Others to be noted

The SQ-ROOT module provides the raw Flow value and the input current value to the FLOW module in the same FLOW unit through a point-to-point copper serial communication link.

The SQ-ROOT module provides an inoperable trip signal and a minor failure alarm signal to the FLOW module over discrete point-to-point wires through the backplane.

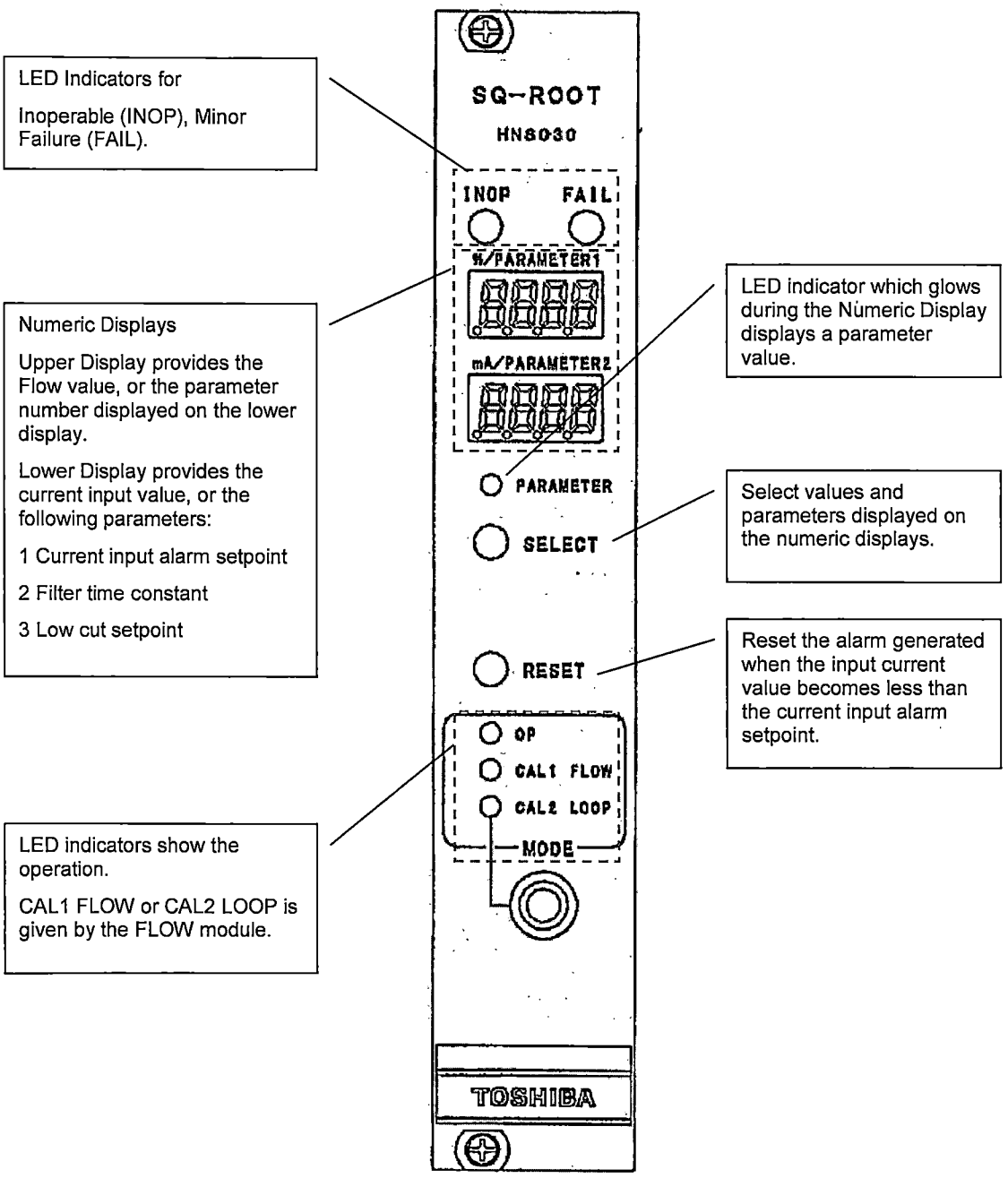

Figure 1 The front panel of the SQ-ROOT module

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the SQ-ROOT module. Table 1 provides functions

of each FPGA.

a,c

Figure 2 Functional Block Diagram of SQ-ROOT module

Table 1 FPGA functions in the SQ-ROOT module

FPGA	Description

a,c

3.4 Self Diagnosis

The SQ-ROOT module generates the following self diagnosis signals.

3.4.1 Minor Failure Alarm

The SQ-ROOT module generates a minor failure alarm if the

a,c

3.4.2 Inoperable Trip

An FPGA monitoring watchdog timer generates a inoperable trip if one or more

a,c

The watchdog timer is reset by a

a,c

a,c

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⓪ Feb.8. 2013	–	First Issue	K.Wakita Feb.8,2013	T.Tatumi Feb.8,2013	H.Ito Feb.8,2013	H.Ito Feb.8,2013
① Feb. 15.2013	1 2 3	Description on inputs was improved. Figure number 3-1 was changed to 1 Figure number 3-2 was changed to 2, and the figure was corrected Table number 3-1 was changed to 1 Descriptions on self diagnosis were improved.	K.Wakita Feb.15, 2013	T.Tatumi Feb.15,2013	H.Ito Feb.15.2013	H.Ito Feb.15.2013

FLOW Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: FLOW module

(2) Module Number: HNS040

(3) Unit and application to be used

FLOW Unit for BWR-2, 3, 4, 5 and 6 Application

(4) Number of FPGA on the module: Four

2 Functional Summary

The FLOW module receives two raw Flow values from the SQ-ROOT module mounted in the same FLOW unit, and calculates a normalized Flow value by taking a sum of the two raw Flow values, and applying a gain value.

3 Module Description

3.1 User Interfaces

Figure 1 shows the front panel of the FLOW module.

3.2 Inputs and Outputs

The FLOW module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules

N/A

(2) Input signals via communication modules

N/A

(3) Others to be noted

The FLOW module receives raw Flow values from the two SQ-ROOT modules with the alarms for the SQ-ROOT modules through point-to-point copper serial communication links. Each SQ-ROOT measures the raw Flow value in each of two recirculation loops.

The FLOW module receives the FLOW Bypass state from the bypass switch via the DIO module.

3.2.2 Outputs

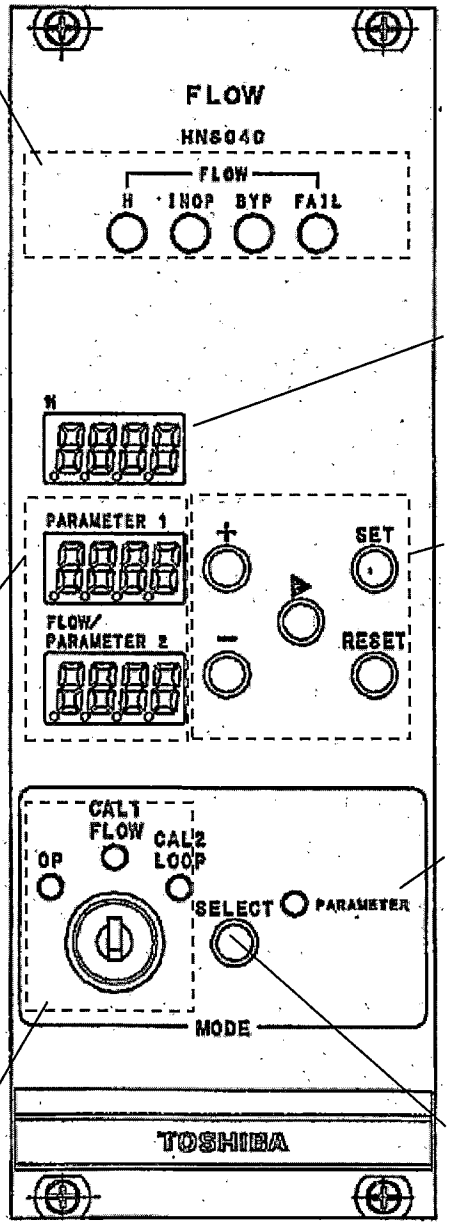
(1) Output signals via process input and output modules

The FLOW module provides trip signals to external equipment via DIO module.

The FLOW module provides the Flow values to external equipment via AO module.

(2) Output signals via communication modules

The FLOW module provides the Flow values and alarms to external equipment, including the LPRM/APRM unit via TRN module.



LED Indicators for

FLOW High (H), Inoperable (INOP), Bypass (BYP), Minor Failure (FAIL).

Numeric Displays provides Flow value.

Numeric Displays provide mode specific data.

In the OP mode, Upper Display provides the parameter number, the Lower Display provides the parameter value.

In the CAL 1 FLOW mode, Upper Display is turned off, Lower Display provides trip test parameter value.

In the CAL 2 LOOP mode, the displays are turned off.

In the CAL 1 FLOW mode, these push buttons provide a method to set parameter value.

LED indicator which glows during the Numeric Displays displays a parameter value in the OP mode.

Key Switch to select operation mode, OP, CAL 1 FLOW or CAL 2 LOOP mode.

LED indicators shows the operation mode.

Select push button selecting parameters displayed on the Numeric Displays.

Figure 1 The front panel of the FLOW module

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the FLOW module where each block shows an FPGA. Table 1 provides functions of each FPGA.

a,c

Figure 2 Functional Block Diagram of FLOW module

Table 1 FPGA functions in the FLOW module

a,c

FPGA	Description

3.4 Self Diagnosis

The FLOW module generates the following self diagnosis signals.

3.4.1 Minor Failure Alarm

The FLOW module generates a minor failure alarm if one of the following occurs:

- An error in periodic receptions of the Flow values from the SQ-ROOT modules
- A minor failure alarm from the SQ-ROOT modules
- Halt of the [ ]a,c FPGA.

3.4.2 Inoperable Trip

An FPGA monitoring watchdog timer generates a inoperable trip if one or more [ ]a,c The watchdog timer is reset by a [ ]a,c
[ ]a,c

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0 Feb.8, 2013	—	First Issue	K.Wakita Feb.8,2013	T.Tarumi Feb.8,2013	H.Ito Feb.8,2013	H.Ito Feb.8,2013
1 Feb. 15 2013	1 3 4	Descriptions in Section 2 and 3 were improved adding information on communication Figure number was changed from 3-1 to 1 Figure number was changed from 3-2 to 2 Table number was changed from 3-1 to 1 Description of self diagnosis was improved.	K.Wakita Feb 15 2013	T.Tarumi Feb. 15, 2013	H. Ito Feb. 15. 2013	H. Ito Feb. 15. 2013

STATUS Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: STATUS module

(2) Module Number: HNS091

(3) Unit and application to be used

LPRM/APRM Unit for BWR-2, 3, 4, 5 and 6 Application

(4) Number of FPGA on the module: One

2 Functional Summary

The STATUS module receives discrete alarm signals from the LVPS and APRM modules in the same unit, and shows the alarm on the module front panel.

3 Module Description

3.1 Module Front Panel

Figure 1 shows the front panel of the STATUS module.

3.2 Inputs and Outputs

The STATUS module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules

N/A

(2) Input signals via communication modules

N/A

(3) Others to be noted

The STATUS module receives discrete alarm signals from the APRM module and the LVPS modules through the backplane.

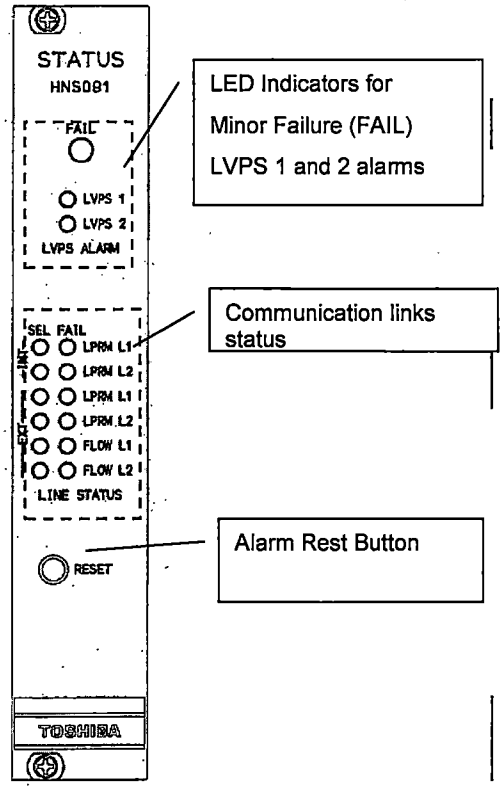

Figure 1 The front panel of the STATUS module

3.2.2 Outputs

(1) Output signals via process input and output modules

The STATUS module provides a minor failure alarm signal through the DIO module.

(2) Output signals via communication modules

N/A

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the STATUS module. Table 1 provides functions of each FPGA.

a,c

Figure 2 Functional Block Diagram of STATUS module

Table 1 FPGA functions in the STATUS module

a,c

FPGA	Description

3.4 Self Diagnosis

3.4.1 Minor Failure Alarm

The STATUS module generates a minor failure alarm if the [ ]a,c FPGA halts, and glows FAIL LED.

3.4.2 Inoperable Trip

N/A

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0 Feb.8. 2013	–	First Issue	K.Wakita Feb.8,2013	T.Tarumi Feb.8,2013	H.Ito Feb.8,2013	H.Ito Feb.8,2013
1 Feb. 15, 2013	1 2 3	Descriptions in Section 2 and 3 were improved. Figure number was changed from 3-1 to 1 Figure number was changed from 3-2 to 2 Table number was changed from 3-1 to 1 Descriptions of self diagnosis were corrected.	K Wakita Feb.15, 2013	T. Tarumi Feb. 15, 2013	H. Ito Feb. 15, 2013	H. Ito Feb. 15, 2013

STATUS Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: STATUS module

(2) Module Number: HNS093

(3) Unit and application to be used

LPRM and FLOW Units for BWR-2, 3, 4, 5 and 6 Application

(4) Number of FPGA on the module: One

2 Functional Summary

The STATUS module receives discrete alarm signals from the LVPS modules in the same unit, and shows the alarm on the module front panel.

3 Module Description

3.1 Module Front Panel

Figure 1 shows the front panel of the STATUS module.

3.2 Inputs and Outputs

The STATUS module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules

N/A

(2) Input signals via communication modules

N/A

(3) Others to be noted

The STATUS module receives discrete alarm signals from the LVPS modules through the backplane.

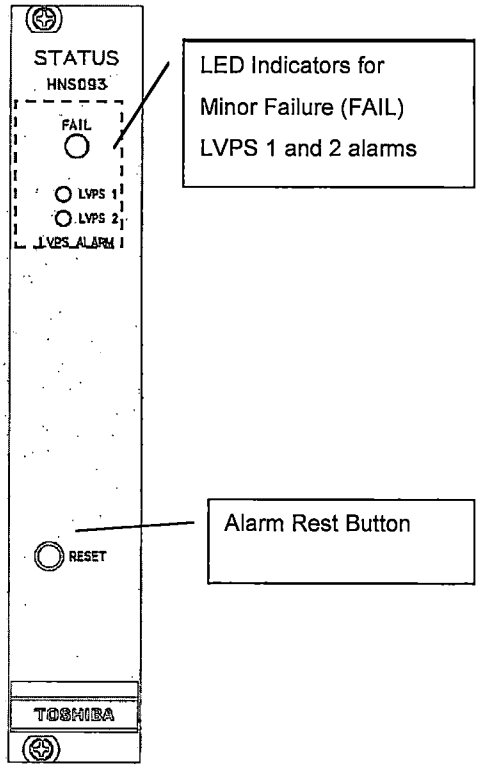

Figure 1 The front panel of the STATUS module

3.2.2 Outputs

(1) Output signals via process input and output modules

The STATUS module provides a minor failure alarm signal through the DIO module.

(2) Output signals via communication modules

N/A

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the STATUS module. Table 1 provides functions of each FPGA.

a,c

Figure 2 Functional Block Diagram of STATUS module

Table 1 FPGA functions in the STATUS module

a,c

FPGA	Description

3.4 Self Diagnosis

3.4.1 Minor Failure Alarm

The STATUS module generates a minor failure alarm if the a,c FPGA halts, and glows FAIL LED.

3.4.2 Inoperable Trip

N/A

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⓪ Feb.8. 2013	–	First Issue	K.Wakita Feb.8,2013	T.Tarumi Feb.8,2013	H.Ito Feb.8,2013	H.Ito Feb.8,2013
① Feb. 15.2013	1 2 3	Descriptions in Section 2 and 3 were improved. Figure number was changed from 3-1 to 1 Figure number was changed from 3-2 to 2 Table number was changed from 3-1 to 1 Descriptions of self dingnosis were corrected.	K.Wakita Feb.15, 2013	T.Tarumi Feb.15,2013	H.Ito Feb.15.2013	H.Ito Feb. 15.2013

TRN Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: TRN module

(2) Module Number: HNS0531

(3) Unit and application to be used

LPRM/APRM, LPRM, FLOW, SRNM Units for BWR-2, 3, 4, 5 and 6 Application

OPRM, LPRM, APRM, SRNM, DTF-RPS, DTF-MSIV, DTF-MSIV-S, TLF-RPS, TLF-MSIV, SPTM, SPTM-S Units for ABWR Application

(4) Number of FPGA on the module: Six

2 Functional Summary

The TRN module has two data processing trains that collect data from other modules mounted in the same unit, generate a data frame in a fixed format by multiplexing the collected data, and transmit the data frame to external over fiber optic links and to other modules in the same unit. When installed in the LPRM/APRM unit, the TRN module receives the data frame from the APRM module in the same unit, and transmits the data frame over fiber optic links instead of the data frame generated in the TRN module.

3 Module Description

3.1 Module Front Panel

Figure 1 shows the front panel of the TRN module.

3.2 Inputs and Outputs

The TRN module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules

N/A

(2) Input signals via communication modules

N/A

(3) Others to be noted

The TRN module has two data processing trains A and B receiving the same inputs data through point-to-point serial communication links in the backplane. The TRN module has the following two data collecting functions:

(a) Collect individual digital data from modules. Up to 16 digital data are collected. The digital data typically come from modules equipped with an analog-to-digital converter, such as the LPRM or SQ-ROOT module.

(b) Receive data frames from a module transmitting more than one data, such as the APRM module. The data frame is in a fixed data format, multiplexing 46 data items of 16 bits long.

3.2.2 Outputs

(1) Output signals via process input and output modules

N/A

(2) Outputs via communication modules

Each data processing train transmits data frames containing collected data items through two identical optical transmitters. Note that the TRN module installs no hand shaking method with the receiver.

(3)Others to be noted

Each data processing train transmits data frames containing the data collected using function (a) in Section 3.2.1described above to other modules through the backplane.

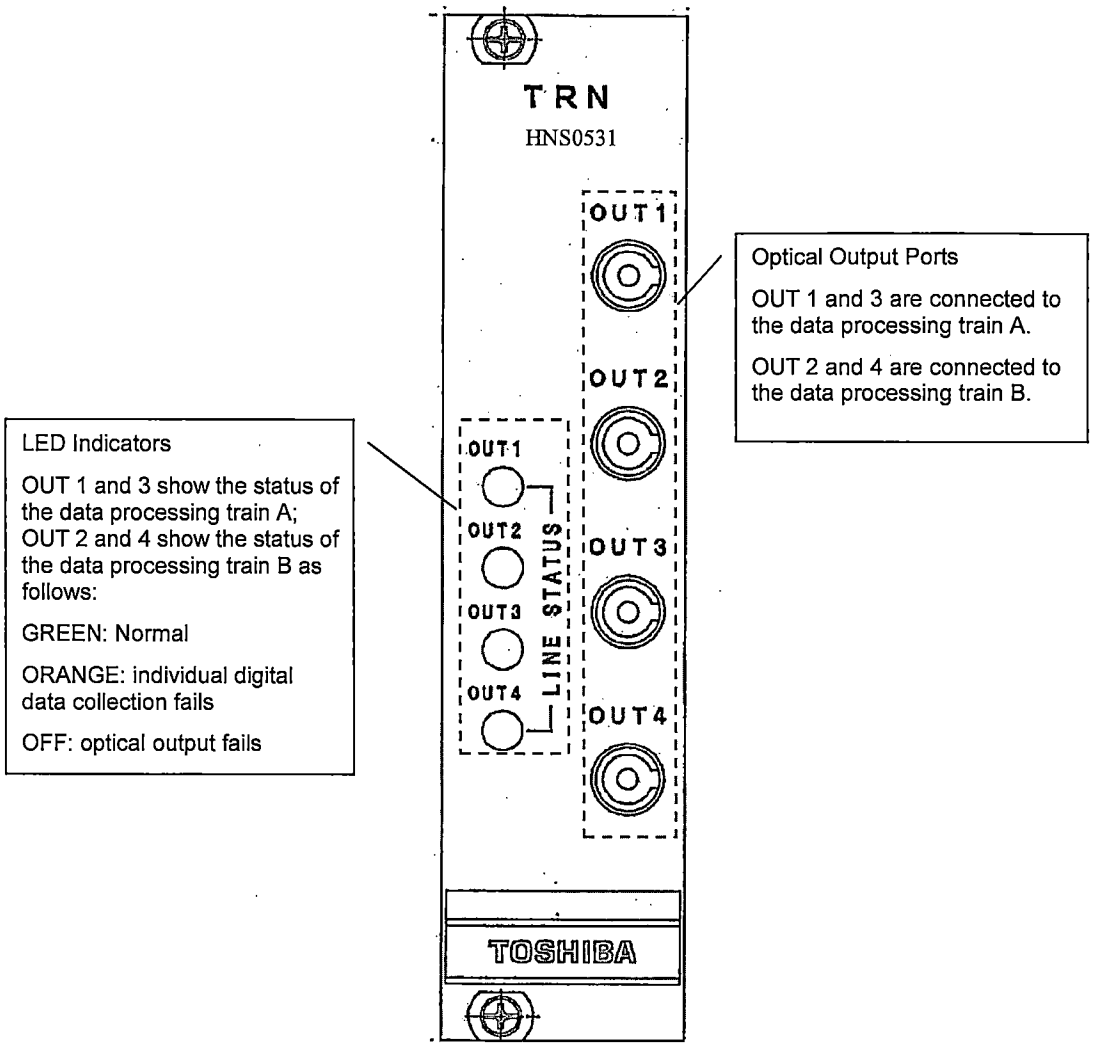

Figure 1 The front panel of the TRN module

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the TRN module. Table 1 provides functions of each FPGA.


a,c

Figure 2 Functional Block Diagram of TRN module

Table 1 FPGA functions in the TRN module

FPGA	Description

a,c

3.4 Self Diagnosis

Watchdog timers in each data processing trains monitors operation of FPGAs. The TRN module shows the results of the monitoring on the front panel.

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0 Feb.13, 2013	–	First Issue	K.Wakita Feb.13,2013	T.Tatumi Feb.13,2013	H.Ito Feb.13,2013	H.Ito Feb.13,2013
1 Feb.15, 2013	1 3	Descriptions on communication were improved. Figure number was changed from 3-1 to 1. Figure number was changed from 3-2 to 2. Table number was changed from 3-1 to 1.	K.Wakita Feb.15, 2013	T.Tatumi Feb.15,2013	H.Ito Feb.15, 2013	H.Ito Feb.15,2013

RCV Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: RCV module

(2) Module Number: HNS0541

(3) Unit and application to be used

LPRM, LPRM/APRM Unit for BWR-2, 3, 4, 5 and 6 Application

OPRM, LPRM, APRM, DTF-RPS, DTF-MSIV, TLF-RPS, TLF-MSIV, SPTM for ABWR Application

(4) Number of FPGA on the module: Eight

2 Functional Summary

The RCV module has four independent data processing trains that receive optical signals containing a fixed format data frame from external, and transmits the data frame to other modules mounted in the same unit through point-to-point serial communication links.

3 Module Description

3.1 Module Front Panel

Figure 1 shows the front panel of the RCV module.

3.2 Inputs and Outputs

The RCV module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules

N/A

(2) Input signals via communication modules

Four optical input ports.

3.2.2 Outputs

(1) Output signals via process input and output modules

N/A

(2) Outputs via communication modules

N/A

(3) Others to be noted

Each data processing train transmits the data frame to other modules mounted in the same unit through point-to-point serial communication links in the backplane.

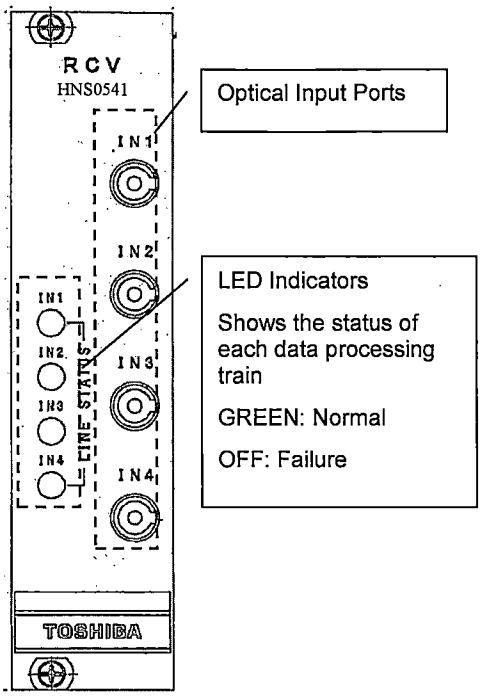

Figure 1 The front panel of the RCV module

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the RCV module. Table 1 provides functions of each FPGA.

a,c

Figure 2 Functional Block Diagram of RCV module

Table 1 FPGA functions in the RCV module

FPGA	Description

a,c

3.4 Self Diagnosis

Each data processing train has a separate watchdog timer that monitors operation of the FPGAs. FPGAs in the RCV module perform the checks described in Table 1, and if an error occurs indicates on the front panel LEDs.

a,c

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1 Feb.15.2013	1 2 3	Descriptions on communication were improved. Figure number was changed from 3-1 to 1. Figure number was changed from 3-2 to 2. Table number was changed from 3-1 to 1. Description on self diagnosis was improved.	K.Wakita Feb.15.2013	T.Tarumi Feb.15,2013	H.Ito Feb.15.2013	H.Ito Feb.15.2013

LVPS Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: LVPS module

(2) Module Number: HNS500

(3) Unit and application to be used

LPRM/APRM, LPRM, FLOW, OPRM, SRNM Units for BWR-2, 3, 4, 5 and 6 Application

LPRM, APRM, OPRM, SRNM, DTF-RPS, DTF-MSIV, DTF-MSIV-S, TLF-RPS, TLF-MSIV, SPTM, SPTM-S Units for ABWR Application

(4) Number of FPGA on the module: None

2 Functional Summary

The LVPS module is a plug-in type direct current (DC) power supply mounted in a unit and supplies DC power to other modules in the same unit through the backplane. Toshiba FPGA-based unit mount two redundant LVPSs, and either alone provide sufficient power to operate the unit. The LVPS module monitors the output voltage inside the power supply, and generates an alarm signal in case of failure.

3 Module Description

3.1 Module Front Panel

Figure 1 shows the front panel of the LVPS module.

3.2 Inputs and Outputs

The LVPS module has the following inputs and outputs.

3.2.1 Inputs

N/A

3.2.2 Outputs

The LVPS module provides a discrete alarm signal to the module which has a function of status indicator in the same unit through the backplane.

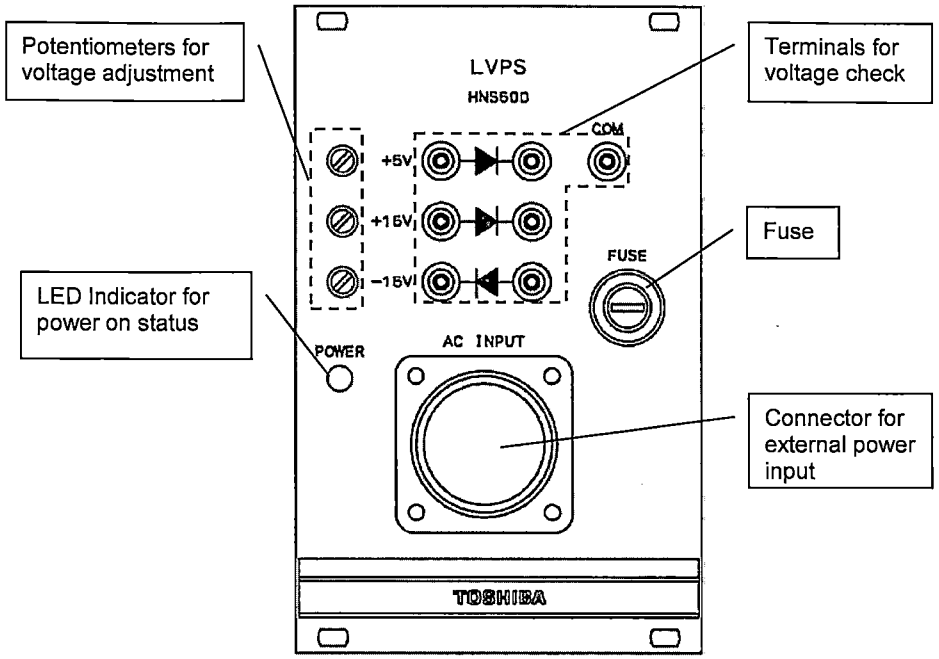

Figure 1 The front panel of the LVPS module

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0 Feb.8, 2013	-	First Issue	K.Wakita Feb.8,2013	T.Tarumi Feb.8,2013	H.Ito Feb.8,2013	H.Ito Feb.8,2013
1 Feb. 15, 2013	1	Improve description in Section 2 and 3. Figure number was changed from 3-1 to 1	K.Wakita Feb.15.2013	T.Tarumi Feb.15,2013	H.Ito Feb.15,2013	H.Ito Feb. 15, 2013

AO Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: AO module

(2) Module Numbers: HNS515, HNS516, HNS517, HNS518

(3) Unit and application to be used

LPRM/APRM, LPRM, FLOW, SRNM Units for BWR-2, 3, 4, 5 and 6 Application

LPRM, APRM, SRNM, SPTM Units for ABWR Application

(4) Number of FPGA on the module: None

2 Functional Summary

The AO module provides sixteen 12-bit analog outputs to external equipment. The AO module receives individual digital values from other modules in the same unit through point-to-point copper serial communication links on the backplane. The AO module converts each output's digital data into an analog output value. The model number specifies the output signal voltage range for all of the digital-to-analog converters.

3 Module Description

3.1 Module Front Panel

Figure 1 shows the front panel of the AO module.

3.2 Inputs and Outputs

The AO module has the following inputs and outputs.

3.2.1 Inputs

Sixteen serial digital data values, over sixteen individual copper communication paths.

3.2.2 Outputs

Sixteen single ended analog voltage output ports of the following voltage ranges. An isolated DC/DC converter provides power to the output ports.

HNS515: 1 to 5 V
HNS516: 0 to 1 V
HNS517: 0 to 5 V
HNS518: 0 to 160 mV

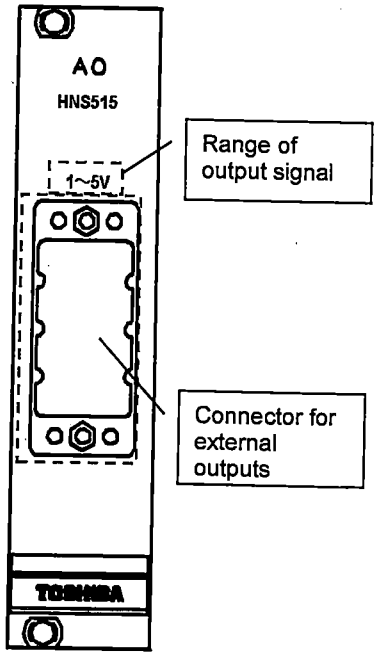

Figure 1 The front panel of the AO module (HNS515)

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⓪ Feb.8, 2013	–	First Issue	K.Wakita Feb.8,2013	T.Tarumi Feb.8,2013	H.Ito Feb.8,2013	H.Ito Feb.8,2013
① Feb. 15, 2013	1	Descriptions in Section 2 and 3 were improved. Added information on the communication.	K.Wakita Feb.15, 2013	T. Tarumi Feb. 15, 2013	H. Ito Feb. 15, 2013	H. Ito Feb. 15, 2013

DIO Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: DIO module

(2) Module Number: HNS520

(3) Unit and application to be used

LPRM/APRM, LPRM, FLOW, SRNM Units for BWR-2, 3, 4, 5 and 6 Application

LPRM, APRM, OPRM, SRNM Units for ABWR Application

(4) Number of FPGA on the module: None

2 Functional Summary

The DIO module provides for sampling four discrete inputs from external equipment, and 16 discrete outputs to external equipment. The received signals are sent to other modules in the same unit. The output signals are provided from other modules in the same unit. The inputs and outputs are provided to the DIO module through the backplane (which Toshiba refers to as a middle plane) on copper point-to-point discrete wiring.

3 Module Description

3.1 Module Front Panel

Figure 1 shows the front panel of the DIO module.

3.2 Inputs and Outputs

The DIO module has the following inputs and outputs.

3.2.1 Inputs

Four discrete 24 VDC input points. All signals share a common ground. The external voltage source is isolated from the backplane through photo couplers.

3.2.2 Outputs

Sixteen discrete contact output points. The sixteen points are grouped in four. Output points in each group share a common ground. Each output point is isolated from the backplane through a photo coupler.

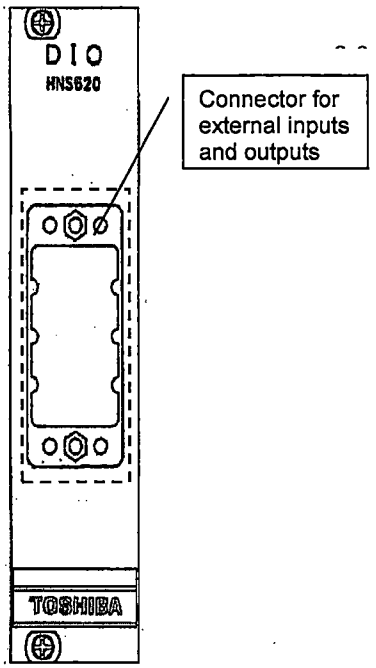

Figure 1 The front panel of the DIO module

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⓪ Feb.5, 2013	–	First Issue	K.Wakita Feb.5,2013	T.Tarumi Feb.5,2013	H.Ito Feb.5,2013	H.Ito Feb.5,2013
① Feb.15,2013	1	Descriptions in Section 2 and 3 were improved Figure number was changed from 3-1 to 1.	K.Wakita Feb.15,2013	T.Tarumi Feb.15,2013	H.Ito Feb.15,2013	H.Ito Feb.15,2013

BLANK Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: BLANK module

(2) Module Number: HNS490

(3) Unit and application to be used
LPRM/APRM, LPRM Units for BWR-2, 3, 4, 5 and 6 Application

(4) Number of FPGA on the module: None

2 Functional Summary

The BLANK module fills a unit slot instead of an LPRM module. The BLANK module bypasses alarm signal lines that take OR (logical disjunction) of each LPRM module alarm.

3 Module Description

3.1 Module Front Panel

Figure 1 shows the front panel of the BLANK module.

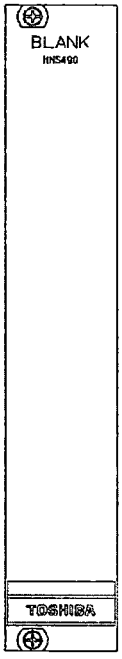

Figure 1 The front panel of the BLANK module

3.2 Inputs and Outputs

The BLANK module has the following inputs and outputs through the backplane.

3.2.1 Inputs

Three types of daisy chain signals (LPRM High, LPRM Downscale, LPRM inoperable) for alarm detection from one neighboring LPRM module.

3.2.2 Outputs

The BLANK module provides the three types of daisy chain signals to the other neighboring LPRM module. A DIO module accepts the signals at the end.

One dummy LPRM inoperable signal to the TRN module.

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⓪ Feb.8. 2013	–	First Issue	K.Wakita Feb.8,2013	T.Tarumi Feb.8,2013	H.Ito Feb.8,2013	H.Ito Feb.8,2013
① Feb. 15.2013	1	Figure number 3-1 was changed to 1.	K.Wakita Feb. 15. 2013	T.Tarumi Feb. 15, 2013	H. Ito Feb. 15. 2013	H. Ito Feb. 15. 2013

CELL Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: CELL module

(2) Module Number: HNS0400

(3) Unit and application to be used

OPRM Unit for ABWR Application

(4) Number of FPGA on the module: Eleven

2 Functional Summary

The CELL module converts LPRM levels to normalized oscillation levels, and provides the data to AGRD and PBD module for trip determinations.

3 Module Description

3.1 User Interfaces

Figure 1 shows the front panel of the CELL module.

3.2 Inputs and Outputs

The CELL module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules

N/A

(2) Input signals via communication modules

The CELL module uses the LPRM levels and status from individual LPRM modules. The TRN module in the LPRM unit that is not shown in the Figure 2 transmits the LPRM data to OPRM unit. The RCV module in the OPRM unit receives the LPRM data. The [redacted]a,c FPGA in the CELL module is responsible for receiving the LPRM data from the RCV module.

The CELL module receives APRM/FLOW levels and status from APRM unit. The TRN module in the APRM unit that is not shown in the figure transmits the APRM/FLOW data to OPRM unit. The RCV module in the OPRM unit receives the APRM/FLOW data. The [redacted]a,c FPGA in the CELL module is responsible for receiving the APRM/FLOW data from the RCV module.

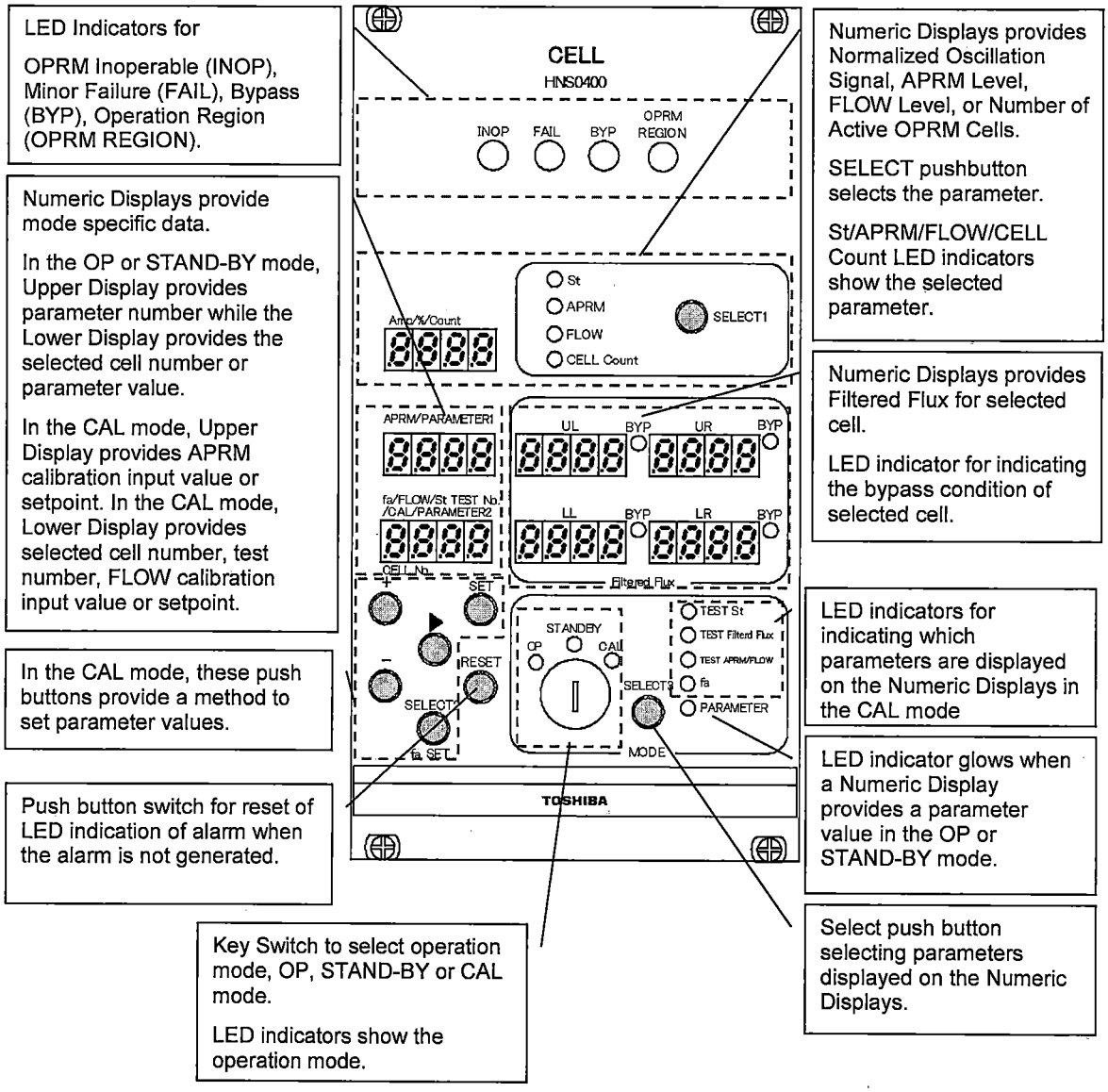

Figure 1 The front panel of the CELL module

3.2.2 Outputs

(1) Output signals via process input and output modules

N/A

(2) Output signals via communication modules

The CELL module provides the data including the discrete alarm signal to the DAT/ST module and DAT/ST module provides the data to external equipment via TRN module.

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the CELL module where each block is an FPGA. Table 1 provides functions of each FPGA.

a,c

Figure 2 Functional Block Diagram of CELL module

Table 1 FPGA functions in the CELL module

a,c

FPGA	Description

[ ]a,c

3.4 Self Diagnosis

The CELL module generates the following self diagnosis signals.

3.4.1 Minor Failure Alarm

The CELL module generates a minor failure alarm if the[ ]a,c [ ]a,c The FPGA[ ]a,c is detected by Watchdog Timer (WDT) and determined as error if the[ ]a,c is not detected.

3.4.2 Inoperable Trip

The CELL module generates an Inoperable trip if the[ ]a,c [ ]a,c The FPGA[ ]a,c is detected by WDT and determined as error if the[ ]a,c is not detected.

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⓪ Feb 25,2013	–	First Issue	K. Wakita Feb 25,2013	T. Tarumi Feb 25,2013	H. Ito Feb 25,2013	H. Ito Feb 25,2013
① Mar. 11, 2013	1	Editorial error correction.	K. Wakita Mar. 11, 2013	T. Tarumi Mar. 11, 2013	H. Ito Mar. 11, 2013	H. Ito Mar. 11, 2013

DAT/ST Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: DAT/ST module

(2) Module Number: HNS0410

(3) Unit and application to be used
OPRM Unit for ABWR Application

(4) Number of FPGA on the module: Two

2 Functional Summary

The DAT/ST module receives data from CELL module, AGRD module, PBD module and LVPS module, multiplexes these data, and outputs them to the TRN module.

The DAT/ST module also displays input and power status on the front panel.

3 Module Description

3.1 User Interfaces

Figure 1 shows the front panel of the DAT/ST module.

3.2 Inputs and Outputs

The DAT/ST module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules

N/A

(2) Input signals via communication modules

N/A

(3) Others to be noted

The DAT/ST module receives data from CELL module, AGRD module, PBD module, and LVPS module on the same chassis.

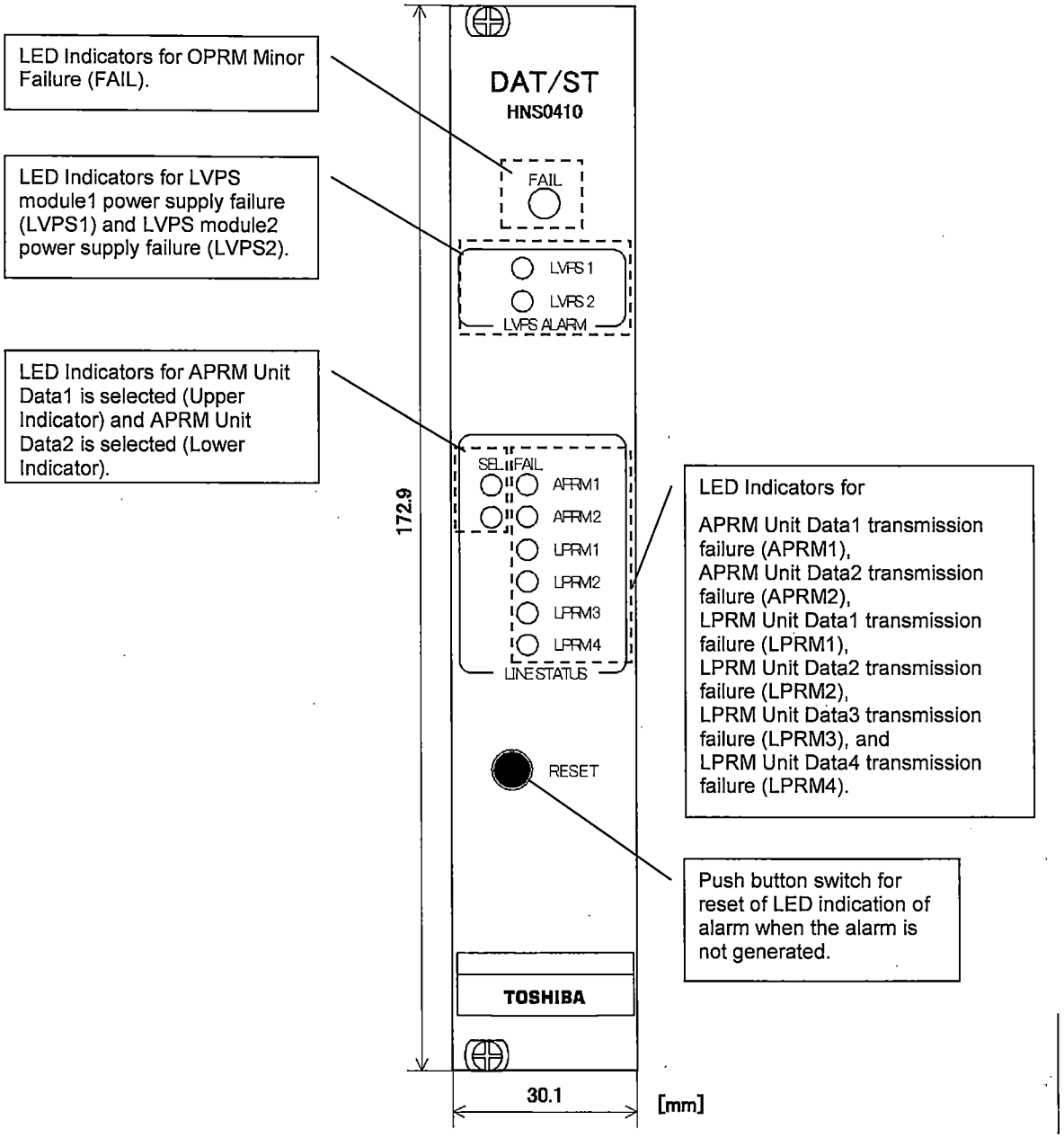

Figure 1 The front panel of the DAT/ST module

3.2.2 Outputs

(1) Output signals via process input and output modules

N/A

(2) Output signals via communication modules

The DAT/ST module provides received data from CELL module, AGRD module, PBD module and LVPS module to external via TRN module.

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the DAT/ST module where each block is an FPGA. Table 1 provides functions of each FPGA.

a,c

Figure 2 Functional Block Diagram of DAT/ST module

Table 1 FPGA functions in the DAT/ST module

FPGA	Description

a,c

3.4 Self Diagnosis

The DAT/ST module generates the following self diagnosis signals.

3.4.1 Minor Failure Alarm

The DAT/ST module generates a minor failure alarm if the [ ]a,c
The FPGA [ ]a,c is detected by Watchdog Timer (WDT) and determined as error if the [ ]a,c is not detected.

3.4.2 Inoperable Trip

N/A

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⓪ Feb 25,2013	–	First Issue	K. Wakita Feb 25,2013	T. Tarumi Feb 25,2013	H. Ito Feb 25,2013	H. Ito Feb 25,2013
① Mar. 11, 2013	1,2	Editorial error correction	K. Wakita Mar 11, 2013	T. Tarumi Mar. 11, 2013	H. Ito Mar. 11, 2013	H. Ito Mar. 11, 2013

AGRD Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: AGRD module

(2) Module Number: HNS0420

(3) Unit and application to be used

OPRM Unit for ABWR Application

(4) Number of FPGA on the module: Eight

2 Functional Summary

The AGRD module receives OPRM cell data from the CELL module, monitors power oscillation for each cell using the Amplitude-Based Algorithm (ABA) and Growth Rate-based detection Algorithm (GRA). When the power oscillation is detected by ABA or GRA, the AGRD module generates a trip signal to DIO module. The AGRD module transmits AGRD calculation data to the DAT/ST module.

3 Module Description

3.1 User Interfaces

Figure 1 shows the front panel of the AGRD module.

3.2 Inputs and Outputs

The AGRD module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules

N/A

(2) Input signals via communication modules

N/A

(3) Others to be noted

The AGRD module receives OPRM cell data from the CELL module.

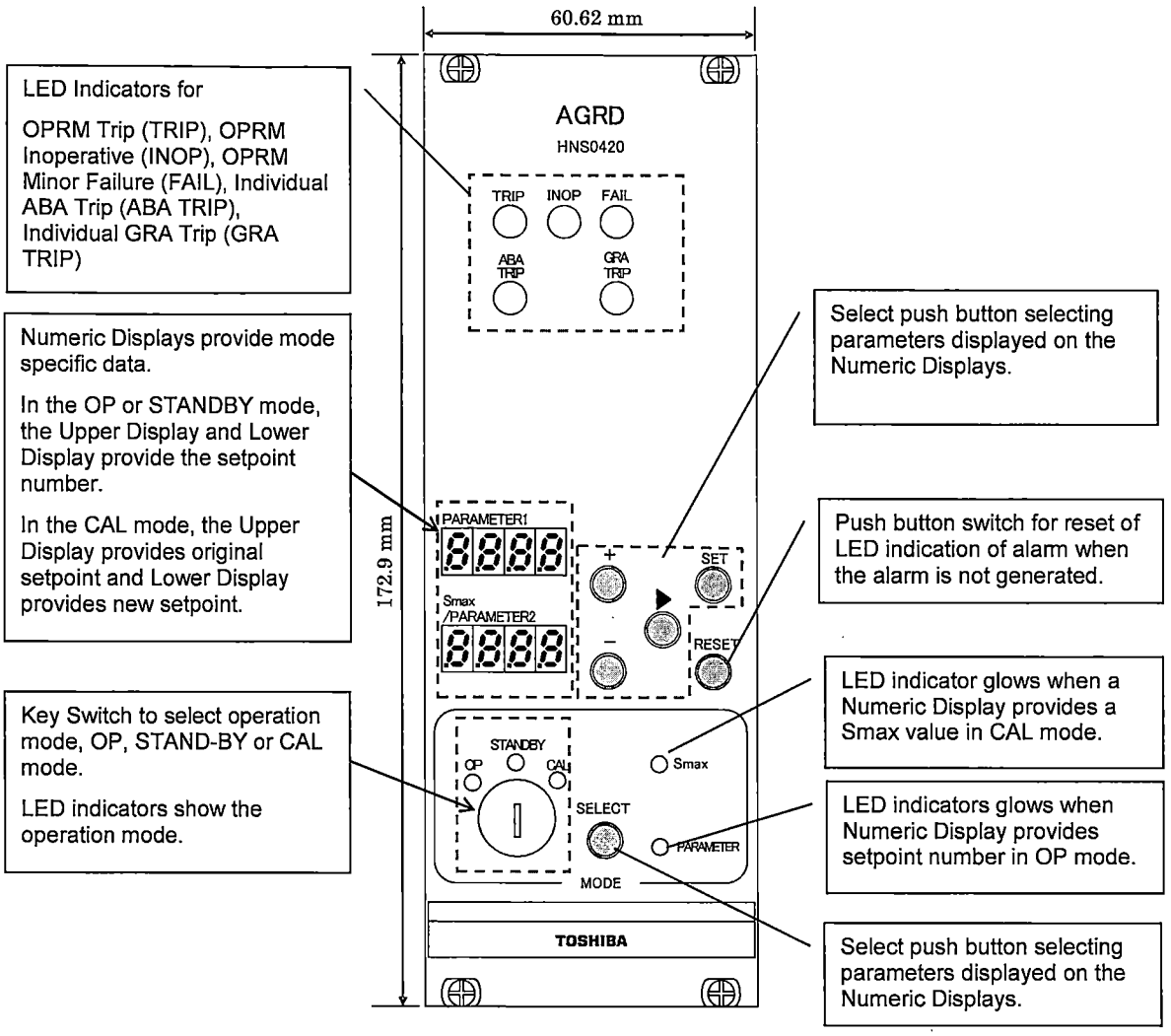

Figure 1 The front panel of the AGRD module

3.2.2 Outputs

(1) Output signals via process input and output modules

When the power oscillation is detected by ABA or GRA, the AGRD module generates a trip signal to DIO module.

(2) Output signals via communication modules

The AGRD module transmits AGRD calculation data to the DAT/ST module.

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the AGRD module where each block is an FPGA. Table 1 provides functions of each FPGA.

a,c

Figure2 Functional Block Diagram of AGRD module

Table1 FPGA functions in the AGRD module

a,c

FPGA	Description

[ ]a,c

3.4 Self Diagnosis

The AGRD module generates the following self diagnosis signals.

3.4.1 Minor Failure Alarm

The AGRD module generates a minor failure alarm if the EEPROM data error or the[ ]a,c [ ]a,c is detected. The [ ]a,c [ ]a,c is detected by Watchdog Timer (WDT) and determined as error if the [ ]a,c [ ]a,c is not detected.

3.4.2 Inoperable Trip

The AGRD module generates an inoperable trip if[ ]a,c [ ]a,c is detected. The [ ]a,c is detected by WDT and determined as error if the [ ]a,c is not detected.

変更記録 REVISIONS						
変更記号 REV.MARK 変更発行日 REV.ISSUED	ページ PAGE	変更箇所・変更内容 CHANGED PLACE AND CONTENTS	承認 APPROVED BY	調査 REVIEWED BY	担当 PREPARED BY	保管 REGISTERED
⓪ Feb 25,2013	–	First Issue	K. Wakita Feb 25,2013	T. Tarumi Feb 25,2013	H. Ito Feb 25,2013	H. Ito Feb 25,2013
① Mar. 11. 2013	1,3	Editorial error correction.	K. Wakita Mar 11. 2013	T. Tarumi Mar. 11, 2013	H. Ito Mar. 11. 2013	H. Ito Mar. 11. 2013

PBD Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: PBD module

(2) Module Number: HNS0430

(3) Unit and application to be used

OPRM Unit for ABWR Application

(4) Number of FPGA on the module: Seven

2 Functional Summary

The PBD module receives OPRM cell data from the CELL module, monitors power oscillation for each cell using the Period-Based Detection Algorithm (PBDA). When the power oscillation is detected by PBDA, the PBD module generates a trip signal to DIO module. The PBD module transmits PBDA calculation data to the DAT/ST module.

3 Module Description

3.1 User Interfaces

Figure 1 shows the front panel of the PBD module.

3.2 Inputs and Outputs

The PBD module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules

N/A

(2) Input signals via communication modules

N/A

(3) Others to be noted

The PBD module receives OPRM cell data from the CELL module.

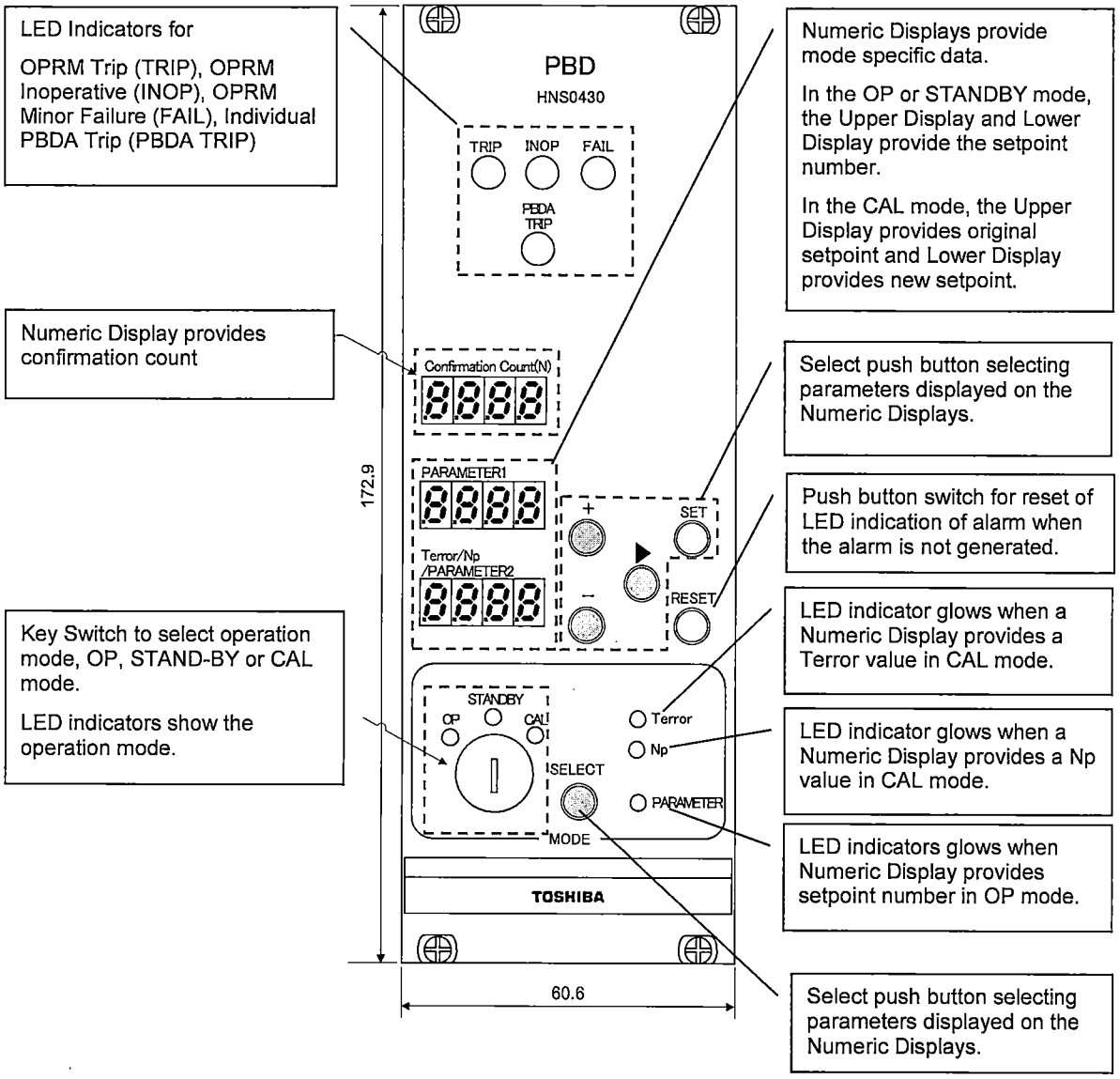

Figure 1 The front panel of the AGRD module

3.2.2 Outputs

(1) Output signals via process input and output modules

When the power oscillation is detected by PBDA, the PBD module generates a trip signal to DIO module.

(2) Output signals via communication modules

The PBD module transmits PBD calculation data to the DAT/ST module.

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the PBD module where each block is an FPGA. Table 1 provides functions of each FPGA.

a,c

Figure 2 Functional Block Diagram of PBD module

Table 1 FPGA functions in the PBD module

a,c

FPGA	Description

3.4 Self Diagnosis

The PBD module generates the following self diagnosis signals.

3.4.1 Minor Failure Alarm

The PBD module generates a minor failure alarm if the EEPROM data error or the [redacted] is detected. The [redacted] is detected by Watchdog Timer (WDT) and determined as error if the [redacted] is not detected.

3.4.2 Inoperable Trip

The PBD module generates an inoperable trip if [redacted] stop is detected. The [redacted] is detected by WDT and determined as error if the [redacted] is not detected.

変 更 記 録 REVISIONS						
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(0) Feb 25,2013	–	First Issue	K. Wakita Feb 25,2013	T. Tarumi Feb 25,2013	H. Ito Feb 25,2013	H. Ito Feb 25,2013
(1) Mar. 11. 2013	1	Editorial error correction.	K. Wakita Mar. 11. 2013	T. Tarumi Mar. 11, 2013	H. Ito Mar. 11. 2013	H. Ito Mar. 11. 2013