Validyne
ENGINEERING CORPORATION

REVISIONS				
LTR	ECO	DESCRIPTION	DATE	APPROVED
A		See DCN	3/23/81	
B		See DCN	4/17/81	

8411200441 841105
PDR ADOCK 05000280
F PDR

SIGNATURE		DATE
PROD TEST		3/18/81
ENGINEERING		3/18/81
QUAL CONTROL		3/19/81

TITLE: CD173-Q2 High-Gain Carrier Demodulator

NUMBER: ATP443 REV: B

SHEET 1 OF 12

8626 WILBUR AVENUE • NORTHRIDGE, CA 91324 • (213) 886-8488 • Telex No. 65-1303

1.0 SCOPE

This document defines the Acceptance Test Procedure (ATP) for the CD173-Q2 High-Gain Carrier Demodulator. The ATP performs functional tests of all operating characteristics. A sample of the Test Report to be used with this ATP is contained in Appendix A.

2.0 EQUIPMENT REQUIRED

Table 1 lists the test equipment required to perform the ATP.

Table 1. Equipment Required for ATP

Description	Manufacturer	Part No. or Model	Alternate
MC1 (Test)	Validyne	--	None
Extender Card (MC1-MC170)	Validyne	--	None
Test Cable	Validyne	--	None
Transducer Simulator	Validyne	1109	Validyne 1527
Digital Multimeter (DMM)	Data Precision	245	Commercial Equivalent
Oscilloscope	B & K	1470	Commercial Equivalent
Decade Resistance Box	Heath Kit	IN-17	Commercial Equivalent
Function Generator	Interstate	F47	Commercial Equivalent
Frequency Counter	Hewlett Packard	5314A	Commercial Equivalent
Modulator	Validyne	1101	Validyne 1104

3.0 PRELIMINARY PROCEDURE

3.1 Plug extender card into front panel connector on MC1.

3.2 Refer to figure 1 and set switches and controls on CD173-Q2 as follows:

Switch or Control	Setting
GAIN (R30)	Full CW
2/4 (S1B)	2
LO/HI (S1A)	LO
MV/V (S3)	10
FILTER (S4)	200
Reference Phase (R15)	Center (0°)

3.3 Plug CD173-Q2 into extender card cable connector.

8626 WILBUR AVENUE • NORTHRIDGE, CA 91324 • (213) 886-8488 • Telex No. 65-1303

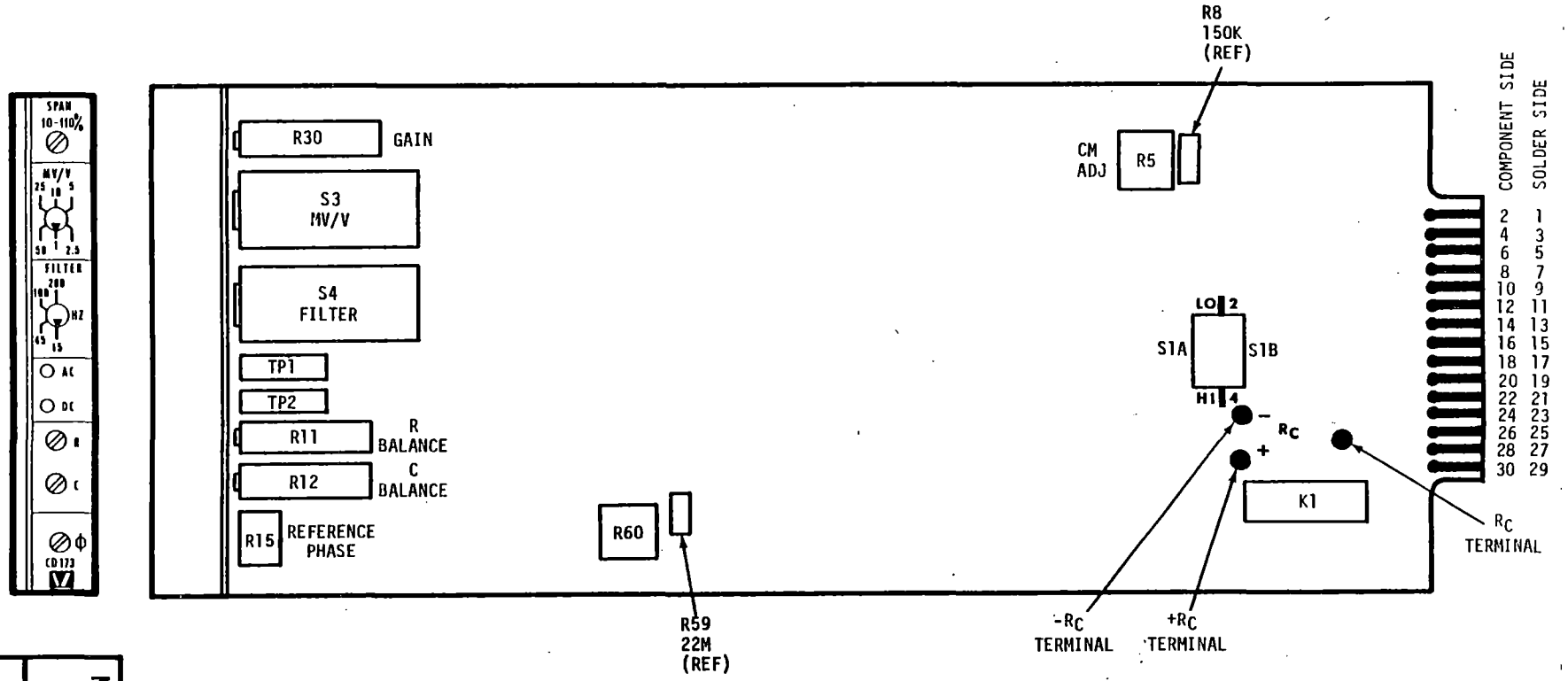


Figure 1. CD173-Q2 Parts Locations

NUMBER	REV
ATP443	B

SHEET 3 OF 12

8626 WILBUR AVENUE • NORTHRIDGE CA 91324 • (213) 886-8488 • Telex No. 65-1303

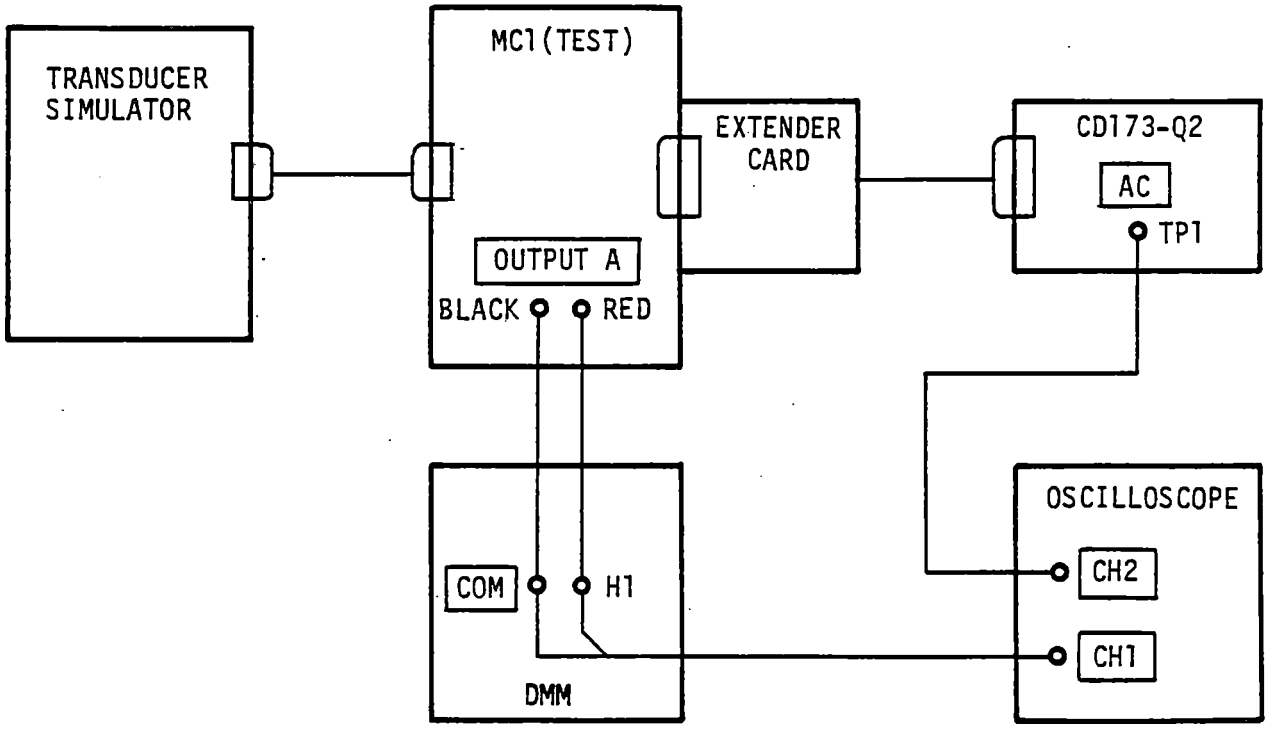
3.4 Connect transducer simulator to input connector on rear panel of MC1; set transducer simulator switches as follows:

Switch	Setting
Polarity	+
X0.1/X1.0	X1.0
Percent (%)	0
RANGE MV/V	1
PIN 2/OFF/CT	PIN 2
PIN 3/OFF/CT	OFF

3.5 If necessary, connect MC1 to 115 Vac and press MC1 power switch; observe that power-on indicator lights.

4.0 INITIAL TEST SETUP

4.1 Connect DMM, oscilloscope, MC1 and CD173-Q2 as shown in figure 2.



NOTE: BOXED CALLOUT [XXX] INDICATES PANEL MARKINGS

Figure 2. Initial Test Setup

NOTE: Unless otherwise indicated, all switches, controls, and test points referred to in the ATP procedures that follow are located on the CD173-Q2; see figure 1 for locations.

8626 WILBUR AVENUE • NORTHRIDGE, CA 91324 • (213) 886-8488 • Telex No. 65-1303

5.0 FUNCTIONAL TESTS

Perform all tests and in the order given.

5.1 Null Adjustment and Noise

5.1.1 Set vertical input sensitivity of oscilloscope channel 2 to 20 mV/division; adjust R and C balance controls R11 and R12 for minimum signal on oscilloscope channel 2 connected to AC test point TP1.

5.2.2 Set MV/V switch S3 to 1. Set DMM to read Vdc.

5.1.3 Adjust R and C balance controls R11 and R12 for minimum signal at AC test point TP1; adjust R60 for 0.000(±0.005)V DC output on DMM.

5.1.4 Output noise level observed on oscilloscope channel 1 should be less than or equal to 20 mV peak-to-peak; indicate acceptance on test report with checkmark.

5.1.5 Set MV/V switch S3 successively to 2.5, 5, 10, 25, and 50; at each position the maximum output indication on the DMM should be 0.000(±0.030)V DC. Indicate acceptance on test report with checkmark.

5.2 Common Mode Adjustment

5.2.1 Set transducer simulator switches as follows:

Switch	Setting
Percent (%)	0
RANGE MV/V	40
PIN 2/OFF/CT	PIN 2
PIN 3/OFF/CT	PIN 3

5.2.2 Set MV/V switch S3 to 1, and 2/4 switch S1B to 4.

5.2.3 Adjust R balance control R11 for 0.000(±0.005)V DC output on DMM.

5.2.4 Set transducer simulator percent (%) switch to 100.

5.2.5 Adjust CM ADJ control R5 for 0.000(±0.005)V DC output on DMM.

5.2.6 Repeat steps 5.2.1, 5.2.3, 5.2.4, and 5.2.5., if necessary to make sure DMM output is 0.000±0.005 Vdc.

5.2.7 Set transducer simulator PIN 3/OFF/CT switch of OFF.

5.3 Maximum Output and Gain

5.3.1 Set transducer simulator percent (%) switch to 25.

5.3.2 Set 2/4 switch S1B to 2. Set DMM to read Vdc.

8626 WILBUR AVENUE • NORTHRIDGE, CA 91324 • (213) 886-8488 • Telex No. 65-1303

5.3.3 The output indication on the DMM should be greater than or equal to +12.000 Vdc: indicate acceptance on test report with checkmark.

5.3.4 Set transducer simulator RANGE MV/V switch to 1 and percent (%) switch to 0.

5.3.5 Adjust R balance control R11 for 0.000(±0.005)V DC output on DMM.

5.3.6 Set transducer simulator percent (%) switch to 100.

5.3.7 Adjust GAIN control R30 fully CCW; output indication on DMM should be +1.000(±0.130) Vdc. Indicate acceptance on test report with checkmark.

5.3.8 Adjust GAIN control R30 for +10.000(±0.005) Vdc output on DMM; output noise level observed on oscilloscope should be less than or equal to 25 mV peak-to-peak. Indicate acceptance on test report with checkmark.

5.3.9 Perform the steps in table 2 to check maximum output and gain of CD173-Q2; for each step set MV/V switch S3 and transducer simulator RANGE MV/V and percent (%) switches as indicated. Indicate acceptance on test report with checkmark.

Table 2. Maximum Output and Gain Check

Step	CD173-Q2 MV/V(S3)	Transducer Simulator		Output Specification On DMM (VDC)
		RANGE MV/V	Percent (%)	
1	1	1	100	+10.000±0.050
2	2.5	2.5	100	+10.000±0.250
3	5	5	100	+10.000±0.250
4	10	10	100	+10.000±0.250
5	25	40	50	+ 8.000±0.200
6	50	40	100	+ 8.000±0.200

5.3.10 Set the simulator to 1 mV/V range. Perform the steps in the following table by setting the percent switch, on the simulator, to 0% and 100% and note the readings at each setting of the mV/V switch (S3) of Cd173-Q2. Call these readings E1 and E2 respectively. The difference between E2 and E1 should be as given in the following table. Indicate acceptance with checkmark on test report.

8626 WILBUR AVENUE • NORTHRIDGE, CA 91324 • (213) 886-8488 • Telex No. 65-1303

5.3.10 (Cont'd).

STEP	CD173-02 mV/V SWITCH (S3) SETTING	DMM READING WITH 0% INPUT E1 (Vdc)	DMM READING WITH 100% INPUT E2 (Vdc)	DIFFERENCE E2 - E1 (Vdc)
1	1	---	---	10.000±0.010
2	2.5	---	---	4.000±0.100
3	5	---	---	2.000±0.050
4	10	---	---	1.000±0.025
5	25	---	---	0.400±0.010
6	50	---	---	0.200±0.005

5.4 Linearity and Symmetry

5.4.1 Set MV/V switch S3 to 10.

5.4.2 Set 2/4 switch S1B to 4. Set DMM to read Vdc.

5.4.3 Set transducer simulator switches as follows:

SWITCH	SETTING
RANGE MV/V	10
PERCENT (%)	0
PIN 2/OFF/CT	2
PIN 3/OFF/CT	CT

8626 WILBUR AVENUE • NORTHRIDGE, CA 91324 • (213) 886-8488 • Telex No. 65-1203

5.4.4 Adjust R balance control R11 for 0.000(±0.002)V DC on DMM.

5.4.5 Set transducer simulator percent (%) switch to 100.

5.4.6 Adjust reference phase control R15 for maximum output on DMM.

5.4.7 Set transducer simulator percent (%) switch to 0; output indication on DMM should be 0.000(±0.002)V DC.

5.4.8 Repeat steps 5.4.4 thru 5.4.6 as necessary to obtain desired readings.

5.4.9 Set transducer simulator percent (%) switch to 100; adjust GAIN control R30 for +10.000(±0.002) Vdc output on DMM.

5.4.10 Perform the steps in table 3 to check linearity and symmetry of CD173-Q2; for each step set transducer simulator polarity and percent (%) switches as indicated, and indicate acceptance on test report with checkmark.

Table 3. Linearity and Symmetry Check

Step	Transducer Simulator		Output Specification On DMM (VDC)
	Polarity	Percent (%)	
1	+	0	0.000±0.002
2	+	25	+ 2.500±0.005
3	+	50	+ 5.000±0.005
4	+	75	+ 7.500±0.005
5	+	100	+10.000±0.005
6	-	0	0.000±0.002
7	-	25	- 2.500±0.005
8	-	50	- 5.000±0.005
9	-	75	- 7.500±0.005
10	-	100	-10.000±0.005

5.5 4-Arm and High/Low Balance

5.5.1 Set transducer simulator switches as follows:

Switch	Setting
Polarity	+
Percent (%)	0
RANGE MV/V	10
PIN 2/OFF/CT	PIN 2
PIN 3/OFF/CT	CT

5.5.2 Set DMM to read Vdc, adjust R balance control R11 for 0.000 (±0.001) Vdc output on DMM.

8626 WILBUR AVENUE • NORTHRIDGE, CA 91324 • (213) 886-8488 • Telex No. 65-1303

5.5.3 Set 2/4 switch S1B to 2, and transducer simulator PIN 3/OFF/CT switch to OFF; output indication on DMM should be 0.000(±0.500)V DC. Indicate acceptance on test report with checkmark.

5.5.4 Set 2/4 switch S1B to 4 and transducer simulator PIN 3/OFF/CT switch to CT.

5.5.5 Set MV/V switch S3 to 25 and LO/HI switch S1A to HI.

5.5.6 Adjust R balance control R11 full CW; output on DMM should be +8.00(±0.4) Vdc. Indicate acceptance on test report with checkmark.

5.5.7 Set LO/HI switch S1A to LO; output on DMM should be +0.800(±0.2) Vdc. Indicate acceptance on test report with checkmark.

5.5.8 Adjust R balance control R11 full CCW; output on DMM should be -0.800 (±0.2) Vdc. Indicate acceptance on test report with checkmark.

5.6 Calibration Circuit

5.6.1 Set 2/4 switch S1B to 2 and transducer simulator PIN 2/OFF/CT switch to PIN 2, and PIN 3/OFF/CT switch to OFF. Set DMM to read Vdc.

5.6.2 Set MV/V switch S3 to 10, and adjust R balance control R11 for 0.000 (±0.002)V DC on DMM.

5.6.3 Set decade resistance box to 24.9K; connect one lead of decade resistance box to the $+R_C$ terminal and the other lead to the unmarked R_C terminal on CD173-Q2 (figure 1); the output indication on DMM should not change.

5.6.4 On CD173-Q2, connect pin 28 of connector (figure 1) to ground; the output indication on DMM should be +9.840(±0.400) Vdc. Indicate acceptance on test report with checkmark.

5.6.5 Move the decade resistance box lead from the $+R_C$ terminal to the $-R_C$ terminal on CD173-Q2 (figure 1); the output indication on DMM should be -9.840(±0.400) Vdc. Indicate acceptance on test report with checkmark.

5.6.6 Remove decade resistance box leads from terminals and the ground from pin 28 of connector.

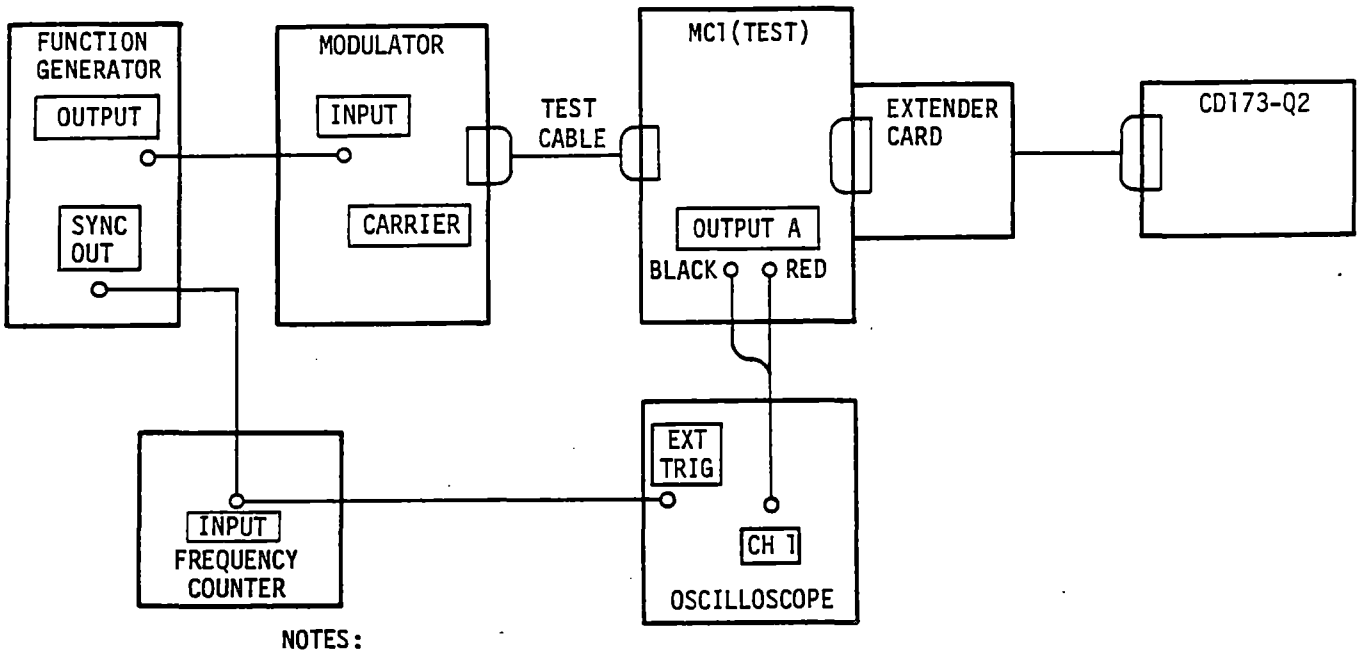
5.6.7 Disconnect oscilloscope from CD173-Q2.

5.6.8 Disconnect DMM and transducer simulator from MC1.

5.7 Filter

5.7.1 Connect function generator, modulator, frequency counter, and oscilloscope as shown in figure 3.

8626 WILBUR AVENUE • NORTHRIDGE, CA 91324 • (213) 886-8488 • Telex No. 65-1303



NOTES:

1. BOXED CALLOUT [XXX] INDICATES PANEL OR BOARD MARKINGS

Figure 3. Filter Test Setup

5.7.2 Set oscilloscope for 1V/DIV display, external trigger, and DC coupling; set function generator for a 60 Hz, 3V RMS output.

5.7.3 Set CD173-Q2 switches as follows:

Switch	Setting
2/4 (S1B)	4
LO/HI (S1A)	LO

5.7.4 15 Hz Test

5.7.4.1 Set FILTER switch S4 to 15 HZ.

5.7.4.2 Set function generator for a 1.5 Hz sinewave output, as indicated on the frequency counter, and adjust modulator output for a 7-division display on oscilloscope.

8626 WILBUR AVENUE • NORTHRIDGE, CA 91324 • (213) 886-8488 • Telex No. 65-1303

5.7.4.3 Increase function generator output frequency until oscilloscope display decreases to 5 divisions; the frequency counter should indicate 15(±2)Hz. Indicate acceptance on test report with checkmark.

5.7.5 45 Hz Test

5.7.5.1 Set FILTER switch S4 to 45 HZ.

5.7.5.2 Increase function generator output frequency until oscilloscope display decreases to 5 divisions; the frequency counter should indicate 45(±7)Hz. Indicate acceptance on test report with checkmark.

5.7.6 100 Hz Test

5.7.6.1 Set FILTER switch S4 to 100 HZ.

5.7.6.2 Increase function generator output frequency until oscilloscope display decreases to 5 divisions; the frequency counter should indicate 100(±15)Hz. Indicate acceptance on test report with checkmark.

5.7.7 200 Hz Test

5.7.7.1 Set FILTER switch S4 to 200 HZ.

5.7.7.2 Increase function generator output frequency until oscilloscope display decreases to 5 divisions; the frequency counter should indicate 200(±30)Hz. Indicate acceptance on test report with checkmark.

5.7.8 Disconnect oscilloscope and test cable from MC1.

5.8 Current Consumption

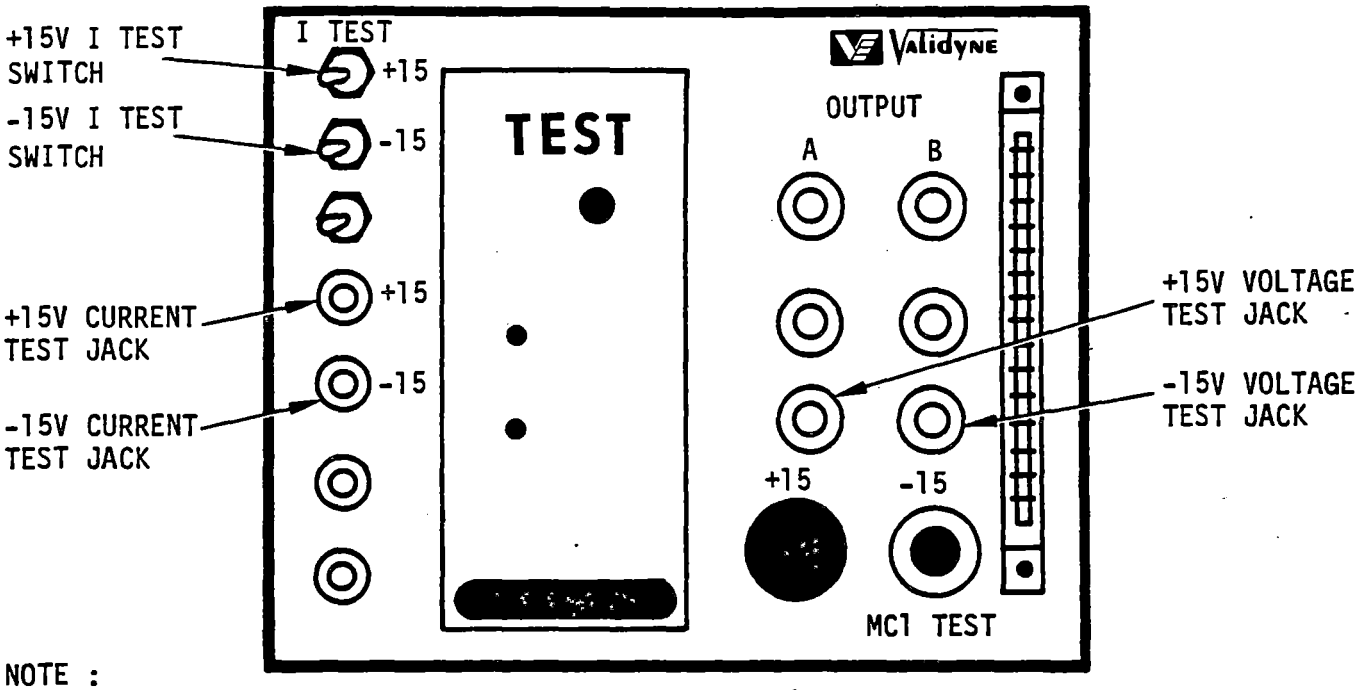
5.8.1 Connect the DMM leads to the MC1 +15V current and voltage test jacks (figure 4); set DMM to read DCmA.

5.8.2 Set the MC1 +15V I TEST switch (figure 4) to +15; the DMM indication should not exceed 22 mA. Indicate acceptance on test report with checkmark.

5.8.3 Set the MC1 +15V I TEST switch to the unmarked position; disconnect the DMM leads from the MC1.

5.8.4 Connect the DMM leads to the MC1 -15V current and voltage test jacks (figure 4).

5.8.5 Set the MC1 -15V I TEST switch (figure 4) to -15; the DMM indication should not exceed 22 mA. Indicate acceptance on test report with checkmark.



NOTE :

1. CONNECT DMM COM LEAD TO CURRENT TEST JACK AND HI LEAD TO VOLTAGE TEST JACK

Figure 4. MC1 (Test) ±15V Current Test Switch and Jack Locations

5.8.6 Set the MC1 -15V I TEST switch to the unmarked position; disconnect the DMM leads from the MC1.

5.8.7 Unplug CD173-Q2 from extender card cable connector.

8626 WILBUR AVENUE • NORTHRIDGE, CA 91324 • (213) 886-8488 • Telex No. 65-1303

Validyne
ENGINEERING CORPORATION

APPENDIX A

SAMPLE TEST REPORT

NUMBER	REV
ATP443	B
SHEET 1 OF 5	

Validyne ENGINEERING CORPORATION

TEST REPORT

ASSY CD173-Q2 High-Gain Carrier Demodulator

S/O _____ CUSTOMER _____

W/O _____ SERIAL NO. _____

TESTED BY _____ DATE _____

Paragraph/Step		Accepted	Specification
5.1	Null Adjustment and Noise		
5.1.4	Oscilloscope Indication	_____	≤20 mVp-p
5.1.5	DMM Indication		
	S3 at 2.5	_____	0.000 (±0.030) Vdc
	S3 at 5	_____	0.000 (±0.030) Vdc
	S3 at 10	_____	0.000 (±0.030) Vdc
	S3 at 25	_____	0.000 (±0.030) Vdc
	S3 at 50	_____	0.000 (±0.030) Vdc
5.3	Maximum Output and Gain		
5.3.3	DMM Indication	_____	≥+12.000 Vdc
5.3.7	DMM Indication	_____	+1.000 (±0.130) Vdc
5.3.8	Oscilloscope Indication	_____	≤25 mVp-p
5.3.9	Table 2 Step Indication On		
	1 DMM	_____	+10.000(±0.050) Vdc
	2 DMM	_____	+10.000(±0.250) Vdc
	3 DMM	_____	+10.000(±0.250) Vdc
	4 DMM	_____	+10.000(±0.250) Vdc

QC _____

8626 WILBUR AVENUE • NORTHRIDGE, CA 91324 • (213) 886-8488 • Telex No. 65-1303

Validyne ENGINEERING CORPORATION

TEST REPORT

ASSY CD173-Q2 High-Gain Carrier Demodulator

S/O _____ CUSTOMER _____

W/O _____ SERIAL NO. _____

TESTED BY _____ DATE _____

Paragraph/Step			Accepted	Specification
5.3.9	Table 2 (Continued)			
	Step	Indication On		
	5	DMM	_____	+8.000 (±0.200) Vdc
	6	DMM	_____	+8.000 (±0.200) Vdc
5.3.10				
	Step	Indication On		
	1	E_2-E_1	_____	10.000±0.010 Vdc
	2	E_2-E_1	_____	4.000±0.100 Vdc
	3	E_2-E_1	_____	2.000±0.050 Vdc
	4	E_2-E_1	_____	1.000±0.025 Vdc
	5	E_2-E_1	_____	0.400±0.010 Vdc
	6	E_2-E_1	_____	0.200±0.005 Vdc
5.4	Linearity and Symmetry			
5.4.10	Table 3			
	Step	Indication On		
	1	DMM	_____	0.000(±0.002) Vdc
	2	DMM	_____	+2.500(±0.005) Vdc

QC _____

NUMBER	REV
ATP443	B

8626 WILBUR AVENUE • NORTHRIDGE, CA 91324 • (213) 886-8488 • Telex No. 65-1303

Validyne ENGINEERING CORPORATION

TEST REPORT

ASSY CD173-Q2 High-Gain Carrier Demodulator

S/O _____ CUSTOMER _____

W/O _____ SERIAL NO. _____

TESTED BY _____ DATE _____

Paragraph/Step		Accepted	Specification
5.4.10	Table 3 (Cont'd).		
Step	Indication On		
3	DMM	_____	+5.000 (±0.005) Vdc
4	DMM	_____	+7.500 (±0.005) Vdc
5	DMM	_____	+10.000 (±0.005) Vdc
6	DMM	_____	0.000 (±0.002) Vdc
7	DMM	_____	-2.500 (±0.005) Vdc
8	DMM	_____	-5.000 (±0.005) Vdc
9	DMM	_____	-7.500 (±0.005) Vdc
10	DMM	_____	-10.000 (±0.005) Vdc
5.5	4-Arm and High/Low Balance		
5.5.3	DMM Indication	_____	0.000 (±0.500) Vdc
5.5.6	DMM Indication	_____	+8.000 (±0.4) Vdc
5.5.7	DMM Indication	_____	+0.800 (±0.2) Vdc
5.5.8	DMM Indication	_____	-0.800 (±0.2) Vdc
5.6	Calibration Circuit		
5.6.4	DMM Indication	_____	+9.840 (±0.400) Vdc
5.6.5	DMM Indication		-9.840 (±0.400) Vdc

QC _____

8626 WILBUR AVENUE • NORTHRIDGE, CA 91324 • (213) 886-8488 • Telex No. 65-1303

Validyne ENGINEERING CORPORATION

TEST REPORT

ASSY CD173-Q2 High-Gain Carrier Demodulator

S/O _____ CUSTOMER _____

W/O _____ SERIAL NO. _____

TESTED BY _____ DATE _____

Paragraph/Step		Accepted	Specification
5.7	Filter		
5.7.4.3	Frequency Counter Indication	_____	15 (±2) Hz
5.7.5.2	Frequency Counter Indication	_____	45 (±7) Hz
5.7.6.2	Frequency Counter Indication	_____	100 (±15) Hz
5.7.7.2	Frequency Counter Indication	_____	200 (±30) Hz
5.8	Current Consumption		
5.8.2	DMM Indication	_____	22 mA max.
5.8.5	DMM Indication	_____	22 mA max.

QC _____

8626 WILBUR AVENUE • NORTHRIDGE, CA 91324 • (213) 886-8488 • Telex No. 65-1303