PRESSURIZED WATER REACTOR OWNERS GROUP

PWROG

PWR Owners Group

PWROG-17018-NP
Revision 0

WESTINGHOUSE NON-PROPRIETARY CLASS 3

Solid State Protection System General Warning Alarm Modification

Licensing Committee

PA-LSC-1366, Revision 1

January 2018

Westinghouse

PWROG-17018-NP
Revision 0

Solid State Protection System General Warning Alarm Modification

PA-LSC-1366, Revision 1

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January 2018

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ACKNOWLEDGEMENTS

This report was developed and funded by the Pressurized Water Reactor Owners Group (PWROG) under the leadership of the participating utility representatives of the Licensing Committee and the Instrumentation and Control Working Group (ICWG). The author would like to thank the following people and/or organizations for their valuable contributions to this report:

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Douglas W. Atkins

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Centrales Nucleares Almaraz-Trillo	Almaraz 1 & 2 (W)	X	
EDF Energy	Sizewell B (W)		X
Electrabel	Doel 1, 2 & 4 (W)		X
	Tihange 1 & 3 (W)		X
Electricite de France	58 Units		X
Elektriciteits Produktiemaatschappij Zuid-Nederland	Borssele 1 (Siemens)		X
Eletronuclear-Eletrobras	Angra 1 (W)		X
Emirates Nuclear Energy Corporation	Barakah 1 & 2		X
Eskom	Koeberg 1 & 2 (W)		X
Hokkaido	Tomari 1, 2 & 3 (MHI)		X
Japan Atomic Power Company	Tsuruga 2 (MHI)		X
Kansai Electric Co., LTD	Mihama 3 (W)		X
	Ohi 1, 2, 3 & 4 (W & MHI)		X
	Takahama 1, 2, 3 & 4 (W & MHI)		X
Korea Hydro & Nuclear Power Corp.	Kori 1, 2, 3 & 4 (W)		X
	Hanbit 1 & 2 (W)		X
	Hanbit 3, 4, 5 & 6 (CE)		X
	Hanul 3, 4 , 5 & 6 (CE)		X
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	Sendai 1 & 2 (MHI)		X
Nuklearna Electrarna KRSKO	Krsko (W)		X
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ACRONYMS AND ABBREVIATIONS

Acronym	Definition
AC	Alternating Current
AEC	Atomic Energy Commission
CCB	Clock Counter Board
CFR	Code of Federal Regulations
CPLD	Complex Programmable Logic Device
DEC	Decoder Board
E10	Self-Test Failure for 10 Consecutive Cycles
ESF	Engineered Safety Feature
ESFAS	Engineered Safety Feature Actuation System
FMEA	Failure Mode Effects Analysis
GW	General Warning
GWMC	General Warning Monitor Circuit
GWAC	General Warning Alarm Circuitry
GWACM	General Warning Alarm Circuitry Modification
ICWG	Instrumentation and Control Working Group
IEEE	Institute of Electrical and Electronics Engineers
LED	Light Emitting Diode
LSC	Licensing Subcommittee
MCB	Main Control Board
NC	Normally Closed
NRC	Nuclear Regulatory Commission
NO	Normally Open
PA	Project Authorization
PCB	Printed Circuit Board
PWROG	Pressurized Water Reactor Owners Group
RTS	Reactor Trip System
SAT	Semi-Automatic Tester
SGD	Safeguards Driver Board
SEE	Systems and Equipment Engineering
SPV	Single Point Vulnerability

SSPS	Solid State Protection System
TR	Topical Report
UFSAR	Updated Final Safety Analysis Report
ULB	Universal Logic Board
U.S.	United States
UVD	Under Voltage Driver Board
VAC	Voltage Alternating Current
VDC	Voltage Direct Current
WCAP	Westinghouse Commercial Atomic Power (topical report)
WDE	Watchdog Error

1 INTRODUCTION AND PURPOSE

1.1 INTRODUCTION

This topical report (TR) was developed for the Pressurized Water Reactor Owners Group (PWROG) Licensing Committee and Instrumentation and Control Working Group (ICWG) to support implementation of Solid State Protection System (SSPS) reliability improvements by minimizing the potential of inadvertent plant reactor trips associated with the current SSPS General Warning (GW) alarm. The SSPS GW alarm generates a partial (half) reactor trip signal when an SSPS train is in the GW alarm condition, and inadvertent reactor trips have occurred due to simultaneous occurrence of a GW alarm in both SSPS trains. Implementation of the General Warning Alarm Circuitry Modification (GWACM) described in this TR would reduce the number of inputs that could lead to an inadvertent reactor trip. The inputs removed from the GW alarm would be moved to a new non-urgent alarm that does not cause a reactor trip signal in the affected SSPS train. The addition of a new non-urgent alarm will also allow plants to enable the new design SSPS printed circuit board (PCB) self-test function to provide remote indication of a self-test alarm condition in the control room on the Main Control Board (MCB).

The GWACM involves removing the following inputs to the SSPS GW alarm circuit:

1) The loss of one 15 VDC power supply
2) The loss of one 48 VDC power supply
3) The multiplexer test switch selected to the "Inhibit" position
4) The pulled card (Rows 2-5) interlock

All of these GW alarm inputs will be moved to provide input to a new non-urgent alarm. The modification also enables the non-urgent alarm to indicate if a new design SSPS Universal Logic Board (ULB), Safeguards Driver (SGD), or Under Voltage Driver (UVD) PCB failed a self-test using the feature that continuously tests the functions of the PCB's basic logic and output drivers. The non-urgent alarm will interface with the MCB to indicate audibly and visually by using either a separate alarm window or a shared alarm window for each SSPS train. It should also be emphasized that the term "non-urgent" was assigned to the new alarm, since it does not initiate a reactor trip input. The non-urgent alarm will provide indications for conditions that do and do not involve a potential loss of safety function; therefore, the operator response to the new non-urgent alarm will be the same as the response to the current GW alarm.

The GW alarm is not included in the plant Technical Specifications, and is not assumed to mitigate any accident in the plant safety analyses.

These circuitry changes will change the SSPS GW alarm design and licensing bases. The SSPS GW alarm reactor trip function was installed as part of the SSPS design that was approved by the United States (U.S.) Atomic Energy Commission (AEC) (Reference 1). The system design basis is documented in WCAP-7672, "Solid State Logic Protection System Description" (Reference 2) and WCAP-7706, "An Evaluation of Solid State Logic Reactor Protection in Anticipated Transients" (Reference 4). These TRs describe the inputs that result in a partial reactor trip signal in an SSPS train, including a loss of 15V and 48V power supplies, a pulled card (PCB), and the multiplexer test switch selected to the "Inhibit" position. A 10 CFR 50.59 Evaluation that was prepared for the PWROG reviewed those SSPS design basis documents and determined that the proposed SSPS GWACM could not be implemented without prior NRC review and approval.

1.2 PURPOSE

The purpose of this TR is to: 1) define the GWACM functional requirements, 2) describe the generic modification details, and 3) provide the technical justification for implementation of the SSPS GWACM.

The GWACM removes the partial reactor trip function for specific GW input signals (see Table 1-1) that, with the exception of the "Failed Self-Test" signal, currently generate a GW alarm condition in the respective SSPS train. The GWACM will move these input signals and the new design SSPS PCB failed self-test input to a new non-urgent audible and visual alarm on the MCB. The new non-urgent alarm will be installed as either a separate or shared indication from the existing GW alarm panel window on the MCB.

Table 1-1 SSPS General Warning Partial Reactor Trip Input Signals
Input Error Inhibit Switch in the INHIBIT position
Memories Test Switch not in the OFF position
Reactor Trip Bypass Breaker RACKED-IN and CLOSED (contact)
Output Mode Selector Switch in the TEST position
Permissive Test Switch not in the OFF position
Logic Test Switch A not in the OFF position
Blown ground return fuse (where applicable – not included in all SSPS designs)
Loss of 118 VAC Output Relay Power (where applicable – not included in all SSPS designs)
Card Frame Interlock Row 1 OPEN circuit
MOVE THE FOLLOWING GENERAL WARNING ALARM INPUT SIGNALS TO A NON-URGENT ALARM
Loss of +48V1 Power Supply
Loss of +48V2 Power Supply
Loss of +15V1 Power Supply
Loss of +15V2 Power Supply
Multiplexer Test Switch in the INHIBIT Position (Not in NORMAL or A+B position)
Pulled Card Interlock (Rows 2-5)
Failed Self-Test(1)
Note: 1. This function is contained in the new design SSPS ULB, UVD, & SGD PCBs only, and is not included in the original SSPS design or the GW input signals.

As shown in Table 1-2, the GWACM, as specified herein, is only applicable to plants that have the new design SSPS PCBs installed.

Table 1-2 New Design SSPS PCBs Required for the GWACM

Assembly Drawing	PCB Description
6D30225	Universal Logic Board (ULB)
6D30252	Safeguards Driver Board (SGD)
6D30350	Under Voltage Driver Board (UVD)
6D30520	Semi-Automatic Tester Board (SAT)

2 BACKGROUND

The SSPS GW alarm partial reactor trip function was installed as part of the original SSPS design that was approved by the AEC in the early 1970s. A GW alarm condition generates a partial reactor trip when active in a single SSPS logic train. If a GW alarm condition is generated in both SSPS trains a reactor trip will occur (see Figure 2-1 and Figure 2-2). Additional information on the current GW circuit design is contained in WCAP-7672 and WCAP-7488-L (References 2 and 3, respectively).

A survey of the Westinghouse SSPS plants was conducted by the PWROG in 2005. The survey identified that a reactor trip occurred on four separate occurrences during at-power actuation logic testing as a result of the SSPS GW alarm partial reactor trip function. A reactor trip occurred at those plants during surveillance testing that required the multiplexer test switch to be placed in the "A+B" position when one SSPS train was in a GW alarm condition and the opposite SSPS train multiplexer test switch was rotated through the "INHIBIT" position. Plant reliability can be improved by minimizing the potential for similar inadvertent reactor trips associated with the SSPS GW alarm.

a,c

Figure 2-1. SSPS GW Monitor Zener Circuit (3-Bay Typical [Left] / 4-Bay Typical [Right])

Figure 2-2. GWMC Simplified Interface Block Diagram (Typical 3-Bay and 4-Bay)

3 GENERAL WARNING ALARM DESIGN

A generic functional block diagram of the current GW alarm design is illustrated by Figure 3-1. The SSPS SAT PCB processes the GW alarm input signals shown on Figure 3-1 to generate the output signals for audible and visual indication on the MCB and also provide a local alarm indication at the SSPS cabinet, as well as initiation of a partial reactor trip. Either an original design or a new design SSPS SAT PCB can implement the functions illustrated in Figure 3-1.

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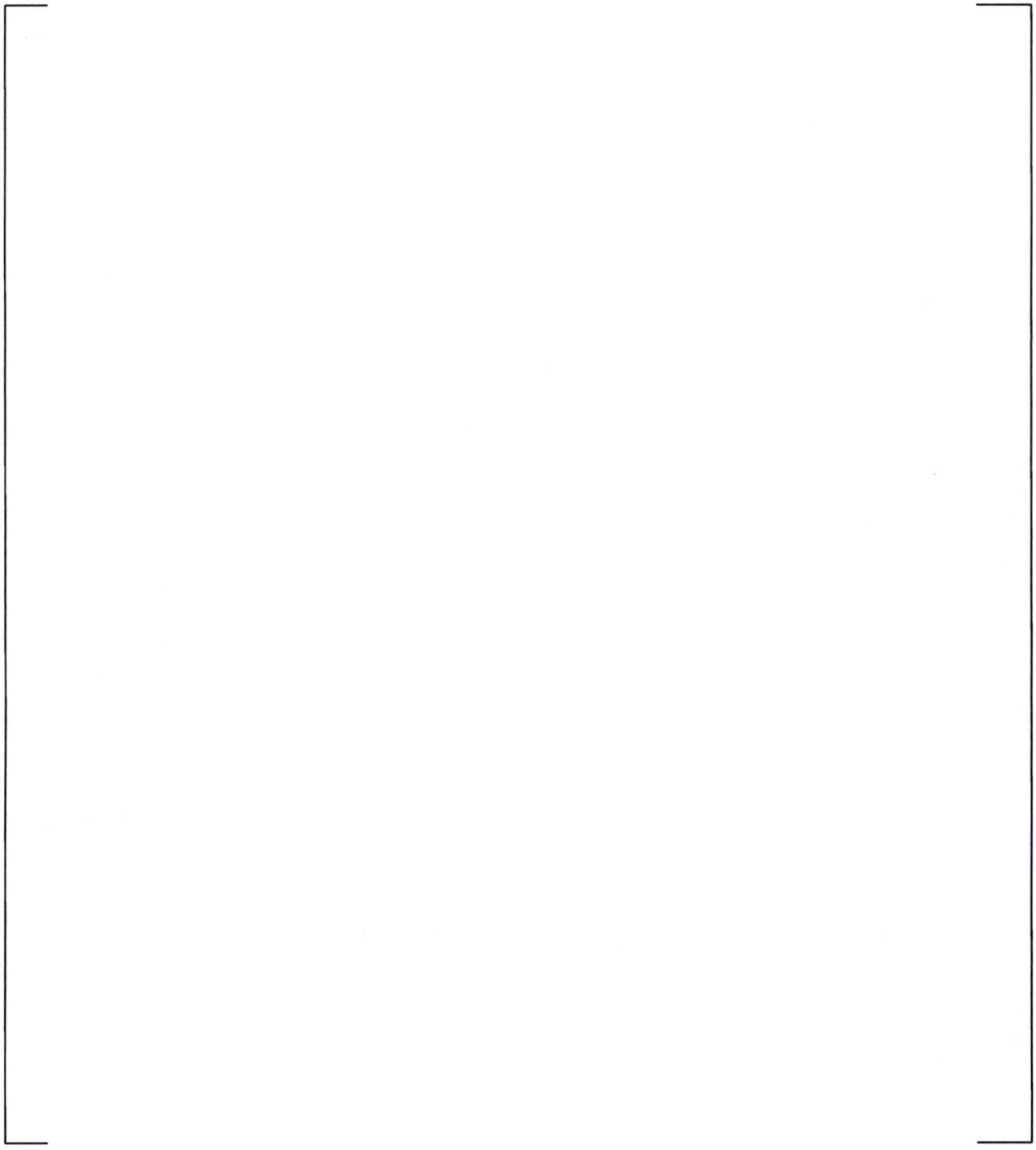

Figure 3-1. General Warning Alarm Circuitry Design (Typical)

4 GENERAL WARNING ALARM CIRCUITRY MODIFICATION

This section describes the system performance requirements for the GWACM design presented in Figure 4-1.

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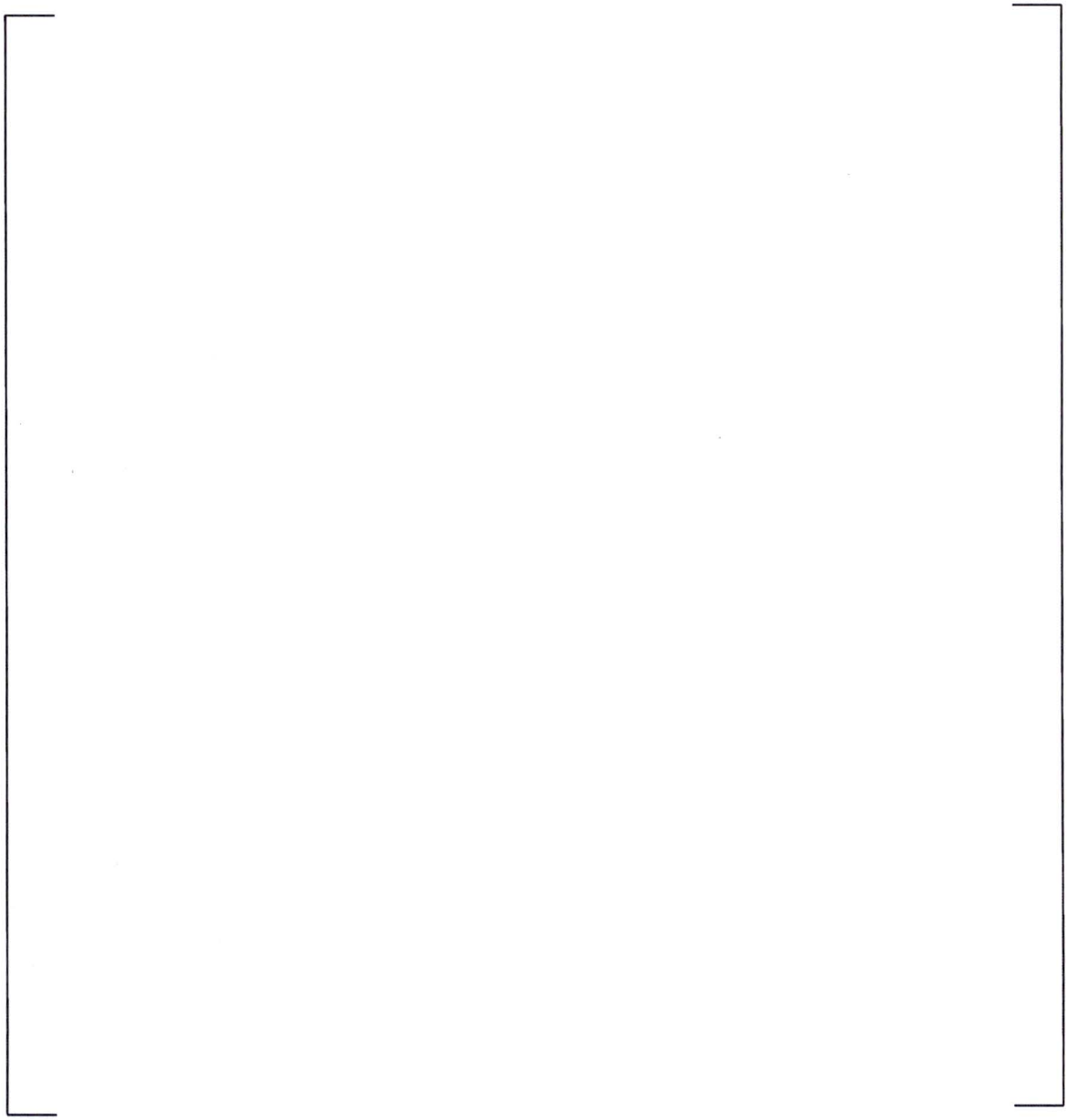

Figure 4-1. Generic GWACM Design

The following sections identify the system performance, annunciator/alarm, physical/fabrication, and compliance requirements for the GWACM.

4.1 NON-URGENT ALARM INPUTS

The GWACM will remove the SSPS train-specific GW alarm reactor trip signal caused by the occurrence of any one of the following alarm inputs. These inputs will provide a remote alarm from each SSPS train as shown in Figure 4-1:

1. Loss of +48V1 power supply
2. Loss of +48V2 power supply
3. Loss of +15V1 power supply
4. Loss of +15V2 power supply
5. Multiplex Test Switch not in the NORMAL or A+B position
6. Pulled Card Interlock Row 2 is an open circuit (due to removed / loose PCB)
7. Pulled Card Interlock Row 3 is an open circuit (due to removed / loose PCB)
8. Pulled Card Interlock Row 4 is an open circuit (due to removed / loose PCB)
9. Pulled Card Interlock Row 5 is an open circuit (due to removed / loose PCB)
10. New Design ULB, SGD or UVD PCB self-test alarm (E10) or Watchdog Error (WDE) indicating an error in the PCB circuitry.

In the original SSPS design, Items 1 through 9 above provide GW alarm inputs, which annunciate a local alarm at the SSPS cabinet and an alarm on the MCB, and the initiation of a partial reactor trip signal in the affected SSPS train consistent with the AEC-approved SSPS design described in References 2 and 3. Item 10 is an additional function that was added to the new design SSPS PCBs. The self-test alarm did not exist with the original SSPS design that was approved by the AEC. The following non-urgent alarm inputs will be implemented with the GWACM:

1&2. Loss of a single +48V1 or +48V2 power supply: Each +48V power supply is redundant (+48V1 and +48V2), and the output is diode auctioneered, such that a loss of one power supply does not inhibit the SSPS train's ability to perform its Reactor Trip System (RTS) and Engineered Safety Feature Actuation System (ESFAS) functions. The SSPS train is operable with loss of redundancy (Single Point Vulnerability [SPV] state), and therefore, there is no loss of safety function in the affected SSPS train. This condition would be indicated to the operator with the SSPS non-urgent alarm on the MCB, similar to the indication already in place with the current GW alarm. A loss of a +48V power supply is sensed by the SSPS SAT PCB. The loss of a single 48V power supply was removed from the three-train SSPS GW alarm design and a non-urgent alarm is sent through multiplexing to the MCB for indication. Therefore, this aspect of the GWACM, i.e., moving power supply monitoring from a GW alarm to a non-urgent alarm has previously been implemented.

3&4. Loss of a single +15V1 or +15V2 power supply: Each +15V power supply is redundant (+15V1 and +15V2), and the output is diode auctioneered, such that a loss of one power supply does not inhibit the SSPS train's ability to perform its RTS and ESFAS

functions. The SSPS train is operable with loss of redundancy (SPV state), and therefore, there is no loss of safety function of the affected SSPS train. This condition would be indicated to the operator with the SSPS non-urgent alarm on the MCB, similar to the indication provided by the current GW alarm. A loss of a +15V power supply is sensed by the SSPS SAT PCB. The loss of a single 15V power supply was removed from the three-train SSPS GW alarm design and a non-urgent alarm is sent through multiplexing to the MCB for indication. Therefore, this aspect of the GWACM, i.e., moving power supply monitoring from the GW alarm to a non-urgent alarm has previously been implemented.

5. Multiplexer Test Switch in the INHIBIT position: The multiplexer test switch is a three-position switch with the following three switch positions: "NORMAL," "INHIBIT," and "A+B." Currently, a GW alarm is generated when this switch is placed out of the "NORMAL" or "A+B" position as it passes through the "INHIBIT" position, which removes the SSPS SAT PCB input path to ground causing an open circuit and a GW alarm signal. While the switch is in the "INHIBIT" position, multiplexing status information is blocked from the associated SSPS train by inhibiting data inputs, causing a loss of the SSPS train data to the MCB and plant computer. However, there is no loss of safety function in the affected SSPS train, since the opposite SSPS train will continue to provide MCB and plant computer trip/logic status data during this time. All safety functions within the SSPS train will continue to operate as required with the multiplexer test switch in the "INHIBIT" position. With the GWACM, the multiplexer test switch in the "INHIBIT" position will be indicated with a non-urgent alarm. This modification is considered to be an SSPS reliability improvement because it minimizes the potential of inadvertently having both SSPS trains in a GW alarm partial reactor trip condition, which would cause a reactor trip.

6-9. Pulled Card Interlock in Rows 2–5: The SSPS ULB, SGD, and UVD PCBs are located in Rows 2–5. In the current SSPS design, a GW alarm occurs and places the affected SSPS train in a partial reactor trip when an SSPS ULB, SGD, or UVD PCB is pulled or not inserted. If it is determined that one of the SSPS ULB, SGD, or UVD PCBs were pulled or not fully inserted, that particular SSPS train's ability to provide an RTS or ESFAS actuation may be affected. With the GWACM, a pulled or not fully inserted SSPS ULB, SGD, or UVD PCB will be indicated with a non-urgent alarm. The new non-urgent alarm would require operator action that is the same as the operator response to a GW alarm response. The redundant SSPS train would provide an RTS or ESFAS actuation, if required. The Row 1 pulled card interlock for the SSPS DEC, CCB, and SAT PCBs is not modified and is retained with the GW alarm inputs. The GWACM pulled card interlock change in Rows 2–5 is necessary for the SSPS ULB, SGD, and UVD PCB self-test alarm to be annunciated on the MCB as described below.

10. New Design SSPS PCB WDT or an E10 Self-Test Failure: The SSPS ULB, SGD, and UVD PCBs have a self-test function that continuously tests the functions of the PCB's basic logic and output drivers. [

]^{a,c} Following the GWACM SSPS logic cabinet wiring modifications and on-board PCB jumper configuration changes, when a new design SSPS ULB, SGD, or UVD PCB generates a self-test error,
[

]^{a,c}
and the SAT PCB will generate a non-urgent alarm without a partial reactor trip signal. This design feature requires the installation of the new design SSPS SAT, ULB, SGD, and UVD PCBs with the specific jumper configurations identified in this TR.

4.2 NON-URGENT ALARM SSPS/ANNUNCIATOR SYSTEM FUNCTIONAL INTERFACE

The GWACM will provide a new remote annunciation (train-specific) interface (e.g., relay contact) to facilitate audible and visual MCB indication upon receipt of a non-urgent alarm. The new alarm can be implemented separately from, or shared with the existing GW alarm annunciation. The operator response for the SSPS non-urgent alarm will be the same as the response to the current SSPS GW alarm response.

A separate indication for the non-urgent alarm identifies that the applicable SSPS train is not in a partial reactor trip condition, and also provides a GW alarm on the existing annunciation circuit. However, the existing MCB alarm windows can be configured to indicate on both the GW alarm and the non-urgent alarm. This minimizes the impact on the MCB alarm panel configuration. Additional annunciator windows are required for a separate indication. A separate non-urgent alarm indication is currently implemented at one plant for the loss of an SSPS output relay AC power supply. A shared non-urgent alarm indication is currently implemented at another plant for the loss of SSPS output relay AC power. Therefore, both shared and separate MCB alarm panel configurations are currently implemented for SSPS alarm indications.

4.3 NON-URGENT ALARM MAIN CONTROL BOARD INTERFACE

The remote annunciation on the MCB will illuminate on the occurrence of any one of the following signals. The non-urgent alarm is not required to have a reflash capability. Conditions 1–4 result in a loss of redundancy. Condition 5 results in a loss of SSPS train data to the MCB and plant computer with no loss of RTS or ESFAS actuation function. Conditions 6–10 result in a potential degraded SSPS logic train and potential inoperable state. However the other SSPS train would be capable performing an RTS or ESFAS actuation, if required.

1. Loss of +48V1 power supply
2. Loss of +48V2 power supply

3. Loss of +15V1 power supply
4. Loss of +15V2 power supply
5. Multiplexer Test Switch not in the NORMAL or A+B position
6. Pulled Card Interlock Row 2 is an open circuit (due to removed / loose PCB)
7. Pulled Card Interlock Row 3 is an open circuit (due to removed / loose PCB)
8. Pulled Card Interlock Row 4 is an open circuit (due to removed / loose PCB)
9. Pulled Card Interlock Row 5 is an open circuit (due to removed / loose PCB)
10. New Design SSPS ULB, SGD or UVD PCB self-test alarm (E10) or WDE indicating an error in the PCB circuitry.

The state of a non-urgent alarm in an SSPS train must be known by the operator in the control room. The operator must be aware that the SSPS train may be degraded when an alarm condition exists. For a shared MCB alarm window, the SSPS GW alarm and non-urgent alarm circuit inputs share common outputs, and any subsequent input condition is not alarmed, consistent with the current GW alarm (no reflash).

[

]^{a,c}

4.4 QUALIFICATION OF NON-URGENT ALARM CIRCUIT PARTS

The GWACM will use only parts that are qualified as Class 1E safety-related for implementation within the SSPS.

The SSPS is a Class 1E safety-related system; therefore, only safety or safety-related parts that have been qualified can be used.

4.5 PCB CONFIGURATION REQUIREMENTS

The GWACM will be implemented with a new design SSPS SAT, ULB, UVD, and SGD PCB in each SSPS train.

The new design SAT PCB must be configured and installed for separation and interface with the GW alarm and non-urgent alarm inputs and outputs as described in Section 5.1. New design SSPS ULB, UVD, and SGD PCBs must be installed and configured to provide a remote non-urgent alarm upon detecting either a WDE or E10 self-test error signal.

4.6 SSPS QUALIFICATION IMPACTS

The GWACM does not impact the equipment qualification of the SSPS. The PCB components are qualified as discussed in WCAP-17867-P-A (Reference 9) and the master and slave relay qualifications are not impacted by this change.

4.7 SSPS RESPONSE TIME IMPACTS

The GWACM does not impact response time requirements as documented in WCAP-14036-P-A (Reference 8) and WCAP-17867-P-A. The GWACM configuration change to the new design PCBs does not affect the PCB response time.

The response time of SSPS components used to process RTS and ESFAS signals is bounded by time response allocations and requirements contained in WCAP-14036-P-A.

4.8 RTS AND ESFAS IMPACTS

The GWACM does not impact the RTS or ESFAS functions provided by the SSPS. The non-urgent alarm circuitry change does not interface with the ESFAS or RTS signals.

5 GENERIC MODIFICATION DETAILS

The following section presents generic modification details for the 3-bay SSPS GWACM. The specific wiring locations, wiring removal, and wiring installation will be confirmed on a plant-specific basis.

5.1 SIMPLIFIED SCHEMATIC DIAGRAMS

Figure 5-1 provides a simplified schematic diagram of the current General Warning Alarm Circuitry (GWAC). Figure 5-2 provides a simplified schematic diagram of the GWAC with the modification installed.

Figure 5-1. GWAC Simplified Current Schematic (Typical)

a,c

Figure 5-2. GWACM Simplified Schematic (Typical)

The GWACM design implements a non-urgent alarm from any one of the inputs listed in Section 4.1 and eliminates the partial reactor trip for these functions. When a non-urgent alarm is generated by the SAT as depicted in Figure 5-2, an audible and visual MCB SSPS non-urgent alarm will be initiated. The non-urgent alarm may also be initiated by the multiplexer test switch when it is out of the "NORMAL" or "A+B" position. [

]^{a,c}

5.2 NEW DESIGN PCBS TO BE INSTALLED

Table 5-1 provides a listing of the new design SSPS PCBs to be installed. Replace all current design SSPS ULB, SGD, UVD, and SAT PCBs with the new design PCB type and groups as specified in Table 5-2. All SSPS ULB, SGD, UVD, and SAT PCBs in both SSPS trains must be new design PCB types. For plants with the new design SSPS PCBs currently installed, the SSPS ULB, SGD, UVD, and SAT PCB jumpers must be configured for the groups identified in Table 5-1.

Table 5-1 New Design SSPS PCBs

PCB	Description
6D30225G02	Universal Logic Board with E10 Interlock
6D30252G03(1)	Safeguards Driver Board with E10 Interlock
6D30350G02	Under Voltage Driver Board with E10 Interlock
6D30520G03(2)	Semi-Automatic Tester Board with Non-Urgent Alarm for Pulled Card Interlock Rows 2 – 5 and Power Supply Failure

Notes:
1. 6D30252G04 for plants that use 6D30252G02
2. 6D30520G04 for three-train SSPS only

Figures 5-3 through 5-8 show the SSPS ULB, SGD, and UVD PCBs before and after the GWACM. Figure 5-9 shows the configuration switch on the SAT PCB.

a,c

Figure 5-3. Universal Logic Board Before GWACM

a,c

Figure 5-4. Universal Logic Board After GWACM

a,c

Figure 5-5. Safeguards Driver Board Before GWACM

a,c

Figure 5-6. Safeguards Driver Board After GWACM

a,c

Figure 5-7. Under Voltage Driver Board Before GWACM

a,c

Figure 5-8. Under Voltage Driver Board After GWACM

a,c

Figure 5-9. Semi-Automatic Tester Board Configuration Switch

5.3 NON-URGENT ALARM MAIN CONTROL BOARD ANNUNCIATOR WINDOW

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]^{a,c} The design for the MCB annunciator can be implemented via the use of a separate annunciator window, or to parallel the signal with an existing annunciator window.

The field cable must be routed from each SSPS output relay cabinet (SSPS Trains A & B) to the MCB annunciator system.

5.4 OTHER CONSIDERATIONS FOR THE GWACM IMPLEMENTATION

5.4.1 MASTER RELAY

[ ]^{a,c}

5.4.2 Slave Relay

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]^{a,c}

5.4.3 4-Bay SSPS General Warning Alarm Circuit

The 4-bay SSPS has different circuitry for the GW alarm than depicted in Figure 5-1 and Figure 5-2. The implementation of the non-urgent alarm circuitry is not impacted by the design difference in the 4-bay SSPS GW alarm circuitry.

5.4.4 Three-Train SSPS Alarm Circuit Design

The three-train SSPS has an existing non-urgent alarm for the loss of a single 15V or 48V power supply. The implementation of the non-urgent alarm for the pulled card interlock and E10 self-test error requires a modification to the current non-urgent alarm circuitry.

a,c

Figure 5-10. SSPS Three Train Non-Urgent Alarm Excerpt

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]a,c

5.5 GWACM QUALIFICATION

The qualification for the new design SSPS PCBs included environmental and seismic testing.

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]a,c

6 POST–MODIFICATION TESTING

A functional test of each non-urgent alarm input signal will be performed after the GWACM modification is installed. The E10 self-test failure on each of the SSPS ULB, SGD, and UVD PCBs will be tested. The acceptance criteria are as follows:

- Each input signal must initiate the non-urgent alarm.
- No partial reactor trip signal will be initiated in the SSPS train being tested.

Perform a functional test of the GW alarm input signals. The acceptance criterion is:

- Each input signal must initiate a GW alarm with a partial reactor trip signal in the SSPS train being tested.

7 FAILURE MODES EVALUATION

Plant reliability can be improved by minimizing the potential of inadvertent reactor trips associated with the SSPS GW alarm. Plant safety can be improved by maximizing the SSPS availability via the new design SSPS ULB, SGD, and UVD PCBs that will immediately alert the operator with an audible and visual MCB alarm if an SSPS PCB fails a self-test, as opposed to being identified when the next surveillance test is performed to identify a degraded SSPS ULB, SGD, or UVD PCB.

7.1 IDENTIFICATION OF NEW FAILURE MODES

The failure modes and effects analyses (FMEAs) that were performed on the new design SSPS PCBs in identify the WCAP confirmed that the FMEA that was performed for the SSPS that is contained in WCAP-7706, remains valid. The new design SSPS ULB, SGD, and UVD PCB failure modes are the same as the original design SSPS ULB, SGD, and UVD PCBs. The similarity of the FMEA results for the new design SSPS ULB, SGD, and UVD PCBs when compared to the original design SSPS ULB, SGD, and UVD PCBs confirmed that there will be no malfunctions of an SSC important to safety with a different result than any previously evaluated in the Updated Final Safety Analysis Report (UFSAR).

Table 7-1 provides a summary of the current GW alarm design functions, the GWACM changes, and identifies those functions that are discussed in WCAP-7488-L and WCAP-7706 (References 3 and 4). The new design SSPS ULB, SGD, and UVD PCB self-test error is also included.

WCAP-7672 Section III.D, "Alarm System" states:

"*If trouble in both trains should develop simultaneously, the reactor will be tripped automatically by the alarm system.*"

Implementation of the GWACM will remove the GW alarm partial reactor trip inputs that are shown in Figure 4-1. Therefore, the changes to the SSPS GW alarm failure modes are identified in Table 7-1.

Table 7-1 General Warning Alarm Summary of Proposed Changes

General Warning (GW) Alarm			GW Alarm Function Discussed in WCAP-7488-L	GW Alarm Function Discussed in the SSPS FMEA	
Functions	**Current Design**	**GWACM Design**		**WCAP-7706**	**Description**
Input Error Inhibit Switch in "INHIBIT"	General Warning with Partial Trip	General Warning with Partial Trip	Yes	Yes	Input Error Inhibit Switch S1, Fuse FU1 (continuously monitored with open circuit alarm and trip)
Logic Test Switch A not in "OFF"	General Warning with Partial Trip	General Warning with Partial Trip	Yes	No	
Memories Test Switch not in "OFF"	General Warning with Partial Trip	General Warning with Partial Trip	Yes	No	
Permissive Test Switch not in "OFF"	General Warning with Partial Trip	General Warning with Partial Trip	Yes	No	
Output Mode Selector Switch in "TEST"	General Warning with Partial Trip	General Warning with Partial Trip	Yes	No	
Loss of 118Vac Output Relay Power (not all plants have this feature)	General Warning with Partial Trip	General Warning with Partial Trip	Yes	No	
Reactor Trip Bypass Breaker racked-in and closed.	General Warning with Partial Trip	General Warning with Partial Trip	Yes	No	
Pulled card interlock (Row 1)	General Warning with Partial Trip	General Warning with Partial Trip	Yes	Yes	The improper insertion of any CCB, DEC, or SAT PCB, one in each SSPS logic train, will generate a reactor trip signal.
Loss of one 48 V power supply	General Warning with Partial Trip	**Non-Urgent Alarm - no partial trip**	Yes	No	
Loss of one 15V power supply	General Warning with Partial Trip	**Non-Urgent Alarm - no partial trip**	Yes	No	
Multiplexer Test Switch to Inhibit	General Warning with Partial Trip	**Non-Urgent Alarm - no partial trip**	Yes	No	
Pulled card interlock (Rows 2-5)	General Warning with Partial Trip	**Non-Urgent Alarm - no partial trip**	Yes	Yes	
Self-Test Error (E10 or WDE)	None	**Non-Urgent Alarm - no partial trip**	No	No	N/A

7.2 GWACM FAILURE EVALUATION

A failure modes and effects analysis was performed for the GWACM as shown in Table 7-2.

A traditional FMEA uses a weight rating that is based on multiplying the criticality (C), likelihood (L), and detectability (D) rankings together, with larger values normally used to indicate more critical failure modes. The combination of criticality and likelihood offers provides insight into the component's impact on the mission if it failed or was at risk. The combination of likelihood and detectability provides insight to the component's need for monitoring, inspection, or testing. This combination offers insight into the surveillance test frequency and other maintenance considerations. For the GWACM, all failures will be considered equal for the purpose of SSPS alarm response and diagnostics.

The multiplexer test switch to generate an inhibit position alarm is not a component failure; therefore, it is not included in Table 7-2. The multiplexer test switch inhibited alarm provides indication when one SSPS train is in test to prevent spurious alarms to the operator; while the opposite SSPS train provides indication during testing. Multiplexing is a non-safety-related function; therefore a partial reactor trip is not needed for the multiplexer test switch to generate an inhibit position alarm.

The loss of a redundant power supply does not affect an SSPS train's operability; therefore, a partial reactor trip is not needed. Also, note that a failure of both of the 15V or both of the 48V power supplies in an SSPS train causes a reactor trip; therefore, a second power supply failure is fail-safe.

The pulled-card interlock alarm is administratively controlled by limiting access to the SSPS train cabinets. Verification that the SSPS ULB, SGD, and UVD PCBs remain inserted is self-evident by the absence of an alarm from the pulled card interlock circuit. A non-urgent alarm condition will occur when a PCB is pulled, or not fully inserted for card interlock Rows 2-5. PCB insertion is confirmed prior to securing each SSPS train cabinet, by confirming there is no SSPS GW or non-urgent alarm condition.

The addition of a PCB self-test failure indication to the non-urgent alarm ensures that PCB failures are immediately detectable. Determination of the non-urgent alarm cause would require observation of local status indications at the affected SSPS logic cabinet. Response to the non-urgent alarm will be the same as the response to the receipt of the current GW Alarm. Therefore, the change in human-system interface from the GWACM would require a change to the SSPS alarm response procedure for operators to respond to an SSPS non-urgent alarm condition to determine if a loss of safety function has occurred in the affected SSPS train. Only after the cause of the non-urgent alarm has been determined, can an assessment be made regarding the affected SSPS train's operability.

Table 7-2 SSPS General Warning Alarm Circuit Modification FMEA Impacts

Failure	Symptoms/ Local Effects in the Affected SSPS Train	Mitigating Features	System Effects	Method of Detection
Failure of one 48 VDC power Supply	Loss of Power	Redundant power supply	None	Non-Urgent Alarm
Failure of one 15 VDC power Supply	Loss of Power	Redundant power supply	None	Non-Urgent Alarm
Failure of SSPS UVD, ULB, SGD PCB self-test	Failure of the module (PCB), potential loss of safety function	Opposite SSPS Train	Capability to perform the safety function is maintained by the redundant train.	Non-Urgent Alarm
Pulled Card Interlock Rows 2-5	Failure of the module (PCB), potential loss of safety function	Opposite SSPS Train	Capability to perform the safety function is maintained by the redundant train.	Non-Urgent Alarm

8 NEW DESIGN SSPS PCB OPERATION AND TESTING

The operation and testing of the new design SSPS PCBs is described in WCAP-17867-P-A. Implementation of the GWACM enables the SSPS self-test feature on the SSPS ULB, SGD, and UVD PCBs to activate a new non-urgent alarm on the MCB. [

]^{a,c} The only operational change to the new design PCBs associated with the GWACM is the external (jumper and switch) alarm circuit configuration that will provide a remote non-urgent alarm on the MCB. No changes are required to the SSPS ULB, SGD, UVD, and SAT PCB design to implement the GWACM.

9 ASSESSMENT OF REGULATORY REQUIREMENTS GUIDANCE AND INDUSTRY STANDARDS

WCAP-17867-P-A provides a cross-reference between the regulatory requirements, selected guidelines, and Industry Standards identified in NUREG-0800 Chapter 7, Table 7-1 (Reference 10), that are applicable to the new design SSPS PCBs. WCAP-17867-P-A identifies the applicable regulation, guidance or Industry Standard, whether the SSPS new design SSPS PCB changes are in compliance, in partial compliance, or not in compliance, and the basis for non-compliance. The topical report sections and/or external references that provide information supporting the new design SSPS PCB compliance with each regulation and guideline are also listed.

Many of the regulatory requirements, selected guidelines, and Industry Standards listed in WCAP-17867-P-A apply on a system level. The new design SSPS PCBs were designed to maintain the current SSPS design and licensing basis so that installation of the new design PCBs has no impact on the SSPS' ability to perform its safety functions. The original design SSPS was designed to IEEE Std. 279-1971 (Reference 11). The new design SSPS PCBs comply with IEEE Std. 603-1991 (Reference 12). The SSPS GWACM does not impact the new design SSPS PCB design and licensing basis.

Aside from the new design SSPS PCBs, the components used in the implementation of the GWACM are not digital and do not contain any programmable devices. The design of the SSPS ULB, SGD, UVD, and SAT PCBs has not changed from the design that was approved by the NRC in WCAP-17867-P-A. The self-test function existed on the PCBs that were approved in WCAP-17867-P-A and the regulatory requirements, selected guidelines, and Industry Standards for these PCBs were addressed in WCAP-17867-P-A. [

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10 SUMMARY AND CONCLUSIONS

Implementation of the GWACM improves plant reliability by minimizing the potential for inadvertent plant reactor trips associated with the SSPS GW alarm. The inputs removed from the GW alarm will be moved to a new non-urgent alarm that does not cause a reactor trip signal in the affected SSPS train. Plant safety will also be improved by maximizing SSPS availability via the new non-urgent alarm to immediately alert the operator if an SSPS PCB fails a self-test. The addition of a new non-urgent alarm will allow plants to enable the new design SSPS PCB self-test function to provide remote indication of a self-test alarm condition on the MCB. The GWACM will alert the operator with an audible and visual MCB alarm if an SSPS PCB fails a self-test, as opposed to being identified when the next surveillance test is performed to identify a degraded SSPS ULB, SGD, or UVD PCB.

The GWACM involves reducing the number of inputs to the SSPS GW alarm circuit by removing the loss of one 15 VDC power supply, the loss of one 48 VDC power supply, the multiplexer test switch selected to the "Inhibit" position, and the pulled card interlock. These inputs will be moved to a new non-urgent alarm. The non-urgent alarm will interface with the MCB annunciator system to indicate using a separate alarm window or a shared with a GW alarm window for each SSPS train. The reduction of inputs to the SSPS GW alarm will reduce the likelihood of inadvertent reactor trips while maintaining plant safety with the remaining inputs to the GW alarm that will provide input for a partial reactor trip signal as originally designed.

The GWACM also enables the non-urgent alarm to indicate if a new design SSPS PCB failed a self-test. The new design SSPS ULB, SGD, and UVD PCBs all contain built in self-test features, including a self-test function that continuously tests the functions of the PCB's basic logic and output drivers. Protection channel trips and actuation signals received during the performance of self-test processes will result in a reactor trip or ESFAS actuation, when required, as originally designed. The SSPS PCB self-test feature does not impact the Technical Specification SSPS surveillance tests or impact the SSPS protection functions. The self-test feature provides early detection of a potential component failure, including logic operation and input power failure. The continuous PCB self-tests on the SSPS ULB, SGD, and UVD PCBs are designed to facilitate timely recognition and identification of equipment that is not performing as designed, so that maintenance can be performed. The addition of LED indications on the visible card edge of the new design SSPS PCBs provide signal status information that is not available on the original design SSPS PCBs. These features, in conjunction with the GWACM, will alert the operator with an audible and visual MCB alarm if an SSPS PCB fails a self-test, as opposed to being identified when the next surveillance test is performed to identify a degraded SSPS ULB, SGD, or UVD PCB.

11 REFERENCES

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Approval Information

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Manager Approval Ackman Mark E Jan-24-2018 07:13:38
Manager Approval Holderbaum Chad M Jan-24-2018 11:52:01

Files approved on Jan-24-2018