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SUBJECT: Forwards addl info re isolation devices for SPDS, per NRC 860110 request.

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Arizona Nuclear Power Project
P.O. BOX 52034 • PHOENIX, ARIZONA 85072-2034

March 14, 1986
ANPP-35548 EEVB/JKO/98.05

Director of Nuclear Reactor Regulation
Attention: Mr. George W. Knighton, Project Director
PWR Project Directorate #7
Division of Pressurized Water Reactor Licensing - B
U.S. Nuclear Regulatory Commission
Washington, D.C. 20555

Subject: Palo Verde Nuclear Generating Station (PVNGS)
Units 1, 2 and 3
Docket Nos. STN 50-528 (License NPF-41)
STN 50-529 (License NPF-46)
STN 50-530
Additional Information Concerning Palo Verde
Safety Parameter Display System (SPDS)
File: 86-056-026; J.9.02

Reference: Letter dated January 10, 1986, from E. A. Licitra, NRC, to E. E. Van Brunt, Jr., ANPP. Subject: Request for Additional Information - Palo Verde Safety Parameter Display System.

Dear Mr. Knighton:

In the referenced letter, you requested additional information concerning the isolation devices for the SPDS. Attached is the requested information for your review.

If you have any further questions regarding this matter, please contact Mr. W. F. Quinn of my staff.

Very truly yours,

E. E. Van Brunt

E. E. Van Brunt, Jr.
Executive Vice President
Project Director

EEVB/JKO/rw

cc: E. A. Licitra
A. C. Gehr
R. P. Zimmerman

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ATTACHMENT

(1) NRC Question

For each type of device used to accomplish electrical isolation describe the specific testing performed to demonstrate that the device is acceptable for its application(s). This description should include elementary diagrams where necessary to indicate the test configuration and how the maximum credible faults were applied to the devices.

Response

Two types of devices are used at PVNGS to accomplish electrical isolation, as given below:

(a) Class 1E Analog Isolation Amplifier Card

The Class 1E analog plant isolation amplifier card performs two functions: (1) isolating the Class 1E input signals from the Emergency Response Facility Data Acquisition and Display System (ERFDADS) (SPDS) Data Acquisition System (DAS) and (2) provide amplification or signal conditioning for the ERFDADS (SPDS). Each isolation card is comprised of four isolation amplifiers.

Isolation between inputs and outputs on the printed circuit cards is provided by a physical separation of input and output circuitry and a Burr-Brown isolation amplifier. The Burr-Brown isolation amplifier is an integrated circuit-transformer coupled isolation amplifier which has a continuous isolation rating of 3500 volts dc and 2000 volts ac RMS.

To verify the isolation capability of the Class 1E Analog isolation amplifier, a hipot test and a Surge Withstand Capability (SWC) test were performed.

The hipot test consisted of applying a test signal of 3000 volts peak voltage dc to 12 randomly selected analog amplifier isolation cards.

To perform the hipot test, the hipot tester and the associated cabling were connected to an individual test channel as shown on Figure 1. Once the test channel was set up, the 15 volt power supply was turned on. The voltage applied to the test channel input was then gradually increased, observing the hipot tester ammeter readings and stopped when 3000 volts was reached or the test channel failed. Zero leakage current across the 1E side and non-1E side at 3000 volts was the criteria for passing the hipot test. These steps were repeated for all 4 channels on all 12 tested cards.

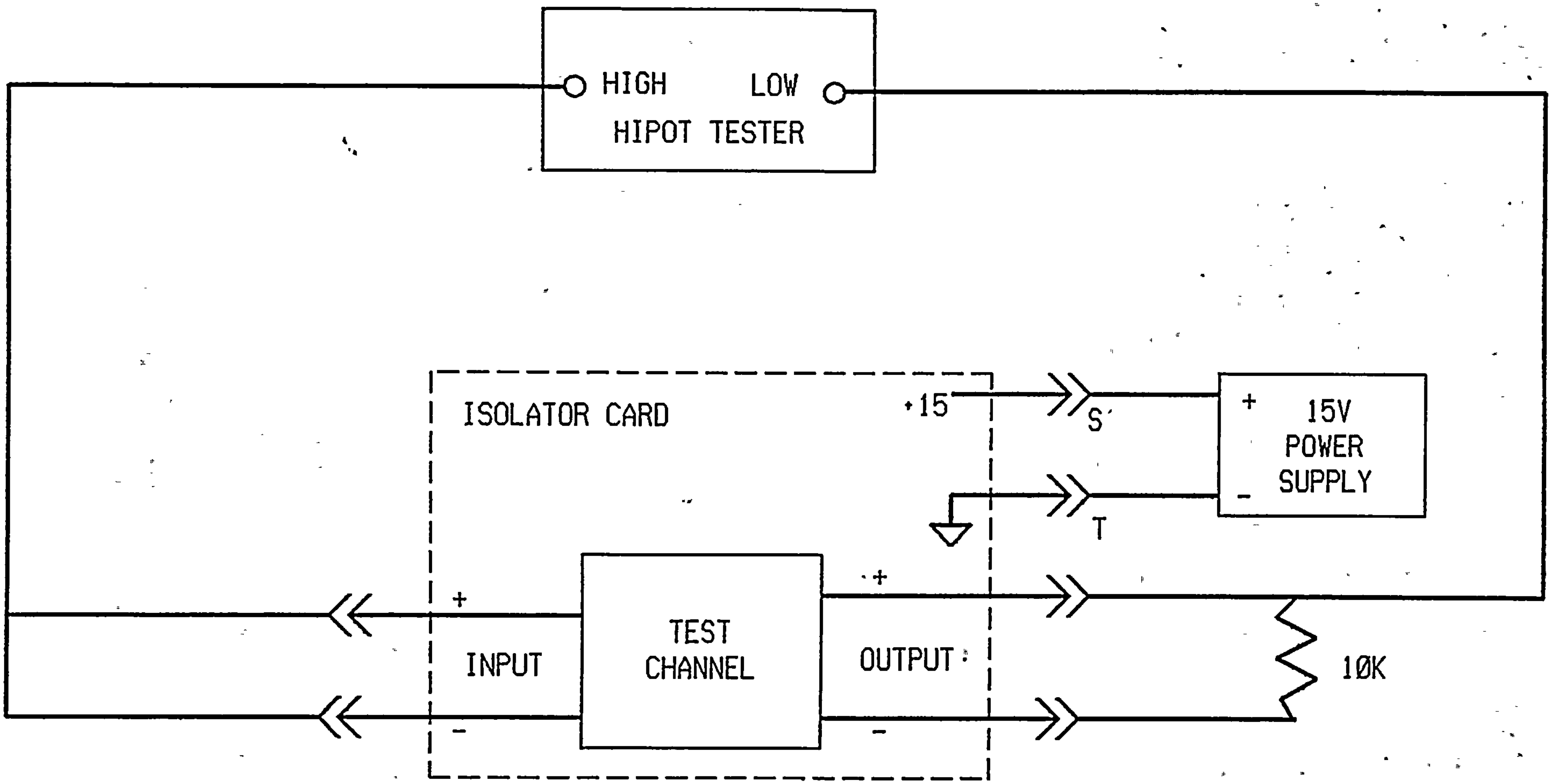


FIGURE 1
TYPICAL CHANNEL TEST CONFIGURATION
FOR
CLASS 1E ANALOG ISOLATION AMPLIFIER TEST

Since transient voltages usually are capacitively or magnetically coupled from a high voltage source of electrical noise into secondary circuits or control wiring, a Surge Withstand Capability (SWC) test was also performed on 8 randomly selected Class 1E analog isolation amplifier cards. The intent of this test was to demonstrate that unsuppressed transient voltages would not appear and cause a failure or a misoperation of system components associated with the Class 1E side.

To verify the SWC of the analog isolation device, the testing was performed to guidance provided in ANSI/IEEE C37 90A-1974, "Guide for Surge Withstand Capability (SWC) Test."

First, a functional test was performed to obtain a pre-SWC test voltage baseline. This functional test was connected using the configuration shown on Figure 2. The pre-SWC test results were documented in the test procedure and later used to determine failure of a test channel.

For testing the test channel for transverse mode SWC and common mode SWC, the Figure 3 and Figure 4 configurations were set-up, respectively. A test wave form of 2500 volts AC peak voltage with a 1.0 to 1.5 MHz frequency was applied. This SWC oscillatory wave shape was composed at a first half cycle of full peak voltage, then decaying the envelope to 50% of the crest value of the first peak in not less than six microseconds from the start of the wave between the high and low input leads (transverse mode and also from input-to-output with capacitive coupling on the inputs common mode) was applied. This test wave was applied to the test channel at a repetitive rate of not less than 50 times per second for a period of not less than two seconds.

Upon completion of testing the test channel for transverse mode SWC and common mode SWC for each test channel of the 8 selected cards, a post-SWC functional test (Figure 2) was repeated for all 8 selected channels to determine any failure of the test channel.

The failure of a test channel was defined as any isolation amplifier output (post-SWC) failing to return to within 1% of the pre-SWC voltage baseline. Results for the post-SWC test have been documented in the test procedure along with the pre-SWC test results. The SWC test results indicate that the analog isolation amplifier devices are acceptable for common mode and transverse mode SWC.

(b) Class 1E Digital Isolation Card

Each of the digital isolation cards are comprised of 8 isolation channels. These cards performs the function of isolating the plant Class 1E signals and the ERFDADS (SPDS) Data Acquisition System (DAS).

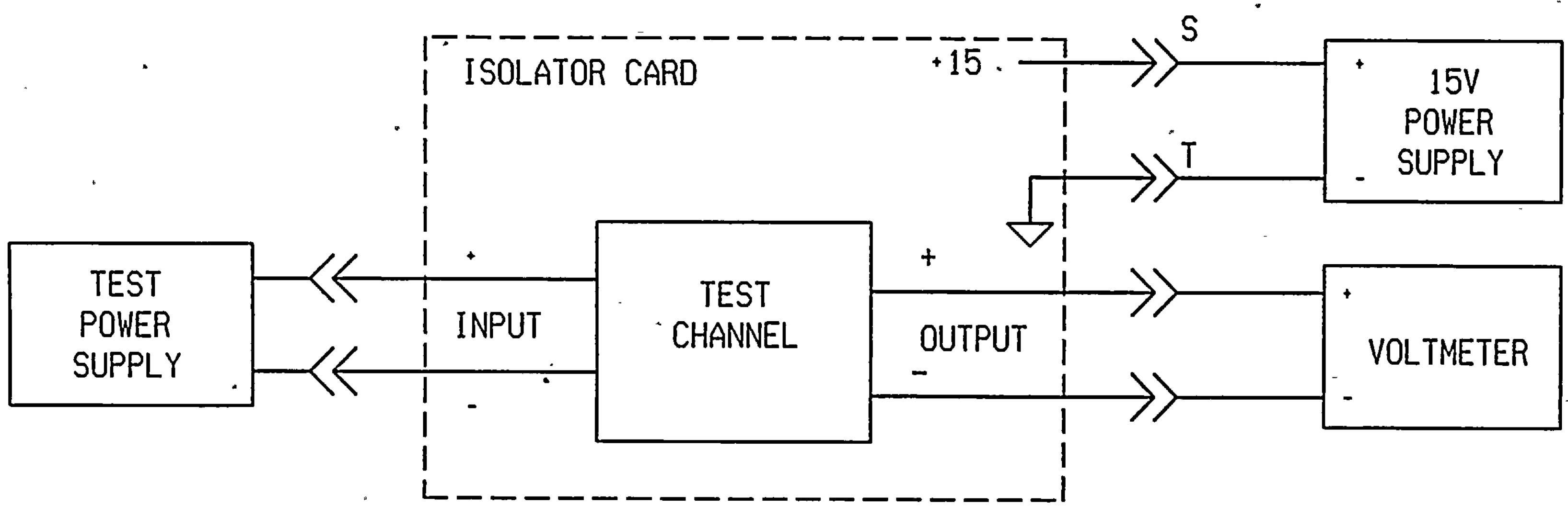


FIGURE 2
TYPICAL TEST CHANNEL CONFIGURATION
FOR SWC FUNCTIONAL TEST

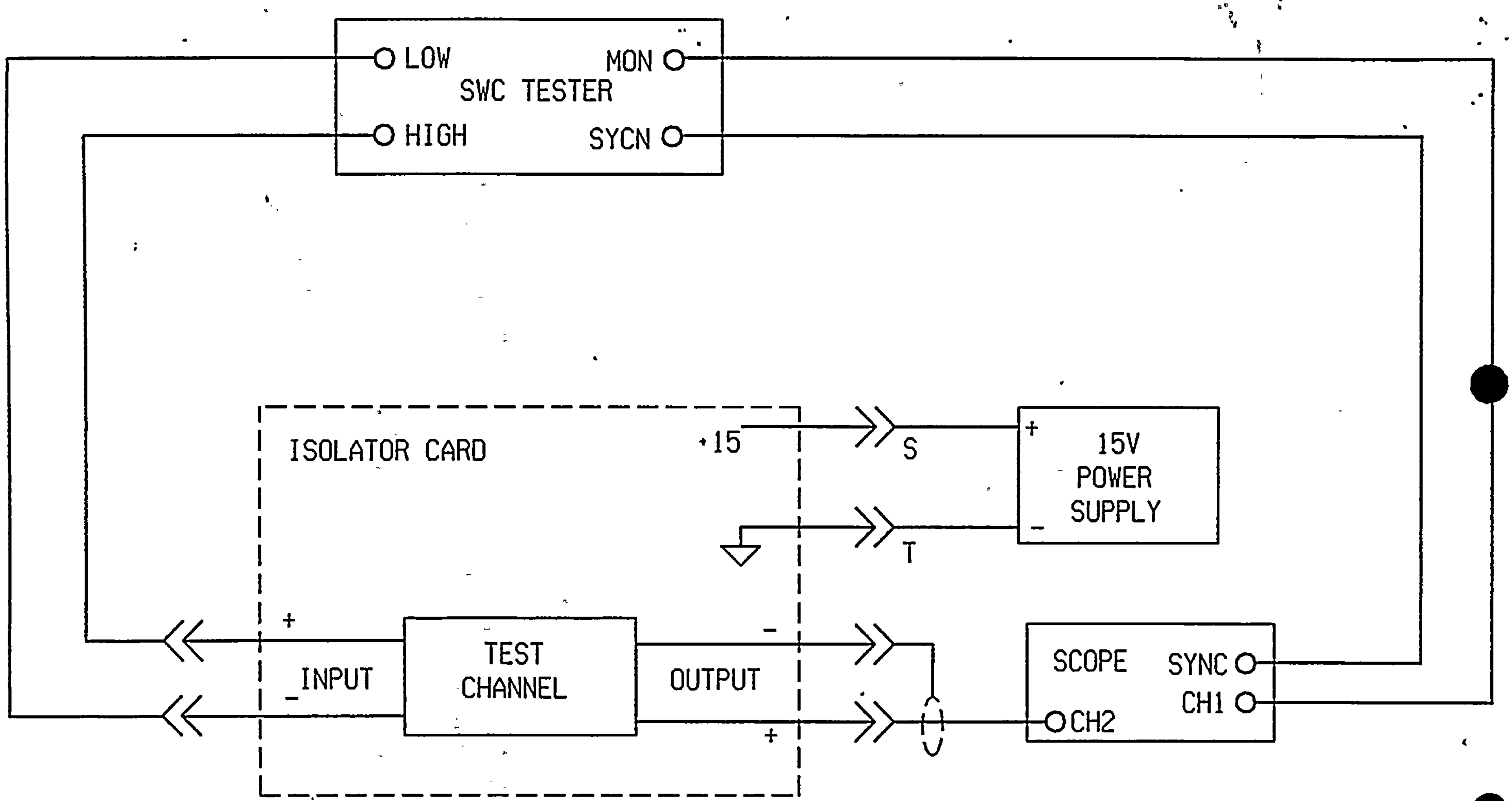
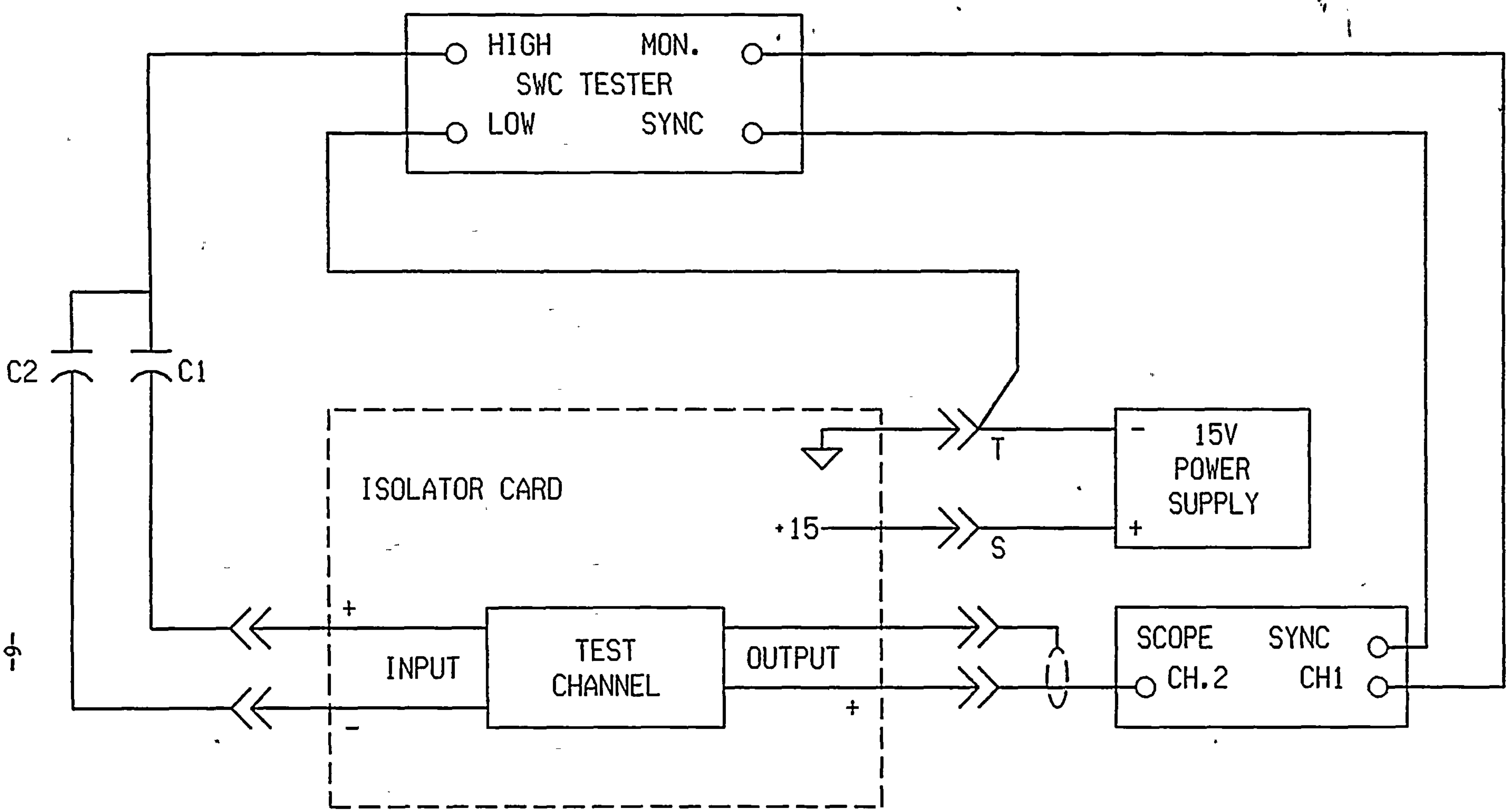


FIGURE 3
TYPICAL CHANNEL TEST CONFIGURATION
FOR TRAVERSE MODE SWC TEST



<u>FIGURE 4</u>
TYPICAL CHANNEL TEST CONFIGURATION
FOR COMMON MODE SWC TEST

Isolation between inputs and outputs of the printed circuit card is provided by physical separation of the input and output circuitry and the Hewlett Packard optoisolator model 4N46.

In verifying the isolation capability of the Class 1E digital optoisolator, a hipot test and a surge withstand capability test were performed.

The hipot test consisted of applying a test signal of 3000 volts peak voltage dc to 12 randomly selected digital isolation cards.

During the pretest setup for the hipot test, the hipot tester and associated cabling were connected to an individual test channel as shown on Figure 5. The high voltage lead of the hipot tester was connected to the test channel input terminals and the hipot ground post to the test channel output terminal. A 5 volt power supply was connected with the (+) to the terminal U and (-) to terminal V of the test channel.

While performing the test, the 5 volt power supply is turned on. The hipot voltage is then raised from 0 volts to 3000 volts or until the isolator channel breaks down. The maximum leakage current was then recorded for each tested channel of all 8 selected digital isolation cards.

To verify the SWC of the digital isolator, the testing was performed to guidance provided in ANSI/IEEE C37, 90A-1974, "Guide for Surge Withstand Capability (SWC) Tests."

Prior to performing the transverse mode SWC test and common mode SWC test a functional test as connected as shown on Figure 6 was performed. The purpose of this functional test was to determine a baseline to which the digital isolator test channel would be compared after the transverse mode SWC and common mode SWC test to determine if the card has been damaged. Results of this pre-SWC test were documented in the test procedure.

During the pretest setup for both the transverse mode SWC test and common mode SWC test of the digital isolator, the Figure 7 and Figure 8 configurations were connected, respectively.

In performing the transverse mode and common mode SWC tests a 2500 volts AC peak voltage and 1.0 to 1.5 MHz frequency were used as test signals. The first half of the test signal cycle is full peak voltage, then its envelope decays to 50% of the crest value of the first peak in not less than six microseconds from the start of the wave. This test wave was applied to the test channel at a repetitive rate of not less than 50 times per second for a period of not less than two seconds using a source impedance of 150 ohms.

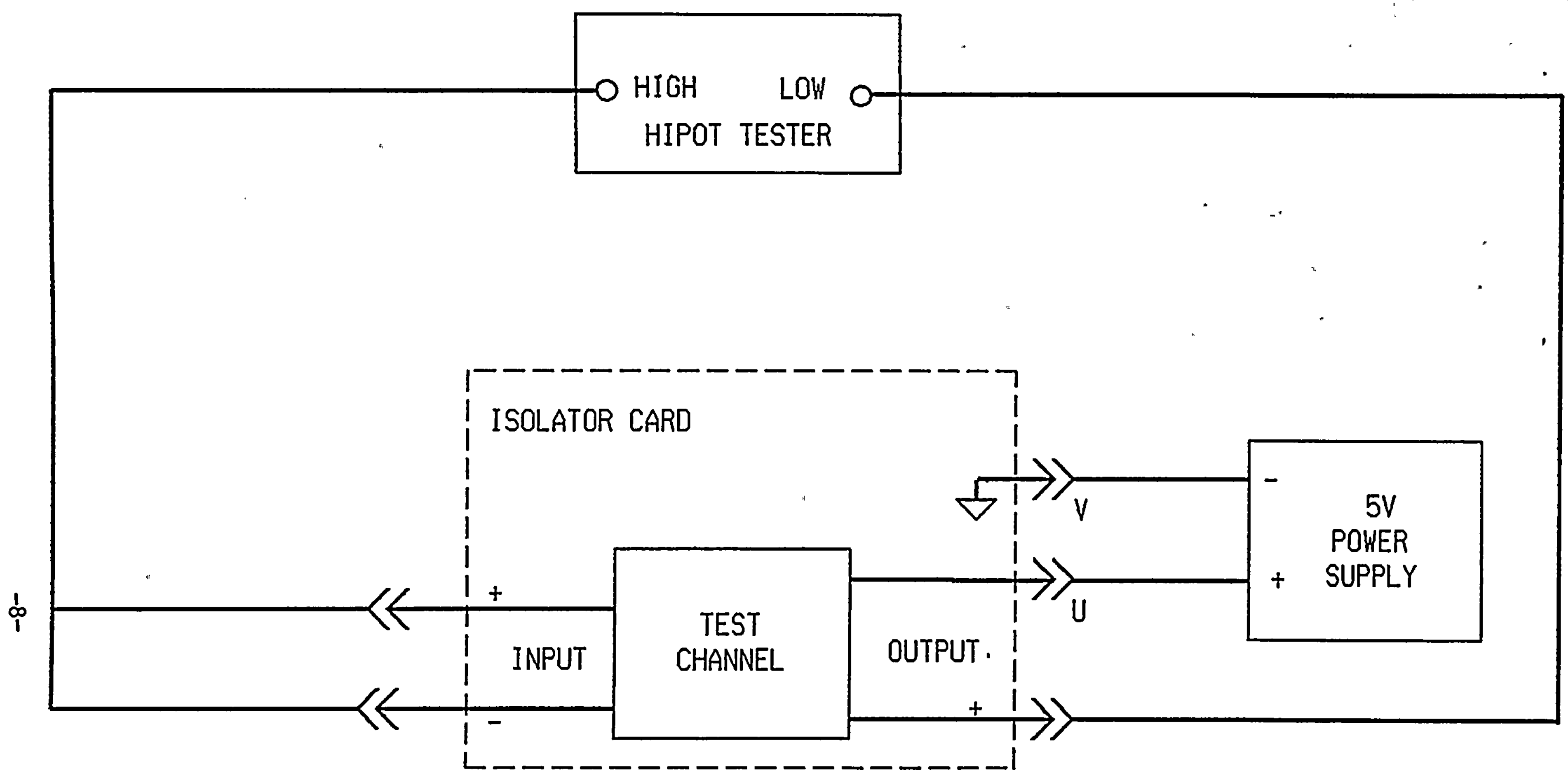


FIGURE 5
TYPICAL TEST CHANNEL CONFIGURATION
FOR
CLASS 1E DIGITAL ISOLATOR TEST

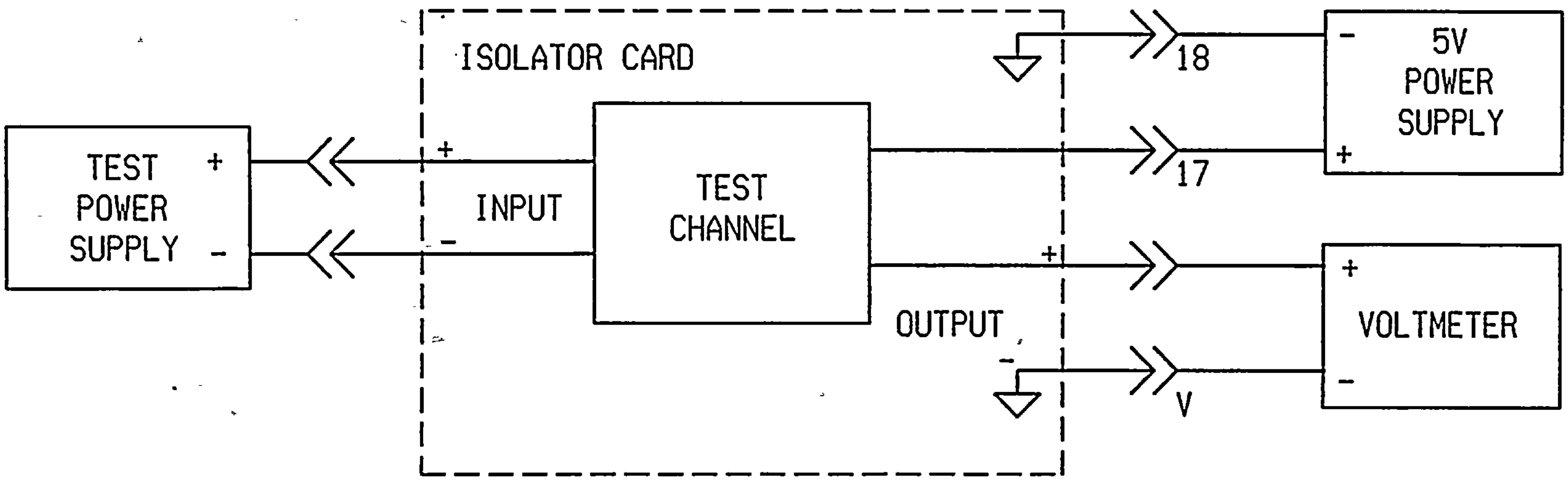


FIGURE 6
TYPICAL CHANNEL TEST CONFIGURATION
FOR SWC FUNCTIONAL TEST

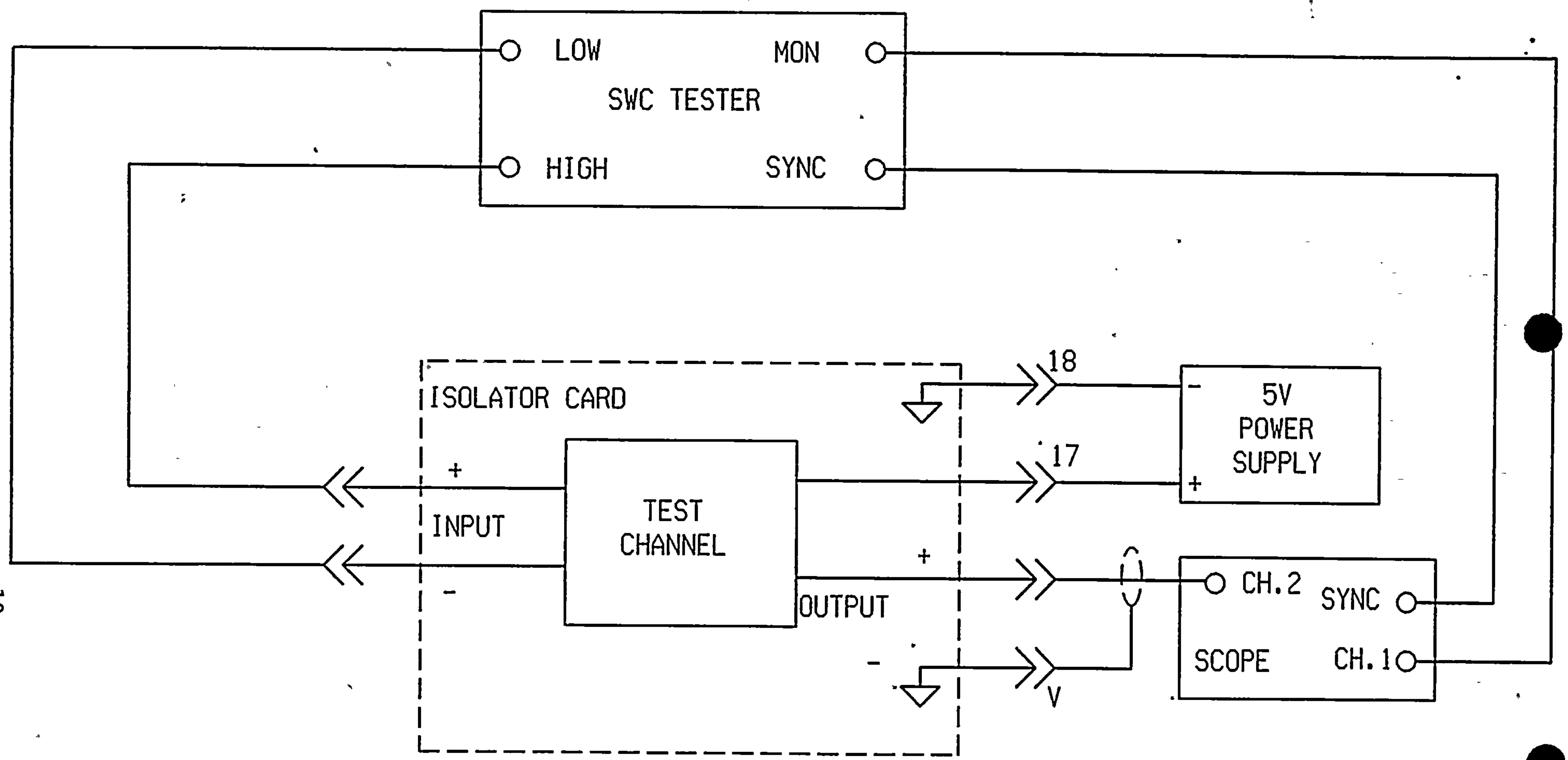


FIGURE 7
TYPICAL CHANNEL TEST CONFIGURATION
FOR TRANSVERSE MODE SWC TEST

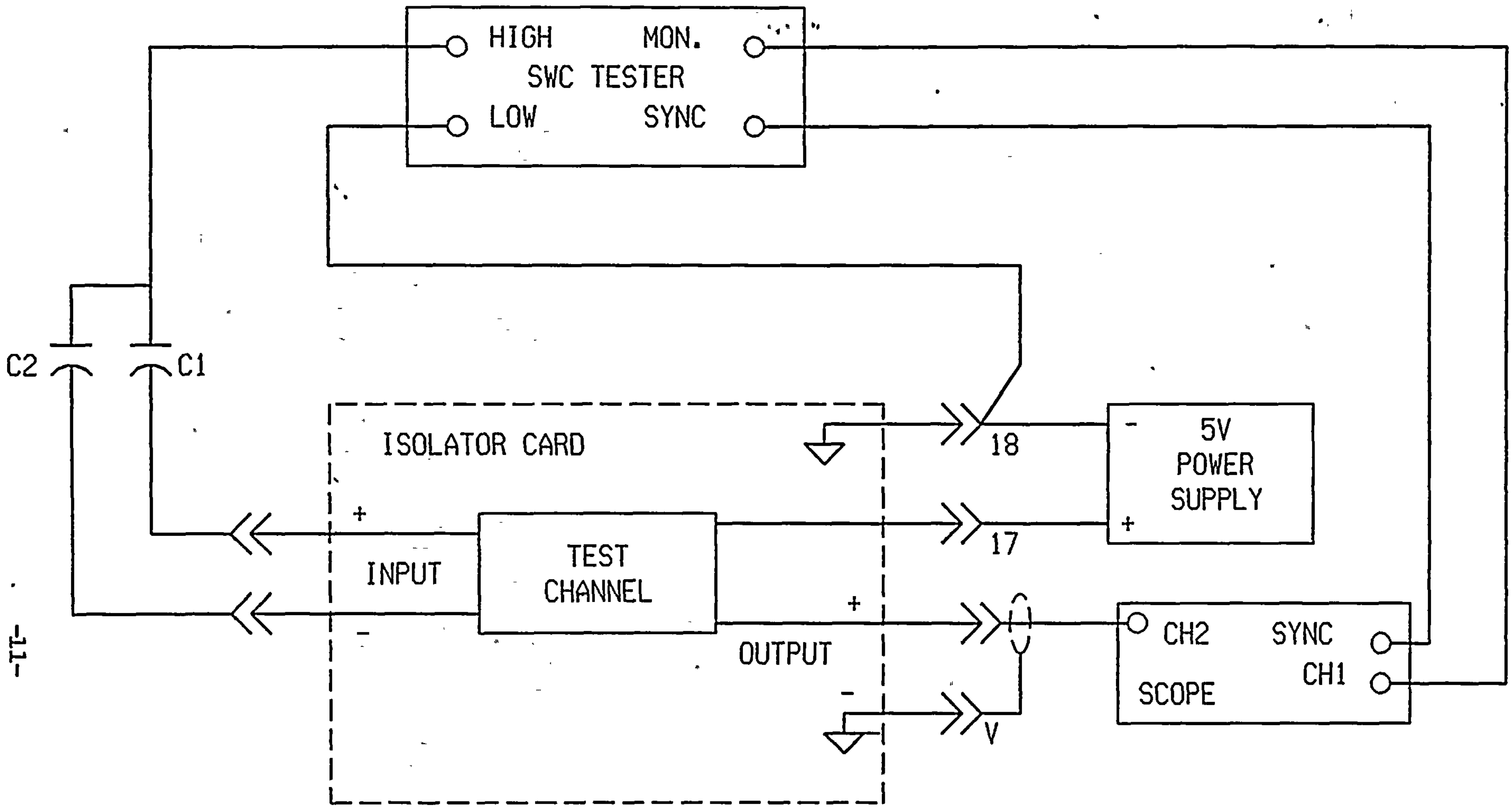


FIGURE 8
TYPICAL CHANNEL TESTCONFIGURATION
FOR COMMON MODE SWC TEST

Upon completion of the above testing, the test channel was subjected to a post-SWC functional test. Results of this post-SWC testing were compared to the pre-SWC test results. This comparison indicates that the digital isolation devices are acceptable for transverse mode and common mode SWC.

(2) NRC Question

Provide data to verify that the maximum credible faults applied during the test were the maximum voltage/current to which the device could be exposed, and define how the maximum voltage/current was determined.

Response

The maximum voltage was defined by determining the highest potential that the non-1E side of the isolators would see in case of an accident.

The highest voltage feeding the ERFDADS (SPDS) isolation cabinets J-SDA-C05, J-SAC-C05, J-SDCB-C06, and J-SDD-C06 is 120 VAC used for the 48 V power supplies. In order to establish this maximum potential, two possible failures were considered; 1) that the cables feeding the isolation cabinets would run in the same tray or conduit as other cables carrying a higher potential such that a short between cables would induce the higher voltage on the isolators non-1E side; 2) the transformers at the 120 VAC distribution panel E-SDN-D03 feeding the isolator cabinets shorted such that the isolator non-1E side would see the higher potential feeding the transformers. It was found that only cables carrying 120 VAC run in the same conduit. Also there are no transformers only a breaker at the 120 VAC distribution panel E-SDN-D03. Failure of this breaker would induce the same potential, i.e., 120 VAC, on the isolator non-1E side. Therefore, the maximum credible fault voltage is 120 VAC $\pm$ 10%.

The isolation devices have been tested to 3,000 volts. The maximum credible fault voltage was exceeded during testing.

(3) NRC Question

Provide data to verify that the maximum credible fault was applied to the output of the device in the transverse mode (between signal and return) and that other faults were considered (i.e., open and short circuits).

Response

The digital and analog isolation devices use optical and transformer coupled components, respectively to provide a physical separation between the device input and output side. Based on this fact, an assumption was made that "the highest voltage to which the isolation device non-class 1E side is exposed would determine the minimum voltage level that the device shall withstand between input and output, and from these terminals to ground." Even though the testing of these isolation devices did not

apply a credible fault to the output of the isolation device in the traverse mode, these tests demonstrated that a credible fault on the non-1E side of the isolation device would not traverse to the 1E side. This was demonstrated by applying a differential voltage of 3,000 volts during the hipot test across the isolation device non-1E side and the 1E side with results yielding zero leakage current between the isolations device 1E side and non-1E side.

To supplement the testing performed above, the following circuit analysis was made for open and short circuits. An open circuit on the signal or return would have no affect on either the 1E or non-1E circuits. A short circuit between the signal and return/ground would have minimal effect. The circuits for both analog and digital cards have been designed with current limiting resistors. Under short circuit conditions the analog isolator current limiting resistor and the digital isolator current limiting resistor, would see small voltage levels thus having no affect on the devices' 1E side.

(4) NRC Question

Define the pass/fail acceptance criteria for each type of device.

Response

The pass/fail criteria applied during the isolation capability test was zero leakage current between the isolation device 1E side and non-1E side. (See testing described in Question 1).

(5) NRC Question

Confirm that the isolation devices comply with the environmental qualifications (10 CFR 50.49) and with the seismic qualifications which were the basis for plant licensing.

Response

Since the isolation devices are located in a mild environment, the devices are not required to comply with the environmental requirements of 10CFR 50.49. The isolation devices have been seismically qualified by performing tests and analysis on 12 analog and 12 digital isolation cards installed in an isolation cabinet.

(6) NRC Question

Provide a description of the measures taken to protect the safety systems from electrical interference (i.e., Electrostatic Coupling, EMI, Common Mode, and Crosstalk) that may be generated by the SPDS.

Response

As discussed above, the isolation devices have been demonstrated to provide the required electrical isolation between the plant 1E systems (safety systems) and ERFDADS (SPDS) non-1E Data Acquisition System (DAS). During the testing performed, the isolation devices were demonstrated to provide protection from electrostatic coupling and common mode during the surge withstand capability tests. To prevent crosstalk, the isolation cabinet circuitry has been physically separated to conform to IEEE 384-1981 criteria. In addition, fiber-optic links between the ERFDADS (SPDS) DAS and the host computer have been provided. The use of fiber-optic links eliminates noise problems associated with EMI/RFI.