SUPPLEMENTAL RESPONSE TO REQUEST FOR ADDITIONAL INFORMATION

APR1400 Design Certification

Korea Electric Power Corporation / Korea Hydro & Nuclear Power Co., LTD

Docket No. 52-046

RAI No.:	**274-8277**
SRP Section:	**7.1 - Instrumentation and Controls**
Application Section:	**7.1, 7.3, and 10.2**
Date of RAI Issue:	**10/27/2015**

Question No. 07.01-40

Clarify the terms used in APR1400 FSAR Tier 2, Table 7.2-7, “Failure Mode and Effects Analysis for the Plant Protection System,” Item 2-14, and clarify why an improper CEA position renders a CPC inoperable and changes the voting logic.

10 CFR 50.55a(h)(3) states, in part, that an application filed on or after May 13, 1999, for design certifications must meet the requirements for safety systems in IEEE Std. 603-1991 and the correction sheet dated January 30, 1995. Clause 5.1 of IEEE Std. 603-1991, states, in part, “The safety systems shall perform all safety functions required for a design basis event in the presence of: (1) any single detectable failure within the safety systems concurrent with all identifiable but non-detectable failures; (2) all failures caused by the single failure; and (3) all failures and spurious system actions that cause or are caused by the design basis event requiring the safety functions.

For the APR1400 FSAR Tier 2, Table 7.2-7, “Failure Mode and Effects Analysis for the Plant Protection System,” Item 2-14, Failure Mode Item b), identifies the following failure terms:

a. Unrecognized software malfunctions
b. Erroneous control element assembly (CEA) position transmission and indication
c. Improper CEA position

It is unclear to the staff what these terms mean with respect to the failure analysis. In addition, it is unclear to the staff how an improper CEA position renders a core protection calculator (CPC) channel inoperable and changes the logic to 2-out-of-2 coincidence. Describe and define the failure terms used: software malfunction, erroneous CEA position, erroneous CEA indication, and improper CEA position. In addition, clarify why an improper CEA position renders a CPC inoperable, and changes the logic to 2-outof- 2 coincidence (e.g. does the

voting logic change to 2-out-of-2). Provide diagrams regarding the operation of the CPCS in the APR1400 FSAR to support these clarifications.

Response

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Supplemental Response

The definitions of the different types of CPCS failures discussed in the response will be added to the APR1400 DCD Tier 2 as indicated in the attachment.

In addition, DCD Tier 2, Figure 7.2-4, “CEA Position Signal Flow for CPCS,” will be modified because it was missing a CPP output signal from the Channel D CPP1 module.

Impact on DCD

Table 7.2-7 and Figure 7.2-4 of DCD Tier 2 will be revised, as indicated in the attachment associated with this response.

Impact on PRA

There is no impact on the PRA.

Impact on Technical Specifications

There is no impact on the Technical Specifications.

Impact on Technical/Topical/Environmental Reports

The Safety I&C System Technical Report "APR1400-Z-J-NR-14001" will be revised, as indicated in the attachment associated with this response.

Table 7.2-7 (24 of 68)

No.	Name	Failure Mode	Cause	Symptoms and Local Effects Including Dependent Failures	Method of Detection	Inherent Compensating Provision	Effect on PPS	Remarks and Other Effects
2-9	CPC digital output (DO) module	DO module failure	Failures resulting in I/O Diagnostics indicating module failure	CPC WDT timeout. DNBR/LPD channel trips and pre-trips, CWP, "CPC Fail" annunciation	• DNBR/LPD channel trip/pre-trip • CPC Fail annunciators and indication at OM/MTP • CPC Trouble indication at OM/MTP • Diagnostics indicate DO module failure. • Local DO Module Fault lamp on, green Run lamp off	• Single PPS channel trip • Three-channel redundancy	RPS logic for function is converted to 1-out-of-2 coincidence logic.	To restore the system logic to 2-out-of-3 coincidence logic, the bypassed channel is returned to operation and the failed channel is bypassed. Module failures are monitored and cause CPC WDT timeouts.
2-10	CPC processor module (PM)	a) OFF; processor off. Failure of either the processor or communication section	Loss of module power; software execution stops	Watchdog timer timeout, DNBR and LPD trip/pre-trip/CWP output contact opening. Also CPC Fail OM/MTP indication.	• Channel DNBR/LPD channel trip and pre-trip, CWP, also CPC Fail, annunciation CPC trouble indication on OM/MTP • CPC processor fault lamp on, green Run lamp out	• Single PPS channel trip • Three-channel redundancy	The RPS logic is converted to 1-out-of-2 coincidence logic.	To restore the system logic to 2-out-of-3 coincidence logic, the bypassed channel is returned to operation and the failed channel is bypassed.
		b) ON; processor running, CPC fails to trip for a bona fide trip condition.	Erroneous inputs, improper addressable constant, Unrecognized hardware or software malfunction. *	Change in DNBR/LPD margin indication value of QIAS-N and IPS.	• Four channel comparison • DNBR/LPD margin indication of QIAS-N and IPS	• Three-channel redundancy	The RPS logic is converted to 2-out-of-2 coincidence logic (assuming no channel trip)	

* Unrecognized software malfunctions: Software failures which cannot be detected by system and application diagnostics.

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No.	Name	Failure Mode	Cause	Symptoms and Local Effects Including Dependent Failures	Method of Detection	Inherent Compensating Provision	Effect on PPS	Remarks and Other Effects
2-12	CEAC 1 processor module (PM) processor section	a) OFF; processor off	Loss of module power; software execution stops	• CEAC 1 watchdog timer timeout, CEAC 1 fail indication on OM/MTP. • Channel trouble indication / annunciation. • CEAC 1 fail flag to CPC in the same channel.	• CEAC 1 fail indication on OM/MTP • Channel trouble indication / annunciation CEAC 1 processor fault lamp on, green run lamp out	Two redundant CEACs in each channel.	• Affected CPC uses the last valid PF from the failed CEAC or the current PF from the operable CEAC, whichever is larger. • If the other CEAC is failed/declared inoperable/or in test, a large pre-assigned PF is assumed in that CPC.	Operation with a single failed CEAC in one or more channels addressed in LCO 3.3.3.
		b) ON; processor running, CEAC fails to detect proper CEA position, or otherwise fails to produce desired results.	Erroneous inputs, unrecognized hardware or software malfunction;	• Possible inconsistency in CEA position with respect to other CEAC/pulse count. • Failure to properly indicate CEA motion.	• Cross channel comparison of CEA position	Two redundant CEACs in each channel.	• Affected CPC uses the higher of the PFs from the two CEACs in the affected channel. • CEAC 1 is the preferred source of Target CEA position to the CPC. • If target CEA position is improper*, could get improper channel response to a valid subgroup deviation or groups out of sequence. • If so, only one CPC channel is affected. • RPS logic is converted to a 2-out-of-2 coincidence logic.	To restore the PPS logic to 2-out-of-3 coincidence, the bypassed channel is returned to operation and the failed channels are bypassed. Note that on line diagnostics identify problems in CEAC module and generate CEAC failure.

* Improper CEA positions: Erroneous CEA positions which cannot generate the DNBR/LPD trip.

Table 7.2-7 (28 of 68)

No.	Name	Failure Mode	Cause	Symptoms and Local Effects Including Dependent Failures	Method of Detection	Inherent Compensating Provision	Effect on PPS	Remarks and Other Effects
2-14	CEA position processor 1 in channels A or B. Processor and/ or communication section.	a) OFF; processor off	Loss of module power; software execution stops.	• CPP1 watchdog timer timeout, CPP trouble OM/MTP indication, channel Trouble annunciation. • Loss of alternate source of RSPT 1 CEA position transmission to CEAC 1 in all four channels. • Loss of preferred source of target CEA position in channel of origin. • Loss of receive ports for alternate CEA position to CEAC 1.	• CPP trouble OM/MTP indication, channel trouble annunciation in all four channels and channel trouble indication on OM/MTP in all 4 channels due to loss of 1 of 2 redundant sources of CEA position input • Run lamp out on affected CPP • Diagnostics identify loss of SDL input to CPC. • WDT in the affected CPP provide failure to CPC	• CPPs 1 and 2 are redundant in each channel. • CPP 2 in channels A and B is preferred source of CEAC 1 CEA position in all channels, and alternate source of target CEA position.	None. CEAC 1 in all channels normally receives CEA position from CPP2. Target CEA position input in affected channel is switched from the CEAC 1 to CPC SDL to the CEAC 2 to CPC SDL. Loss of CPP 1 receives ports in channels A and B disables the alternate source of SDL input to CEAC 1. This has no effect on CEAC 1 since the preferred SDL input is directly to the CEAC processor receive port.	Operation with a single failed CEAC in one or more channels addressed in LCO 3.3.3.
		b) ON; Erroneous CEA position transmitted *	Unrecognized hardware or software malfunction	• Failure to provide proper alternate source of CEA position in CEAC 1 in all channels. • Possible failure of preferred source of target CEA position transmission in channel of origin	• Possible erroneous target CEA position indication • If problem is due to processor failure, this is detected by on line diagnostics and a CPP trouble/CPP WDT time out.	• CPP1 is alternate source for CEAC 1 position indication, and is normal • CPP1 i source position CEA p improp channe • 3-chan	None. If target CEA position is improper, one CPC	To restore the PPS logic to 2-out-of-3 coincidence logic, the bypassed channel is returned to operation and the failed channels are bypassed

* Erroneous CEA position transmitted: When CEA values are different from reading values transmitted from the analog input modules to the CPP/ CEAC/CPC processors.

The figure will be replaced with the next page.

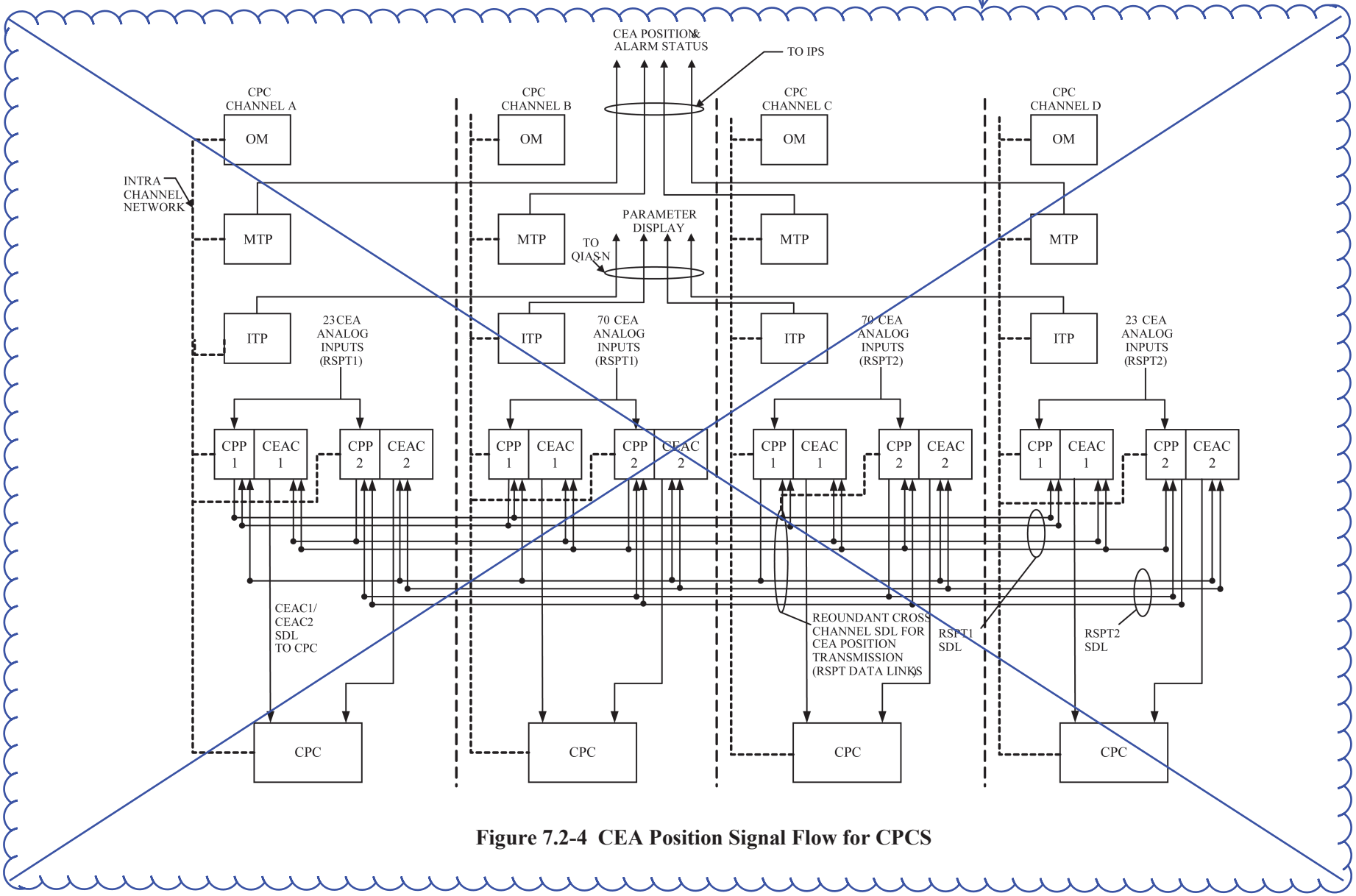


Figure 7.2-4 CEA Position Signal Flow for CPCS

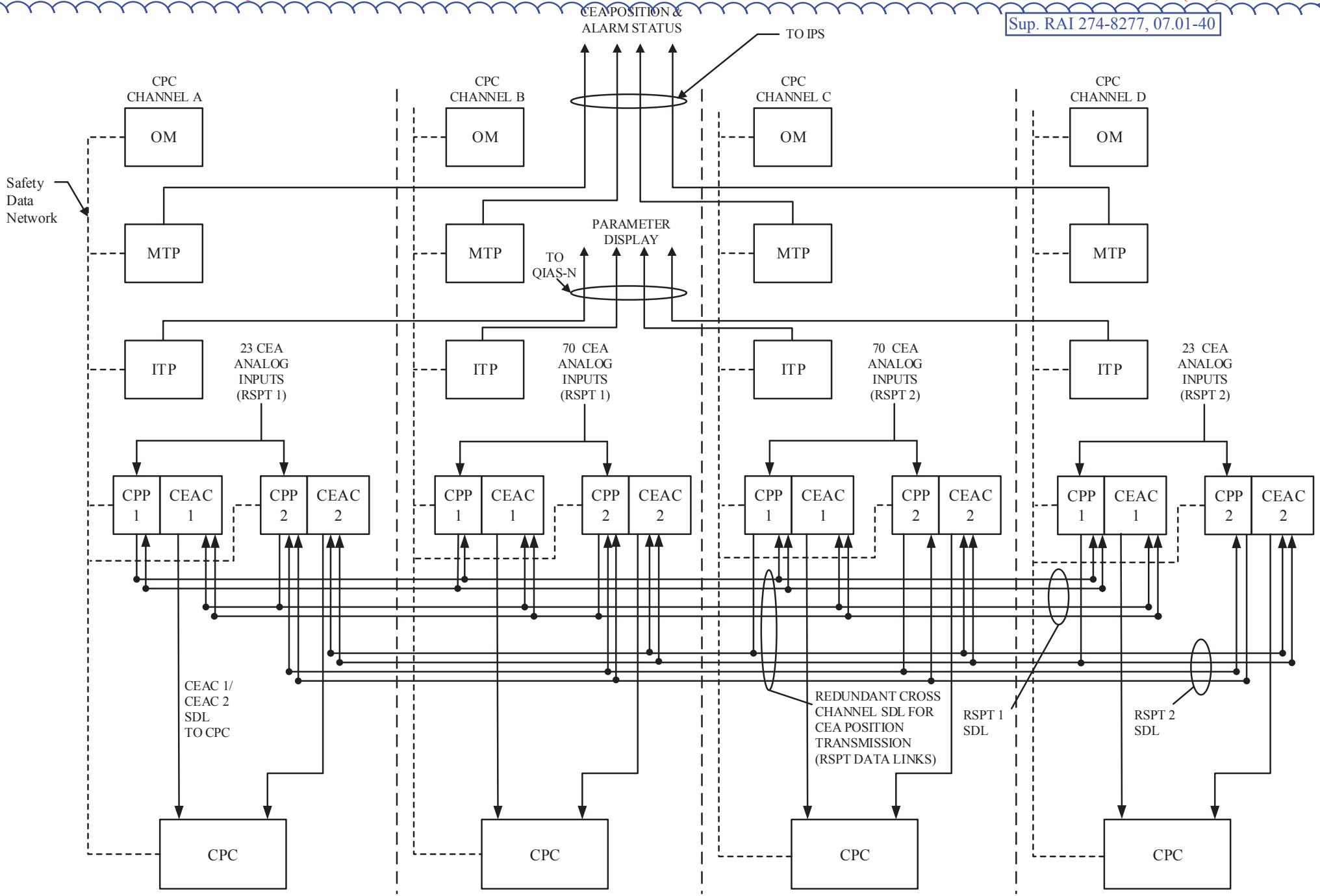
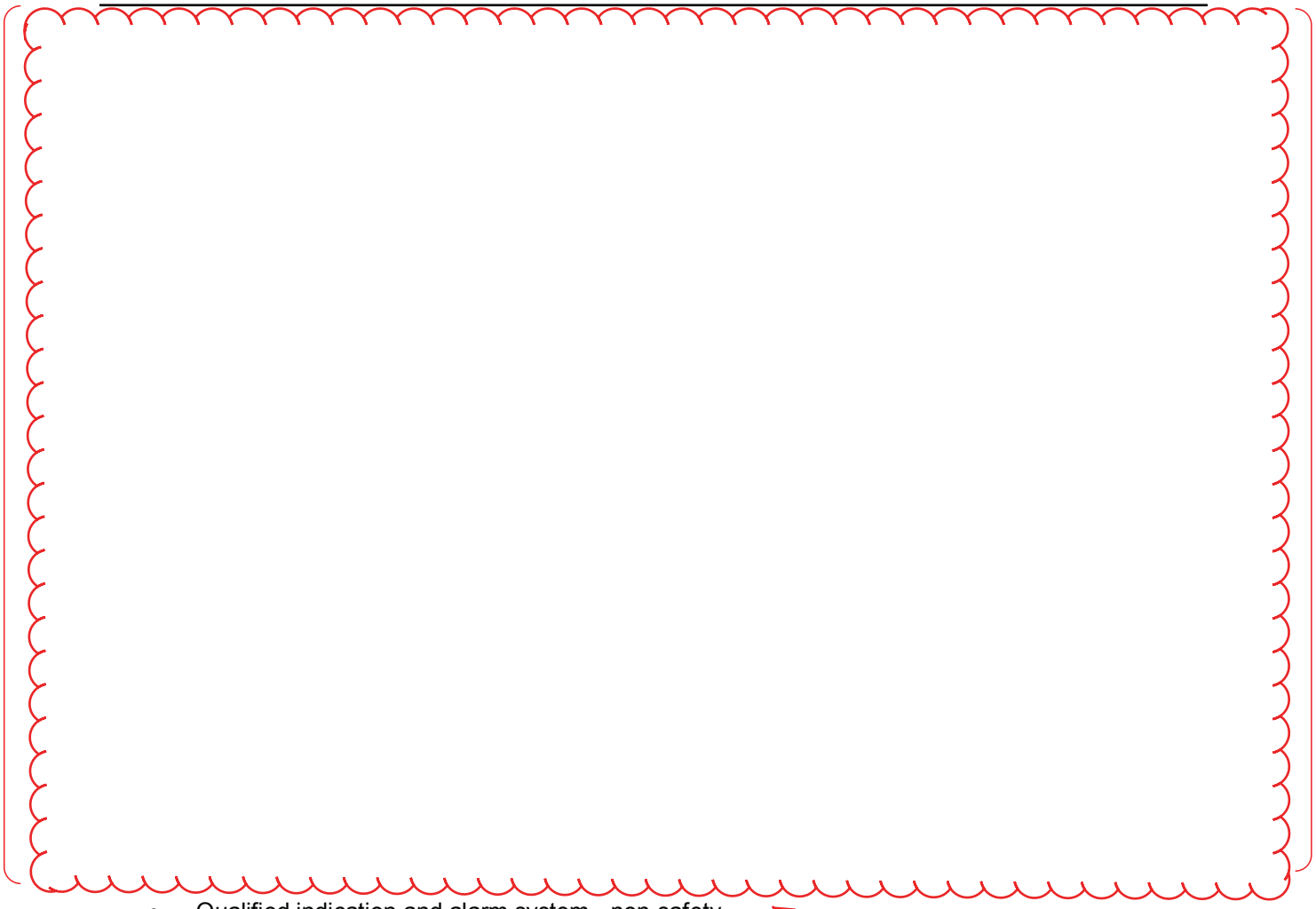


Figure 7.2-4 CEA Position Signal Flow for CPCS

LIST OF TABLES

The statement will be added.

LIST OF FIGURES



- Qualified indication and alarm system - non-safety
- Vital bus power supply system
- Field sensors

The figure will be added.

4.3.4.1 Auxiliary Process Cabinet-Safety

The CPC processor receives the pressurizer pressure signals from the APC-S used for DNBR and LPD calculation.

4.3.4.2 Ex-core Neutron Flux Monitoring System

The CPC processor receives the linear sub-channel power signals from the ENFMS. These are used for the reactor power calculation and power distribution calculation.

4.3.4.3 Reactor Coolant Pump Shaft Speed Sensing System

The CPC processor receives RCP speed signal from reactor coolant pump shaft speed sensing system (RCPSSSS) for the flow rate calculation.