HF Controls

HF CONTROLS CORPORATION

HFC-6000 Safety Platform

ERD921 Control System Test Specimen

Pre-Qualification Detail Report

TR901-201-02 Rev. A

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[XXXXXXXXXXXX]

Revision History

Date	Revision	Author	Changes
6/22/11	A0	I. Chow	Initial revision
5/28/15	A	Y. Lu	Revised for submittal

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1.0 Purpose and Scope

1.1 Purpose

HFC-6000 platform has been qualified by NRC to be used as safety systems in US nuclear power plants. NRC has released the safety evaluation report (SER) for the HFC-6000 platform in April 2011. This document summarizes the pre-qualification test activities of the ERD921 test specimen. In addition, the baseline performance for the ERD921 test specimen is provided in this document.

1.2 Scope

This document covers the components listed in the SER for the HFC-6000 platform. These components are listed in the following table. Modules listed in bold face fonts indicate that they are listed in the current HFC-6000 SER. The modules listed that are not bold face are additional modules with the updated test specimen.

Table 1 – Components in the ERD921 Test Specimen

Quantity	Modular Type	Description
2	**PS, Jasper 24V**	**600W 24V Power Supply**
1	Rack, Jasper PS	8-slot Jasper PS Rack, 19"
1	HFC-HUB06-16-01	16 Port 10/100 Hub
1	HFC-HUB06-16-02	16 Port 10/100 Hub
1	HFC-HUB06-16-EXT	Hub Extender
1	**HFC-BPC01-19**	**Controller Chassis backplane**
1	HFC-BPC03-08	3 Loop, 8 inch backplane
5	**HFC-SBC06**	**Main Controller**
4	**HFC-DPM06**	**Dual-Ported Memory**
2	HFC-SCG06	Communication Gateway
1	HFC-DPM06BP	Backplane Connected DPM06
12	**HFC-DI16I**	**Digital Input Card with SOE**
8	HFC-DO16C	Solid State Output Card
6	HFC-AI16RD	Analog Input Card (0 – 5 vdc) (DSP)
6	HFC-AO8FD	Analog Output Card (4 – 20 mA) (DSP)
3	HFC-AI8LD	Thermocouple Input Card
3	HFC-AI8MD	RTD Input Card, 100 ohm (DSP)
2	HFC-FOT06	Fiber-Optic Transmitter
4	**HFC-ILR06**	**I/O Link Repeater/Terminator**
1	**HFC-BPE01-19**	**Expander Chassis backplane**
1	HFC-SBC04A	Single Loop Controller
1	HFC-AC36FD	Analog I/O Module

2.0 References and Acronyms

2.1 References

ATP0402 ERD111– Control System Qualification Program, Application Software Objects Test Plan, Rev. A

DD0401 HFC-6000 Safety-Related Control System Qualification, Test Specimen Design Description, Rev. D

EPRI TR-107330	Generic Requirement Specification for Qualifying Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants, 1996
ML110831017	HFC-6000 Safety Evaluation Report by US NRC
TP901-201-02	TUV DMR Integration Test Plan, Rev B
TP901-202-02	TUV TMR Integration Test Plan, Rev B
TP901-203-02	TUV SLC Integration Test Plan, Rev B
TP901-201-04	DMR Operability Test Procedure, Rev E
TP901-202-04	TMR Operability Test Procedure, Rev D
TP901-203-04	SLC Operability Test Procedure, Rev C
TP901-201-05	ERD921 DMR Prudency Test Procedure, Rev B
TP901-202-05	ERD921 TMR Prudency Test Procedure, Rev C
TP901-203-05	SLC Prudency Test Procedure, Rev B
TP901-201-03	DMR TSAP Validation Test Plan, Rev B
TP901-202-03	TMR TSAP Validation Test Plan, Rev B
TP901-203-03	HFC-SBC04A SLC TSAP Validation Test Plan, Rev B
TP901-200-00	EPRI TR 107330 Pre-Qualification Test Procedures, Rev A
TP901-200-01	EPRI TR 107330 Burn-in Test Procedures, Rev. B
TR901-201-01	ERD921 – Control System Qualification Project (Retest), Summary Report for Burn-in Tests, Setup and Checkout Test, TSAP Validation Test, Rev. A
VV901-301-02	TUV DMR Master Configuration List, Rev C
VV901-302-02	TUV TMR Master Configuration List, Rev C
VV901-303-02	HFC-SBC04A System Master Configuration List, Rev C

2.2 Acronyms

AIC	Analog Input with Compensation
ANO	Analog Output
ASO	Application Software Objects
BOE	Burst of Events
C-Link	Communication Link
CPC	Communication Protocol Controller
CR	Condition Report
CRC	Cyclical Redundancy Check
DCS	Distributed Control System
DDB	Database Broadcast
DHA	Digital High Alarm
EMI	Electromagnetic Interference
ERD921	Engineering Research & Development Project 921
EWS	Engineering Workstation
HAS	Historical Archiving System
HFC	Doosan HF Controls
HPAT	HFC Plant Automated Tester
ICL	Intercommunication Link
I/O	Input/Output
MCRT	Microsoft (Windows) CRT Workstation
LAN	Local Area Network
MCL	Master Configuration List

MTP	Master Test Plan
PCB	Printed Circuit Board
PID	Proportional/Integral/Derivative
PCC	Peripheral Communication Controller
PLC	Programmable Logic Circuit
PV	Process Variable
PROM	Programmable Read Only Memory
RFI	Radio Frequency Interference
RTD	Resistance Temperature Detector
SER	Safety Evaluation Report
SP	Set Point
TSAP	Test System Application Program
UCP	Universal Communication Protocol

3.0 Pre-Qualification Test Sequences

Before the assembly of the ERD921 Control System/Test Specimen, the PLC/PCB components were verified for correct calibrations. After the assembly of the test specimen hardware was completed, the Test System Application Program (TSAP) was installed in the controllers and was verified as part of the overall integration process. Baseline performance data of the test specimen were collected after the Operability and Prudency tests were performed. This baseline performance data will be used in subsequent qualification testing for comparison. See Figure 1 for the pre-qualification test sequences.

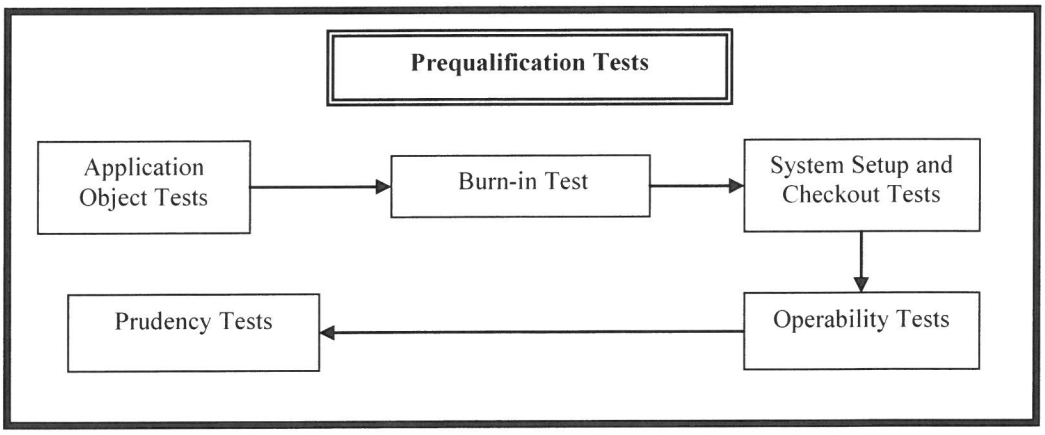

Figure 1 – Pre-Qualification Test Sequences

Application object tests, burn-in test, system setup, checkout and TSAP validation tests were one time tests. They were not repeated during or after the qualification stress tests. Selected operability and prudency tests were repeated during and after the qualification stress tests as required in accordance with EPRI TR 107330 guidance. Results of the pre-qualification tests are provided in the following sections.

4.0 Pre-Qualification Test Results

4.1 Application Object Test (ATP0402)

4.1.1 Purpose and Scope

The Application Object Test provides comprehensive testing of software objects that have a direct impact on the application code or that can be accessed by application code while it is running on the HFC-SBC06 controller. Such objects are designated as application software objects (ASO). The scope of testing included both functional operation and exception conditions for the following:

- Processing algorithms (called CQ4 blocks) used for analog control functions
- Mathematical operations executed directly by the application code without a CQ4 block
- Boolean operations executed directly by the application code

During compilation of the application object, the compiler generates error reports if any errors occur. Any compiling errors will be identified before the object code to be executed in the controller is generated. Only object code successfully compiled is downloaded via the UCP into the controller to be executed. During the download of the object code, the memory for the object code is write/read protected until the download action is finished. Therefore, the software for the compiler tool, peer-to-peer communication or UCP communication, and the execution of the object code are fully isolated. The successful testing of the ASO verifies the peer-to-peer communication and the compiler communication were successfully achieved during the test setup.

The Application Software Objects Test Plan, ATP0402 was developed following references in EPRI TR 107330-1996.

4.1.2 Results

The Application Software Objects Test Plan was completed successfully. No anomalies were found. See TR001-000-02, Application Software Test Report. This report was submitted to NRC.

4.2 Burn-in Test (TP901-200-01)

4.2.1 Purpose and Scope

The circuit card assemblies for HFC-6000 control system (Test Specimen) were run in a normal operating environment for a minimum period of 352 hours prior to system integration. The purpose of this test was to detect any early-life failures of component circuit cards. The scope of the test included two and a half times the total number of cards required for the complete Test Specimen. Circuit card assemblies not included in the initial configuration of the Test Specimen were reserved as spares to be used as replacements for any card that failed during the subsequent qualification tests.

4.2.2 Results

All assemblies that passed through to the qualification test program passed the burn-in test by successfully achieving the minimum cumulative 352 hours of burn-in operation.

4.3 Integration (Set-up and Checkout) Test (TP901-201-02, TP901-202-02, TP901-203-02)

4.3.1 Purpose and Scope

System setup and checkout tests were performed to verify that the project specified hardware, wiring and communication cabling had been installed and that communication had been established over each communication link prior to TSAP validation.

The following activities were performed:

- Verify that all project specified equipment / hardware had been received, functionally tested, and set-up per project documents
- Verify correct software was installed in Test Specimen, HPAT, EWS PC's
- Verify correct installation for all interconnection wiring and communication had been established
- Verify that all HFC-6000 I/O modules were functional and communicating with HFC-SBC06 controllers

4.3.2 Results

All equipment was configured properly. Communication links were correctly setup with no errors.

4.4 TSAP Validation (TP901-201-03, TP901-202-03, TP901-203-03)

4.4.1 Purpose and Scope

TSAP validation tests were performed to verify that the system with the TSAP application installed can communicate with the controllers to support the operability and prudency tests in accordance with EPRI TR 107330.

The following activities were performed:

- Source code review of the TSAP
- Validation of the functional operations of TSAP manually to ensure performance functionality of individual PCB's as required by the standards
- Validation of the automated operability and prudency test algorithms

4.4.2 Results

This test procedure was completed and all equipment was configured as required. Any anomalies that were found were resolved prior to completion of the procedure.

4.4.3 Summary

All assemblies met the acceptance criteria for the system setup, checkout and TSAP validation. The ERD921 test specimen was validated to collect baseline system performance data for the qualification tests.

4.5 OPERABILITY TEST (TP901-201-04, TP901-202-04, TP901-203-04)

The purpose of the operability test was to collect the performance data for the system. Data collected before qualification testing was used as baseline performance data. This performance baseline was then used as the basis for evaluating system performance during and/or following each of the qualification tests required by the EPRI 107330. The operability test includes the following tests:

- **Accuracy Test** - This test developed a baseline to compare against the accuracy and linearity of the analog I/O modules observed during the qualification tests.

- **Response Time Test** – This test measured the response time for discrete and analog inputs.

- **Discrete Input Operability Test** - This test verified the capability of discrete input channels to detect a transition in the input signal being monitored.

- **Discrete Output Operability Test** - This test verified the capability of discrete output channels to operate reliably within its specified loading conditions.

- **Communication Operability Test** – This test verified reliable data transfer over the ICL, C-Link, and serial interfaces with external devices - Control Switch Module (CSM) and M/A stations. Although CSM, and M/A stations are not part of the qualified components, they were present during the testing.

- **Timer Test** – This test developed the baseline for the timer function accessible to the TSAP.

- **Test of Failure to Complete Scan** – This test validated that the system can be configured to failover to the redundant controller when an application could not complete within one scan cycle. This test also validated the hardware watchdog function.

- **Failover Operability Test** – This test demonstrated correct operation of the failover function.

- **Loss of Power Test** – This test demonstrated correct response of all I/O channels to loss of source power followed by reapplication of power to the system.

- **Power Interruption Test** – This test demonstrated the capability of the power modules to sustain system operation during a temporary (40-ms transient) power interruption.

4.5.1 Accuracy Test Results

4.5.1.1 AI16RD – 0 to 5V Analog Input Card

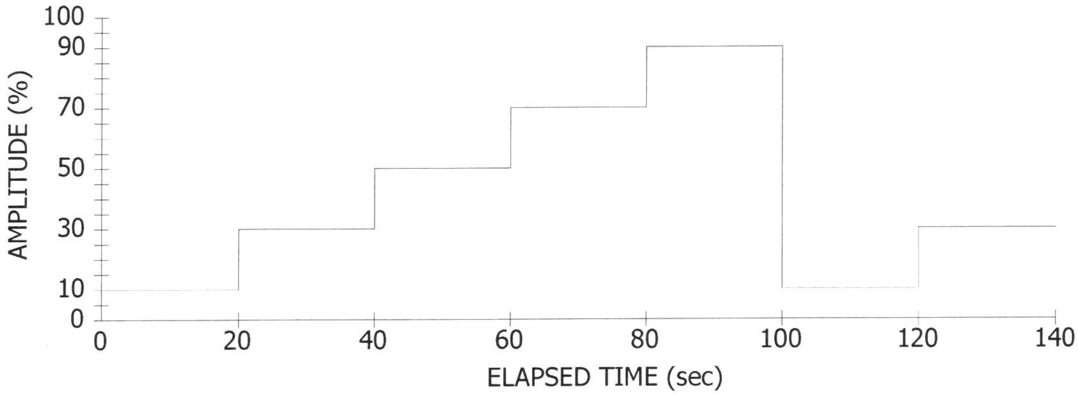

***Figure 2* – Algorithm for 4- to 20 mA Analog Channel Accuracy Test**

Table 2 – TMR AO8FD-AI16RD Manual Accuracy Test Results

AO8FD-AI16RD Signal Level	Average Test Signal	Accuracy AI Image	[XXX] AIC Value	% Accuracy
[XXX]	[XXX]	[XXX]	[XXX]	[XXX]
	[XXX]	[XXX]	[XXX]	[XXX]
	[XXX]	[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]	[XXX]	[XXX]
	[XXX]	[XXX]	[XXX]	[XXX]
	[XXX]	[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]	[XXX]	[XXX]
	[XXX]	[XXX]	[XXX]	[XXX]
	[XXX]	[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]	[XXX]	[XXX]
	[XXX]	[XXX]	[XXX]	[XXX]
	[XXX]	[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]	[XXX]	[XXX]
	[XXX]	[XXX]	[XXX]	[XXX]
	[XXX]	[XXX]	[XXX]	[XXX]

Table 3 – DMR AO8FD-AI16RD Manual Accuracy Test Results

AO8FD to AI16RD		Average	Accuracy	[XXX] %	
Set Value	Count Value	Measured AO	AI Image	AIC Block	Accuracy
[XXX]	[XXX]	[XXX]	[XXX]	[XXX]	[XXX]
		[XXX]	[XXX]	[XXX]	[XXX]
		[XXX]	[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]	[XXX]	[XXX]	[XXX]
		[XXX]	[XXX]	[XXX]	[XXX]
		[XXX]	[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]	[XXX]	[XXX]	[XXX]
		[XXX]	[XXX]	[XXX]	[XXX]
		[XXX]	[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]	[XXX]	[XXX]	[XXX]
		[XXX]	[XXX]	[XXX]	[XXX]
		[XXX]	[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]	[XXX]	[XXX]	[XXX]
		[XXX]	[XXX]	[XXX]	[XXX]
		[XXX]	[XXX]	[XXX]	[XXX]

4.5.1.2 AI8MD RTD Card

A test configuration for measuring analog output channel accuracy was shown in Figure 3. The RTD card under test was calibrated from 0 °C to 200°C. A Fluke 743B with accuracy within ±0.01% of output + 0.04Ω was used for generating temperature input to the RTD input channels. The actual readings from the card were compared with the inputs to calculate accuracy for each RTD channel.

Table 4 show the analyses of test data and the resulting accuracies of the channels under test calculated as 100%*(Actual value – Expected value)/32767, in which 32767 represents the full RTD operational range.

Figure 3 – RTD Channel Test Configuration

Table 4 – AI8MD Accuracy Test Results

AI8MD Input (°C)	Expected	Actual Measurement (counts) CH1	Accuracy (%) CH1
[XXX]	[XXX]	[XXX]	[XXX]
		[XXX]	[XXX]
		[XXX]	[XXX]
[XXX]	[XXX]	[XXX]	[XXX]
		[XXX]	[XXX]
		[XXX]	[XXX]
[XXX]	[XXX]	[XXX]	[XXX]
		[XXX]	[XXX]
		[XXX]	[XXX]
[XXX]	[XXX]	[XXX]	[XXX]
		[XXX]	[XXX]
		[XXX]	[XXX]
[XXX]	[XXX]	[XXX]	[XXX]
		[XXX]	[XXX]
		[XXX]	[XXX]
		Avg.	[XXX]

4.5.1.3 AI8LD TC Card

The TC card under test was calibrated from -30°C to 500°C. A Fluke 743B with accuracy within ±0.01% of output + 0.04Ω was used for generating temperature input to the TC input channels. The actual readings from the card were compared with the inputs to calculate accuracy for each TC channel.

Table 5 show the analyses of test data and the resulting accuracies of the channels under test calculated as 100%*(Actual value – Expected value)/32767, in which 32767 represents the full RTD operational range. All eight AI8M channels measured meet the acceptance criteria of ±0.285% (± 2 °C) accuracy in accordance with EPRI TR 107330.

Table 5 – AI8LD Accuracy Test Results

AI8MD Input (°C)	Expected	Actual Measurement (counts) CH1	Accuracy (%) CH1
[XXX]	[XXX]	[XXX]	[XXX]
		[XXX]	[XXX]
		[XXX]	[XXX]
[XXX]	[XXX]	[XXX]	[XXX]
		[XXX]	[XXX]
		[XXX]	[XXX]
[XXX]	[XXX]	[XXX]	[XXX]
		[XXX]	[XXX]
		[XXX]	[XXX]
[XXX]	[XXX]	[XXX]	[XXX]
		[XXX]	[XXX]
		[XXX]	[XXX]
[XXX]	[XXX]	[XXX]	[XXX]
		[XXX]	[XXX]
		[XXX]	[XXX]
		Avg.	[XXX]

4.5.1.4 Automated Analog Accuracy

The automated test sequence was executed after the manual test sequences during prequalification testing, and then repeated before, during, and after selected qualification tests. The purpose of the prequalification test was to provide a baseline to compare the tests performed at the other times listed above in addition to the manual accuracy test data.

The test waveform for the 4 to 20mA AO channels is generated by an algorithm running in the TSAP on command from MCRT. No special configuration is required prior to running this automated test. The RTD modules each have one channel configured with an RTD wire, and the TC modules have two channels configured with input signal sources. Values for the TC and RTD channels will be logged continuously by the HAS.

TMR Description	**Output Point**	**Input Point**	**HAS Log Point**
[XXX]	[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]	[XXX]

DMR Description	**Output Point**	**Input Point**	**HAS Log Point**
[XXX]	[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]	[XXX]
SLC Description	**Output Point**	**Input Point**	**HAS Log Point**
[XXX]	[XXX]	[XXX]	[XXX]

Figure 4 – Automated Analog Accuracy Test Arrangement

The following figures show the data collected for AI16RD and AO8FD PCB's during the pre-qualification testing.

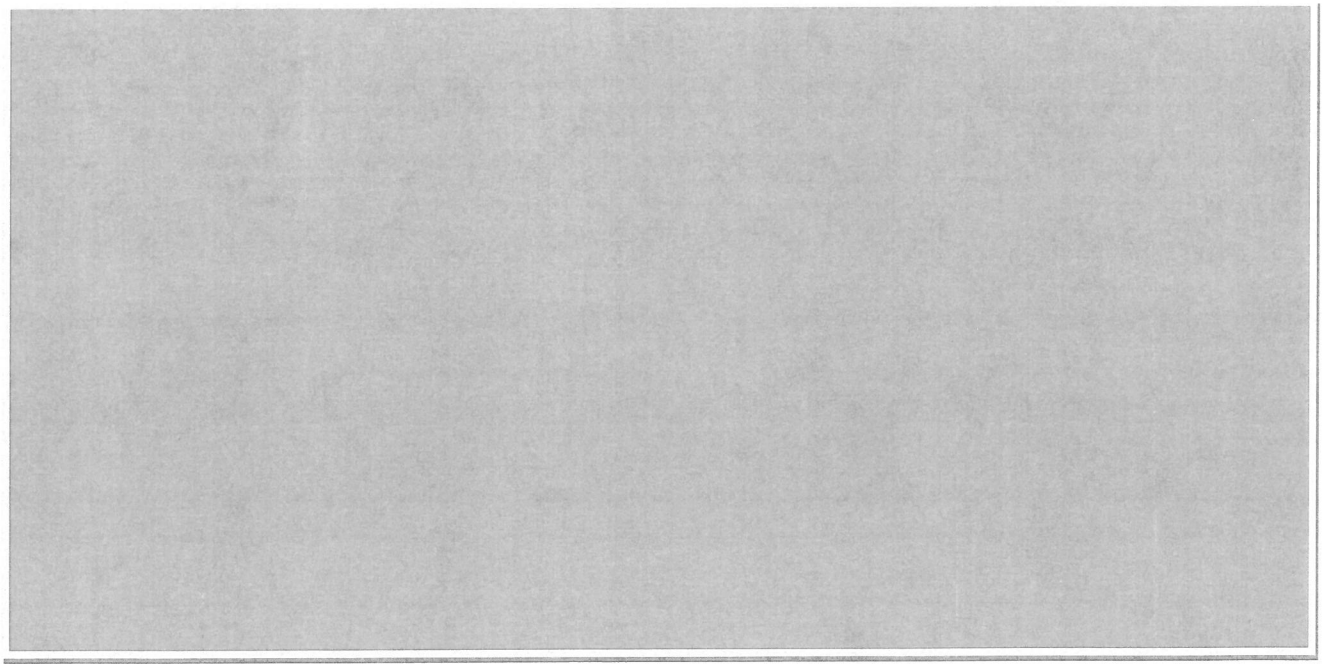

Figure 5 – AI16RD Automated Accuracy Data

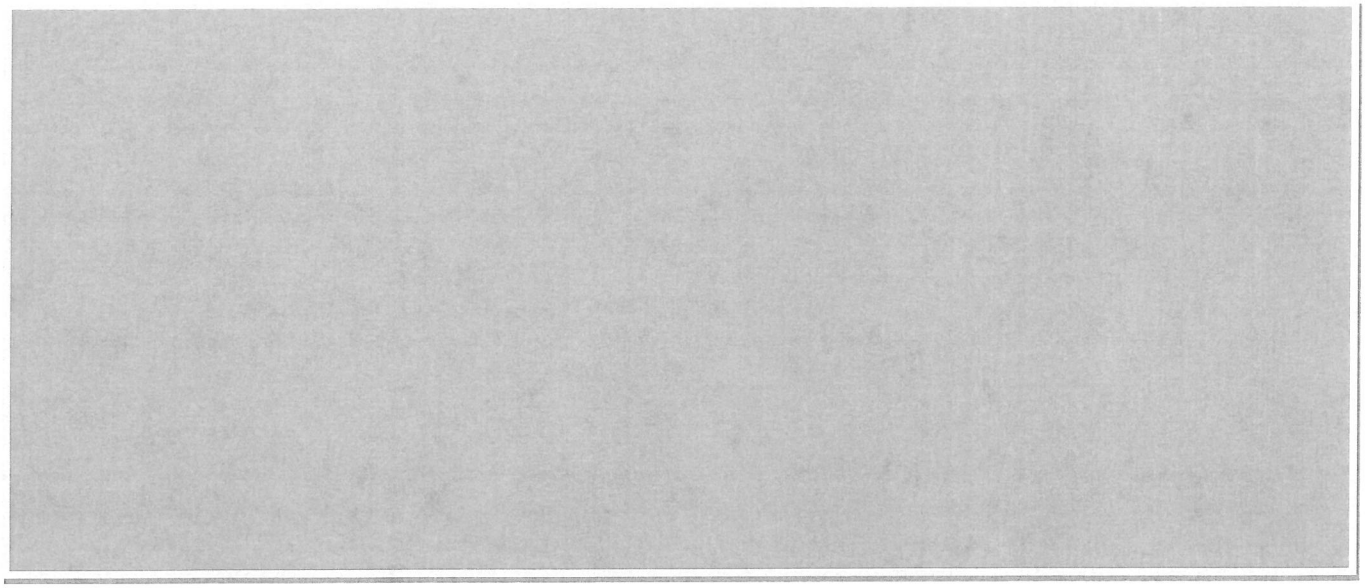

Figure 6 – AO8FD Automated Accuracy Data

The adjusted accuracy based on the corrector factors for AI16RD and AO8FD automated channels are listed in the following tables:

Table 6 – TMR Accuracy Measured Using the Automated Algorithm

Input (%)	Accuracy (%) AO8FD - AI16RD
[XXX]	[XXX]
[XXX]	[XXX]
[XXX]	[XXX]
[XXX]	[XXX]
[XXX]	[XXX]
Average	[XXX]

Table 7 – DMR Accuracy Measured Using the Automated Algorithm

Input (%)	Accuracy (%) AO8FD - AI16RD
[XXX]	[XXX]
[XXX]	[XXX]
[XXX]	[XXX]
[XXX]	[XXX]
[XXX]	[XXX]
Average	[XXX]

As shown in Table 6, the accuracy for AI16F and AO8F were within 0.35% and 0.32% respectively in every step of the input algorithm which meets the acceptance criteria in EPRI TR 107330.

The AI8MD RTD and AI8LD TC Card channels were configured for automatic logging by the HAS logger. A summary of these setups and the initial logged values is provided below.

AI8MD RTD Channels - [XXXX] resistors had been installed to serve as load for channel 1 on an RTD card (1,AI,17). During the prequalification testing, a Fluke 743B will be used to simulate the operation of an RTD element, it is connected to the terminals for 1,AI,18. Fluke 743B will then simulate five temperature levels, [XXXXXXXXXXXXXXXXXX]. Channels 1 was monitored in the HAS as points "1,BL,17".

AI8LD TC Channels - 1, AI,32 is connected to a real type-E thermocouple. 1,AI,25 is connected to a constant voltage source of [XXXXX] (equivalent to an input of [XXX]. During the prequalification testing, a Fluke 743B will be used to simulate the operation of an TC element, it is connected to the terminals for 1,AI,26. Fluke 743B will then simulate five temperature levels, [XX XXXXXXXXXXXXXXXXX]. Selected channel was monitored in the HAS as points "1,BL,89".

4.5.2 Response Time Test Results

4.5.2.1 Digital Response Time

The automated digital response time test used two different algorithms as shown in Figure 7. The first algorithm consists of seven consecutive DI points driving seven consecutive DO points within the TSAP, and hard-wire connections routed the DO signals to the input points for those DI channels. When the test was enabled, these points produced a free-running algorithm that required 14 transfer passes to produce a single cycle. Consequently, dividing the average period by 14 produced one measure for the input-to-output response time.

The second algorithm consists of a single input from the HPAT that set/reset a MS point within the TSAP. The image of this MS point then controlled a trip output, so the delay between the transition of the input from the HPAT to the response of the trip output constitutes a direct measure of the input-to-output response time of the ERD921 controller.

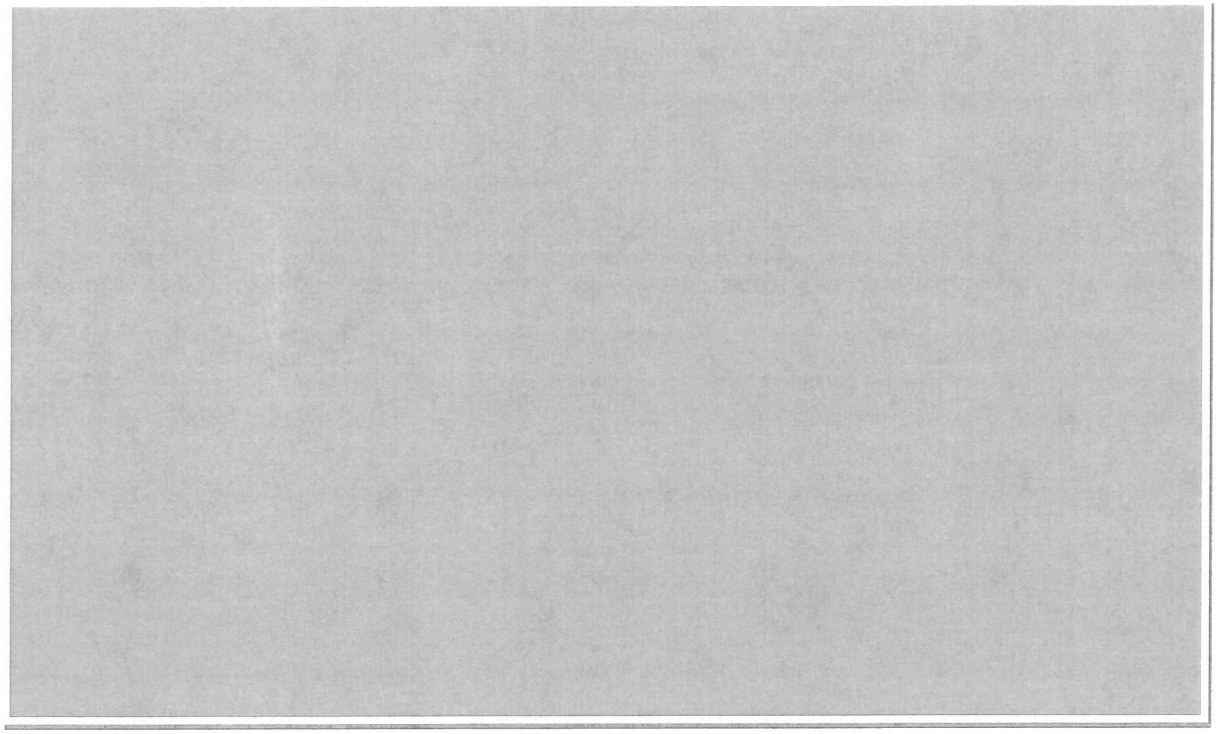

Figure 7 – Algorithm for Digital Response Time

Table 8 – Digital Response Time Test Results

Response Delay	**2,DO,401 to 2,DO,405**	
Algorithm	**Leading Edge**	**Trailing Edge**
Baseline Response SOE File: TMR Automated Response 5-24-10.txt		
Average	[XXXXX]	[XXXXX]

Response Delay	2,DI,421 to 2,DI,417	
Algorithm	Leading Edge	Trailing Edge
Baseline Response SOE File: DMR S1801150.txt		
Average	[XXXXX]	[XXXXX]

Baseline Results	SOE File: SLC Response Time Test 5-14-10.txt			
Algorithm	Log Point	Minimum	Average	Maximum
Test Response	2,DI,241– 2,DI,242	[XXXXX]	[XXXXX]	[XXXXX]

4.5.2.2 Analog Response Time Test

The algorithm used to test analog response time consists of a simulated analog trip signal from the HPAT and a DHA block configured to trip when its input reaches 50%. See Figure 8. Since the HAS logger is limited to a one-second update rate, the SOE logger was used to record the data for this test. In order to produce signals that could be detected by the SOE input card, an external module triggered a relay at the leading and trailing edge of the analog trip signal.

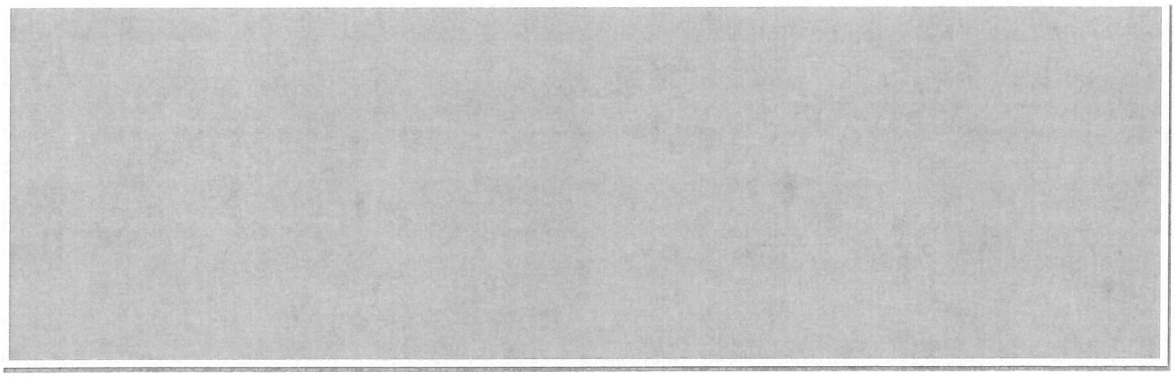

***Figure 8* – Analog Response Time Test Algorithm**

Table 9 – Analog Response Time Test Results

Response Delay	2,DI,411 to 2,DI,412	
Algorithm	Leading Edge	Trailing Edge
Baseline Response SOE File: TMR Automated Response 5-24-10.txt		
Average	[XXXXX]	[XXXXX]

Response Delay	2,DI,428 to 2,DI,427	
Algorithm	Leading Edge	Trailing Edge
Baseline Response SOE File: DMR S1801150.txt		
Average	[XXXXX]	[XXXXX]

Response Delay	2,DI,243 to 2, DI,244	
Algorithm	Leading Edge	Trailing Edge
Baseline Response SOE File:		

Average	[XXXXX]	[XXXXX]

4.5.3 Discrete Input Operability Test

This test was conducted during the pre-qualification phase of testing to establish a performance baseline. The baseline data will be compared against the data from the same test preformed at the completion of the qualification program.

The Discrete Input Operability test demonstrates the capability of each type of discrete input channel to detect a transition in the signal being monitored. In order to accomplish this, DI channels under test are subjected to an input signal whose voltage level is controlled by a manual rheostat. During the test, the set voltage level and the reset voltage level for each DI channel type were measured.

One channel of each DI card type to be qualified is tested for the following characteristics while the card is operating in the Test Specimen chassis:

- Set Voltage Threshold – the lowest voltage level that the DI image is switched from off to on
- Maximum Input Voltage – the maximum voltage level the DI channel to remain stable
- Dropout Voltage (reset voltage level) – is the voltage level that the DI image is switched from on to off and remained reset
- The voltage to the DI channel was dropped from the reset voltage level to 0 to prove the channel remains reset
- Each DI channel being tested was turned on to prove input signal isolation

Table 10 – Discrete Input Channel Test Results

Test SLC	Test Results (Average on 3 measurements)		
	SBC04A – 48V		
Set Voltage Threshold	[XXXXX]	[XXXXX]	[XXXXX]
Maximum Input Voltage	[XXXXX]	[XXXXX]	[XXXXX]
Dropout Voltage	[XXXXX]	[XXXXX]	[XXXXX]

Test TMR	Card Type Under Test							
	DI16I				DC33			
	1	2	3	Average	1	2	3	Average
Set Voltage Threshold	[XXX]	[XXX]	[XXX]	[XXX]	[XXX]	[XXX]	[XXX]	[XXX]
Maximum Input Voltage	[XXX]	[XXX]	[XXX]	[XXX]	[XXX]	[XXX]	[XXX]	[XXX]
Dropout Voltage	[XXX]	[XXX]	[XXX]	[XXX]	[XXX]	[XXX]	[XXX]	[XXX]
	DC34				DC35			
	1	2	3	Average	1	2	3	Average
Set Voltage Threshold	[XXX]	[XXX]	[XXX]	[XXX]	[XXX]	[XXX]	[XXX]	[XXX]
Maximum Input Voltage	[XXX]	[XXX]	[XXX]	[XXX]	[XXX]	[XXX]	[XXX]	[XXX]
Dropout Voltage	[XXX]	[XXX]	[XXX]	[XXX]	[XXX]	[XXX]	[XXX]	[XXX]

Test DMR	Test Results (Average on 3 measurements)		
	DI16I – 48V		
Set Voltage Threshold	[XXX]	[XXX]	[XXX]
Maximum Input Voltage	[XXX]	[XXX]	[XXX]
Dropout Voltage	[XXX]	[XXX]	[XXX]

4.5.4 Discrete Output Operability Test

The Discrete Output Operability test demonstrated the capability of each type of discrete output channel to operate within its specified range of loading conditions. In order to accomplish this, the channel under test was energized while connected to a simulated field load that imposes maximum loading on the channel. The test demonstrated the capability for individual channels to sustain such maximum loading conditions without failure and without affecting operation of adjacent channels. The test was conducted during the pre-qualification phase of testing to establish a performance baseline and after completion of the environmental stress tests to detect any deterioration from that level of that performance. It was not repeated before, during, and after any of the other qualification tests. Refer to ERD111 test results.

4.5.5 Communication Operability Test

The Communication Operability Test was conducted during the prequalification phase of testing and then repeated before, during and after each qualification test. The purpose of the prequalification test was to provide a baseline to compare against the tests performed at the other times listed above. Refer to ERD111 test results.

The HFC-6000 control system includes two internal communication networks. Intercommunication links (ICL) enable communication between the controller and all configured I/O modules for a particular controller. Redundant C-Link channels enable communication between a remote controller and attached workstation PCs, other remote controllers, or with external equipment.

This test used link error counters to provide a basis for evaluating the quality of communication on these links. The overall test method consisted of recording the count value of the error counters at the start and end of a test period and interpreting the total accumulated error count as the measure of communication reliability. The automatic tests were run to provide background activity for the communication test.

4.5.5.1 ICL Error Counters

The ICL link error counters can be read through an HFC software utility – Memory Editor and screen captures were made for the ICL link error counters. The system controller maintains an ICL error counter for each I/O module that communicates with that controller through an ICL. Whenever the system controller resets, all the ICL error counters will be reset to 0. Whenever an I/O module fails, its corresponding ICL error counter will increase rapidly. ICL error counter rolls over at 32767, i.e. $FFFF_H$. Refer to ERD111 test results.

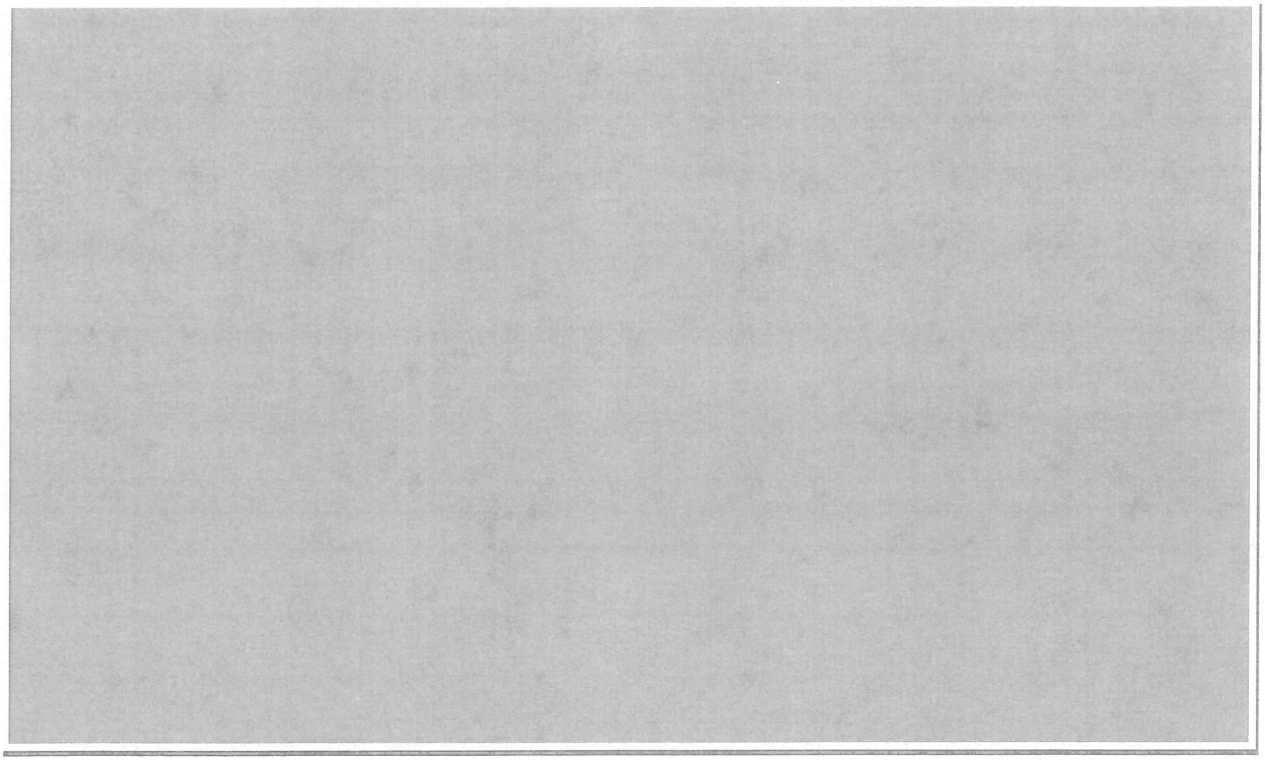

Figure 9 – Memory Editor Screenshots before and after Pre-Qualification Tests

Figure 9 shows the screen captures of HFC memory editor during pre-qualification tests. As indicated in the figures, the ICL error counter did not increase during the pre-qualification tests.

Therefore, no ICL communication errors were reported. The ICL communication was validated in accordance with the acceptance criteria.

4.5.5.2 C-Link Error Counters

C-Link error counters were captured through HAS data from the CPC error counters: 4,CO,10 and 4,CO,11. The HAS database showed the values of these two counters remained zero during the operability tests for the ERD921 test specimen. Therefore, C-Link communication also met the acceptance criteria for the communication operability test

4.5.6 Timer Test

The purpose of this test was to verify the accuracy of the timer function used in the TSAP. The timer test is based on logic completely contained within the TSAP. This logic consists of four pulse timers configured to control two separate free-running square waveforms. The output from one set of timers is on for 1 second and off for 1 second; the waveform from the second set is on for 5 seconds and off for 1 second. The two output signals drive two separate DO channels. This arrangement allows the direct measurements with an oscilloscope. During qualification testing, the outputs from the two DO channels are routed to separate SOE input channels of the HPAT to permit automatic recording of the signal transitions.
The results of the automated timer test are shown in the following table:

Table 11 – Time Test Results

TMR Timer Test 4-28-10.TXT

Test Phase	Averaged Period	2, DI,403		2, DI , 404	
		Avg Value	Accuracy	Avg Value	Accuracy
Baseline Test	**Period Total**	[XXXX]	[XXXX]	[XXXX]	[XXXX]

DMR Timer Test 5-6-10.TXT

Test Phase	Averaged Period	2,DI,419		2,DI,420	
		Avg Value	Accuracy	Avg Value	Accuracy
Baseline Test	**Period Total**	[XXXX]	[XXXX]	[XXXX]	[XXXX]

The specified acceptance criterion for the timer function is that timer accuracy shall vary by no more than ±1% of the preset value or by more than ±3 scan cycles. Based on the counter value, "1,CO,50", the TSAP application was estimated to run 22 times per second on average. That meant the scan cycle was about ~[XX]. 3 scan cycles were around ~[XX].

Table 11 indicates that the *averaged* period meets the ±1% acceptance criterion for all timer periods: 1s OFF to ON, 1s ON to OFF, 5s OFF to ON, 1s OFF to ON.

4.5.7 Test of Failure to Complete Scan

This test validated that the system could be configured for failover to the redundant controller when an application did not complete a full scan within one context switch.

The following figure shows how response time can provide evidence for detecting the failure to complete scan event. The response time included the digital transfer time which was ~82ms. Subtracting the digital transfer number from the response time, the value became less than 200ms which was twice the context switch time. This response time range of values was expected because it took at least 1 context switch to allow the application not to complete and it took approximately less than 2 context switch time for the system to detect that.

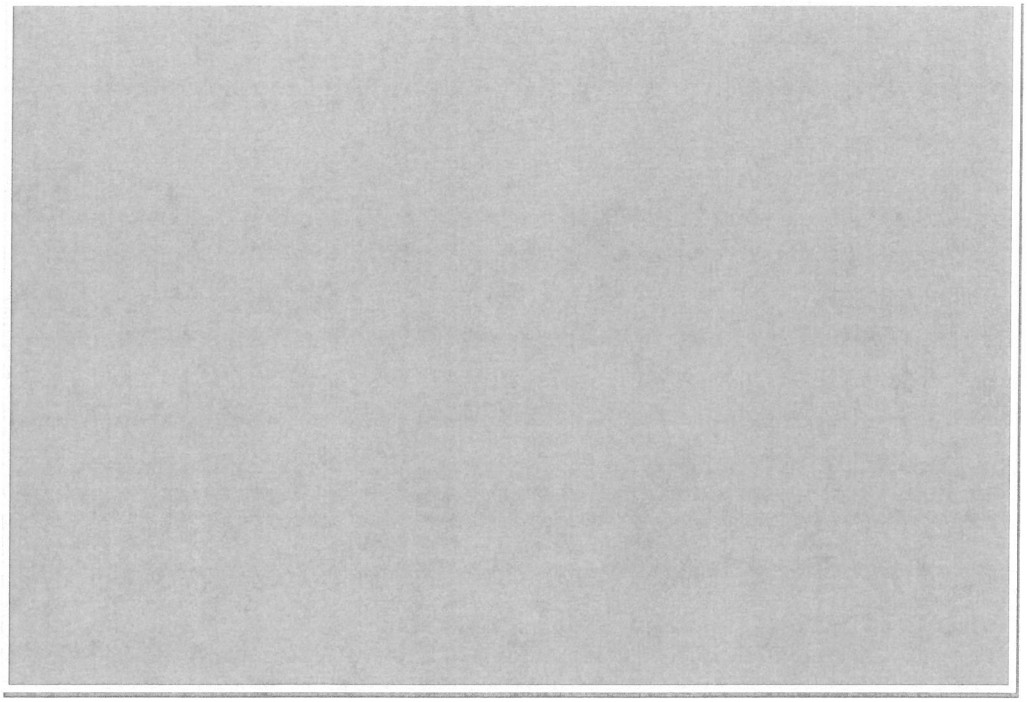

Figure 10 – Calculation of the detection of failure to complete scan time

4.5.8 Failover Operability Test

The purpose of this test was to verify proper failover of the redundant controllers. The baseline data will be compared against other data from the same tests performed at the completion of the qualification program to demonstrate that the system performance was not impacted by being stressed up to and beyond its normal operating state.

The HFC-6000 control system includes redundant controllers and redundant power supplies. The redundant controllers share a Dual-Ported Memory (DPM) assembly that provides the mechanism for transferring system status from the primary to the secondary controller.

Tests were also performed to measure the effect of the failover on both digital and analog loops. These failover tests focused on capturing the magnitude of disruption to analog and additional values from the I/O cards and system performance during failover.

These tables and figures show there were no impacts on stable analog values or analog values in transition during failover. Refer to ERD111 test results.

4.5.9 Loss of Power Test

The purpose of the test was to demonstrate that output channels went to their inactive levels when power was lost and that they remained in those states until the controller completed its internal initialization. This test was run during pre-qualification, at the end of the high temperature and low temperature phases of the environmental stress test.

The acceptance criterion in EPRI TR 107330 states that all output channels return to de-energized state during power loss and all output channels remain in failsafe state until operator initiates operation.

Refer to ERD111 test results.

The HAS data examined the interval from approximately 2 minutes before the power outage to 2 minutes after the power outage. The SOE records were started during the power outage and recorded data for several minutes after power was restored. No output from the ERD921 test system was logged by either the SOE or the HAS during the power outage. During the first several minutes following restoration of power, the following transitions are noted to occur:

- The SOE logged several transitions of the analog response time trigger signal before the first response from the ERD921. This corresponds to the initialization period of the test system during which all output channels remained static.
- The HAS log indicates that input channels started reporting value updates before any output channel started to drive any output signal.

The test results showed that after the loss of power:

1. All AO channels are open
2. All power output channels are open
3. All solid state relay DO channels are open
4. All mechanical relay DO channels are deenergized

After power was restored, all operations returned to normal:

- The performance ranges of the digital and analog response time algorithms are within the limits previously received
- The averaged values for the timer test are within the ranges previously recorded

These test results provided evidence that the ERD921 test specimen meet the acceptance criteria for loss of power.

4.5.10 Power Interruption Test

The power interruption test subjects the system to a 40 ms interruption in source AC power to demonstrate the capability of the system to continue functional operation during switchover to a backup power source. The test was conducted during pre-qualification, during the high temperature and low temperature phases of the environmental test with the following background conditions configured:

- Static points were configured to known states
- Automatic accuracy test, response time test, and timer test were running

The following acceptance criteria are specified for this test:

- No controller resets
- No static DO channel changes state
- No static AO point changes its value by more than 5%
- Logged parameters for all of the automated tests remain within tolerance

Refer to ERD111 test results.

During power interruption, there was no delay or loss of signal which could degrade performance data below the acceptable limits. System performance data was all in line with data collected when power input was stable.

In addition to the above dynamic test results, the static points monitoring by HAS did not show any variation. No anomalies were found during the power interruption test.

4.6 Prudency Tests (TP0901-201-05, TP901-202-05, TP901-203-05)

The prudency testing validates the PLC/PCB system performance in highly dynamic conditions. In addition, data collected from the Burst of Events (BOE) for analog input and output cards provide different sets of performance data.

The entire Prudency test was conducted during the pre-qualification phase of testing to establish a performance base line. During subsequent qualification tests, the BOE test and the other tests were repeated at various points in accordance with the EPRI standards to identify any performance degradation from the performance baseline. The prudency test includes the following tests:

- **Burst of Events Test** - This test consists of the simultaneous activation of a significant proportion of input and output channels in accordance with EPRI TR-107330 paragraph 5.4.A. This test was automated and was typically run as a continuous background operation for selected qualification test.

- **Serial Port Failure Test** – The test specimen has two redundant serial communication links. For each redundant link, this test imposed three simulated failures on one cable at a time: link open, transmit line shorted to ground, and transmit line shorted to receive line.

- **Serial Port Noise Test** - This test introduced a white noise signal on each of the serial links one port at a time.

4.6.1 Digital BOE Test

The digital BOE test was logged a number of times during the execution of the Prudency tests. A summary of three SOE reports are presented in the following tables, and this data represents averages from a total of BOE transitions. The data from exhibited one instance of relay contact bounce. Apart from that one instance of contact bounce, every transition was present within the stipulated tolerance of 1.00 ± 10% second, and no link or station alarm occurred during the test interval.

These tables were divided into two sets of points. These two sets of points represent the different phase relationship between the BOE driving signals. Two of the source control signals were logged directly – 2,DO,17 and 2,DO,18. These signals were slightly asymmetric due to the characteristics of the timer function in the HPAT. This deviation produced a small part of the reported deviation, and the remainder was produced by the processing of the ERD921 Test Specimen and the TSAP logic.

4.6.2 Analog BOE Test

The test channel are driven by the same HPAT algorithm, and all are logged by the HAS.

The following table showed the result:

Table 12 – BOE Algorithm

TMR	Value	Accuracy %
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
	Average	[XXX]
	10%	[XXX]
	90%	[XXX]
DMR	Value	Accuracy %
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]

[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
[XXX]	[XXX]	[XXX]
	10%	[XXX]
	90%	[XXX]
	average	[XXX]

The following specific results are noted:

- Worst case deviation of the AI image in all of the tests was [XXXX], which is well within the 0.35% acceptance criteria.

4.6.3 Serial Ports Failure Tests

The Serial Port Failure test was designed to simulate the failure of the transmit line and the receiver line. The transmit line was to left floating for 5 to 10 seconds, and then shorted to ground for 5 to 10 seconds and the following by shorting it to the receive line for 5 to 10 seconds.

Since HFC-6000 safety platform supports redundant communication, the failure of single serial port will have no impact to the overall performance. The results of the simulated C-Link and ICL failure tests are shown in the following sections. There was no impact to the BOE performance during those simulated failure tests.
Refer to ERD111 test results.

4.6.3.1 C-Link Failure Tests

These logs reflect the results obtained under the following test conditions: TX-line open; TX line shorted to ground; TX line shorted to RX line. An examination of these tables indicates that all averaged values remain within the 1.00 $\pm$ 10% second acceptance criterion for the BOE test without any stress or failure condition applied. Entries with * indicate that contact bounces occur on the channel during the BOE tests.
Refer to ERD111 test results.

4.6.3.2 ICL Failure Tests

The tables above contain a summary of SOE reports logged during execution of the ICL failure test under different combinations of conditions imposed for the ICL failure tests. The logged values

remained within the 1.00 ± 10% second acceptance criterion for the BOE test without any stress or failure condition applied. No anomalies were founded related to the PCBs covered by this report. Refer to ERD111 test results.

4.6.4 Serial Link Noise Test

The Serial Port Noise test was designed to superimpose a white noise signal on the transmit and the receive signal line of each serial link (one channel of the redundant pair) one at a time.
The acceptance criterion for this test is that the BOE signal characteristics do not deviate by more than ±10% while the failure condition is being imposed. Failure to communicate over the link under test while the failure is imposed does not constitute failure of the test. The C-Link noise and ICL noise test results are listed in the following.

Refer to ERD111 test results.

4.6.4.1 C-Link Noise Test

During execution of the Prudency C-Link noise test, a large amplitude noise signal was injected into the communication link of the test specimen. All records were within the specified 1.00 ± 10% second tolerance for BOE transitions.
Refer to ERD111 test results.

4.6.5 Fault Simulation Test

The Fault Simulation Test covers introduction of a simulated condition to trigger failover from the primary to the secondary controller. Demonstration of the failover function is covered by the Failover Operability test in the Operability Test Procedure (TP901-201-04, TP901-202-04, TP901-203-04). Therefore, this test was not intended to be run as a part of the Prudency Test Procedure (TP901-201-05, TP901-202-05,TP901-203-05).

4.7 Anomalies

There were no anomalies were found during the pre-qualification test. Summary
The pre-qualification test sequences were executed in the following order:

1. Application Object Test
2. System Integration (Set-up and Checkout) Test
3. TSAP Validation Test
4. Operability Test
5. Prudency Test

For each test, test results and data was analyzed. All tests were found to meet their respective acceptance criteria. Performance data collected during the operability and prudency tests were used to establish the baseline performance data for comparison with data collected during and after qualification tests to ensure no substantial degradation of the system in accordance with the standards.

A few anomalies related to contact bounce were found during execution of the BOE tests. However, these anomalies did not impact the overall system performance of the test specimen.

5.0 Quality Records

This document and related test results shall be preserved as nuclear records in accordance with QPP 7.1 "Quality Records".

6.0 Attachments

None