HF Controls

HF CONTROLS CORPORATION

HFC-6000 Control System

ERD111 – Control System Qualification Project

Post-Qualification after Retest Detail Report

TR901-200-05 Rev. A

Effective Date: 6/30/2011

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[ ]

Revision History

Date	Revision	Author	Changes
6/30/11	A	Y. Lu	Initial revision

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1.0 Purpose and Scope

1.1 Purpose

HFC-6000 platform has been qualified by NRC to be used as safety systems in US nuclear power plants. NRC has released the safety evaluation report (SER) for the HFC-6000 platform in April 2011. In the report, six open items were listed addressing some equipment qualification which needs to be clarified. Retest of environmental stress and EMI/RFI for this equipment was performed. This document summarizes the post-qualification test activities of the ERD111 specimen after environmental stress and EMI/RFI retests were performed.

1.2 Scope

The scope of this document covers the components listed in the SER for the HFC-6000 platform. These components are listed in the following table. Note: Modules listed in bold-faced font indicate that they are listed in HFC-6000 SER.

Table 1 – Components in the ERD111 Test Specimen

Quantity	Modular Type	Description
4	**PS, Jasper 24V**	**600W 24V Power Supply**
1	Rack, Jasper PS	8-slot Jasper PS Rack, 19"
2	HFC-FOT06	Fiber-Optic Transmitter
4	**HFC-ILR06**	**I/O Link Repeater/Terminator**
1	**HFC-BPC01-19**	**Controller Chassis backplane**
2	**HFC-BPE01-19**	**Expander Chassis backplane**
1	HFC-BPC03-08	3 Loop, 8 inch backplane
2	**HFC-SBC06**	**Main Controller**
1	**HFC-DPM06**	**Dual-Ported Memory**
2	HFC-SCG06	Communication Gateway
1	HFC-DPM06BP	Backplane Connected DPM06
1	HFC-DO16C	Solid State Output Card
2	**HFC-DC33**	**Special Function Card (120 vac output)**
4	**HFC-DC34**	**Special Function Card (125-vdc output)**
1	HFC-DC35	Special Function Card (120 vac output)
2	**HFC-AI4K**	**Pulse Input Card**
1	HFC-AI4K2	Pulse Input Card
1	**HFC-AI16F**	**Analog Input Card (4- to 20 mA)**
1	HFC-AI16FD	Analog Input Card (4- to 20 mA) (DSP)
2	**HFC-AO8F**	**Analog Output Card (4- to 20 mA)**
1	HFC-AI8LD	Thermocouple Input Card
1	**HFC-AI8M**	**RTD Input Card, 100 ohm**
4	HFC-AC36	Analog Input/Output Board
2	HFC-PCC06	Serial Channel Card
7	**HFC-DI16I**	**Digital Input Card with SOE**
1	**HFC-DO8J**	**Relay Output Card**
6	HFC-DO16J	Relay Output Card

2.0 References and Acronyms

2.1 References

DD0401	ERD111 Safety-Related Control System Qualification, Test Specimen Design Description, Rev. D
EPRI TR-107330	Generic Requirement Specification for Qualifying Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants, 1996
TP0402	ERD111 – Control System Qualification Project, Operability Test Procedure, Rev. L
TP0403	ERD111 – Control System Qualification Project, Prudency Test Procedure, Rev. G
TR901-200-02	ERD111 – Pre-Qualification before Retest Detail Report, Rev. A
VV0414	Nuclear Qualification Project ERD111 System, Master Configuration List, Rev. E

2.2 Acronyms

ASO	Application Software Objects
BOE	Burst of Events
CPC	Communication Protocol Controller
CR	Condition Report
CRC	Cyclical Redundancy Check
DCS	Distributed Control System
DDB	Dynamic Database
EMI	Electromagnetic Interference
EWS	Engineering Workstation
HAS	Historical Archiving System
HFC	Doosan HF Controls
HPAT	HFC Plant Automated Tester
ICL	Intercommunication Link
I/O	Input/Output
MCRT	Microsoft (Windows) CRT Workstation
LAN	Local Area Network
MCL	Master Configuration List
MTP	Master Test Plan
PCB	Printed Circuit Board
PCC	Peripheral Communication Controller
PLC	Programmable Logic Circuit
PROM	Programmable Read Only Memory
RFI	Radio Frequency Interference
RTD	Resistance Temperature Detector
SER	Safety Evaluation Report
SOE	Sequence of Events
TSAP	Test System Application Program
UCP	Universal Communication Protocol

3.0 Post-Qualification Test Sequences

Selected operability and prudency tests were repeated after the qualification stress tests as required in accordance with EPRI TR 107330 guidance. Results of the post-qualification tests are provided in the following sections. See Figure 1 for the post-qualification test sequences.

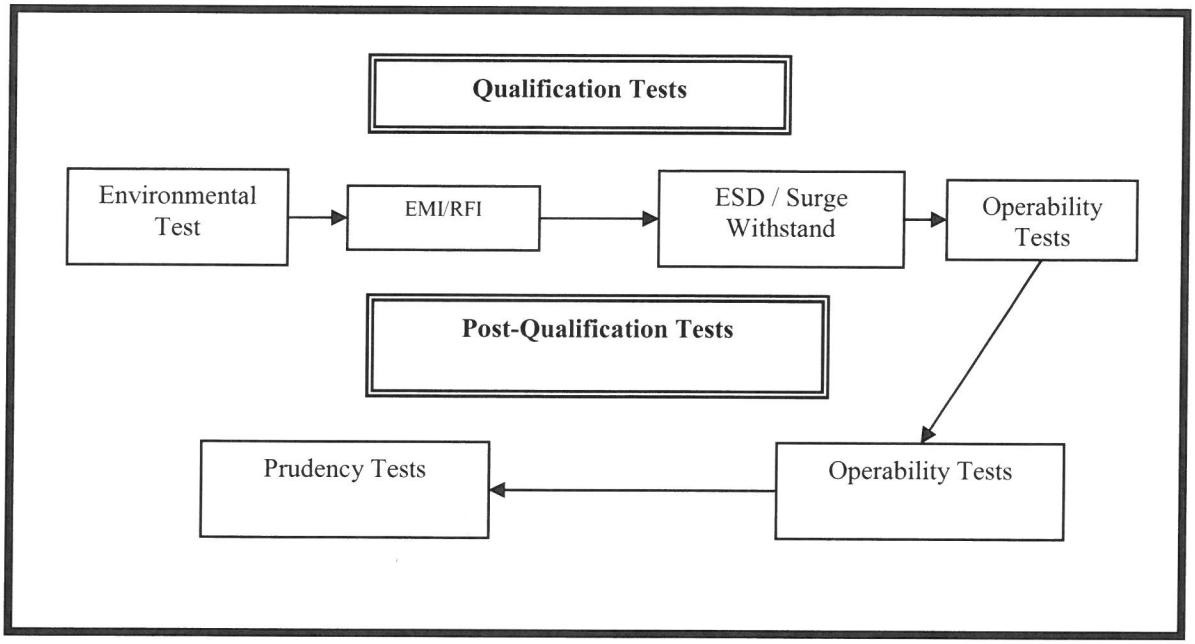

Figure 1 – Qualification and Post-Qualification Test Sequences

4.0 Post-Qualification Test Results

4.1 OPERABILITY TEST (TP0402)

The purpose of the operability tests was to collect the performance data for the system. The performance data was then used to compare against the baseline established in the pre-qualification.

- **Accuracy Test** – This test measured the accuracy of the AI and AO cards in the system.
- **Response Time Test** – This test measured the response time for discrete and analog inputs.
- **Discrete Input Operability Test** - This test verified the capability of discrete input channels to detect a transition in the input signal being monitored.
- **Discrete Output Operability Test** - This test verified the capability of discrete output channels to operate reliably within its specified loading conditions.
- **Communication Operability Test** – This test verified reliable data transfer over the ICL and C-Link.

- **Timer Test** – This test validated the timer functions supported by the system.
- **Test of Failure to Complete Scan** – This test validated that the system can be configured to failover to the redundant controller when an application could not complete once within one context switch.
- **Failover Operability Test** – This test demonstrated correct operation of the failover function.
- **Loss of Power Test** – This test demonstrated correct response of all I/O channels to loss of source power followed by reapplication of power to the system.
- **Power Interruption Test** – This test demonstrated the capability of the power modules to sustain system operation during a temporary (40-ms transient) power interruption.

4.1.1 Accuracy Test Results

4.1.1.1 AI16F 4 to 20-mA Analog Input Card

The test configuration for measuring analog input channel accuracy is shown in Figure 2. A static step analog algorithm, as shown in Figure 3 was generated by HPAT logic and fed into an Analog Output (AO) channel in the HPAT, which was wired to a 4-20 mA AI channel under test in TSAP. Table 2 shows the analysis of the test data and the calculated accuracy. Table 2 shows the average accuracy calculated is -0.03313% which shows that AI16F its specification of 0.1% and the accuracy requirement of 0.35% in EPRI TR 107330.

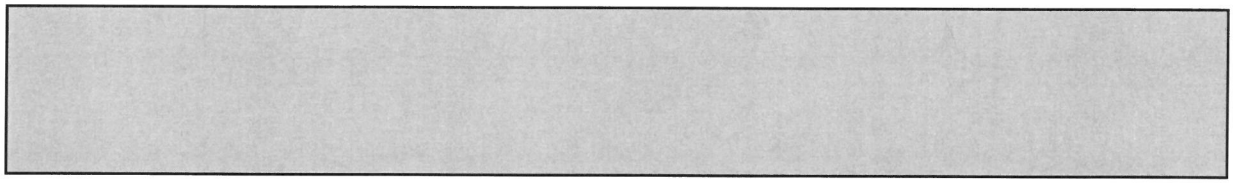

Figure 2 – AI Channel Accuracy Test Setup

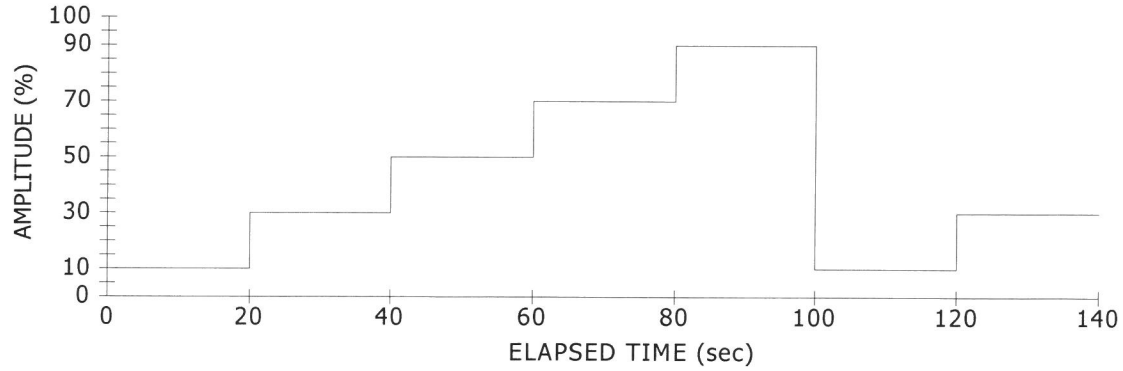

***Figure 3* – Algorithm for 4- to 20 mA Analog Channel Accuracy Test**

Table 2 – AI16F Manual Accuracy Test Results

Input	Test Signal (mA)	AI Image	Expected	Accuracy %
	[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]
			Average	[ ]

4.1.1.2 AO8F 4 to 20-mA Analog Output Card

Same test configuration as pre-qualification test was used for measuring analog output channel accuracy is shown in Figure 4. A static step analog algorithm (Figure 3) was generated by TSAP logic and fed into an AO channel under test. Table 3 shows the analysis of test data and calculation of accuracy for a 4-20 mA AO8F channel. The accuracy measurement taken as described shows that the AO8F card accuracy meets its specification of 0.1% and the 0.32% acceptance criterion for the module in EPRI TR 107330.

***Table 3* – AO8F Manual Accuracy Test Results**

Input (%)	Test Signal (mA)	AI Image	Expected	Accuracy
	[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]
			Average	[ ]

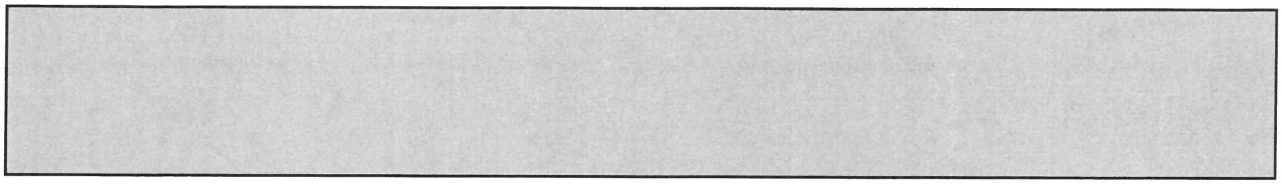

***Figure 4* – AO Channel Accuracy Test Setup**

4.1.1.3 AI8M 100 Ohm RTD Card

Same test configuration was used as in pre-qualification test for measuring analog input channel accuracy is shown in Figure 5. The RTD card under test is calibrated from 0 °C to 700 °C. A Fluke 743B with accuracy within ±0.01% of output + 0.04Ω was used for generating temperature input to the RTD input channels. The actual readings from the card are compared with the inputs to calculate accuracy for each RTD channel.

Table 4 and Table 5 show the analyses of test data and the resultant accuracies of the channels under test calculated as 100%*Absolute value of (Actual value – Expected value)/32767, in which 32767 represents the full RTD operational range. All 8 AI8M channels measured meet the acceptance criteria of ±0.285% (± 2 °C) accuracy in accordance with EPRI TR 107330.

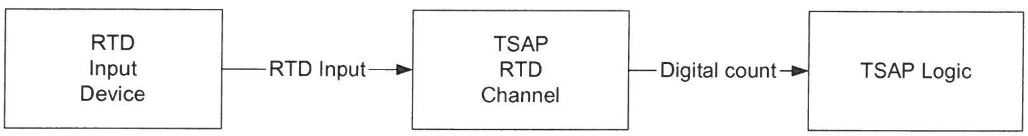

Figure 5 – RTD Channel Test Configuration

Table 4 – AI8M Accuracy Test Results for channels 1 to 4

AI8M		Actual Measurement				Accuracy (%)			
Input (Ω)	Expected	CH1	CH2	CH3	CH4	CH1	CH2	CH3	CH4
[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
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[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
					Avg.	[ ]	[ ]	[ ]	[ ]

Table 5 – AI8M Accuracy Test Results for channels 5 to 8

AI8M		Actual Measurement				Accuracy (%)			
Input (Ω)	Expected	CH5	CH6	CH7	CH8	CH5	CH6	CH7	CH8
[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
					Avg.	[ ]	[ ]	[ ]	[ ]

4.1.1.4 AI4K Pulse Input Card

The pulse card under test was located in Remote 1, Rack 4, Slot 11 and consisted of 4 channels. Channel 1 was tested in the rate mode and channel 3 was tested in the accumulate mode. In the accumulate mode, a prescaler value of 10 was used.

Channel 1 was run in the rate mode to confirm proper counting of various pulse signals. The results are provided in Table 6. Channel 3 was run in the accumulate mode to confirm proper counting of various pulse signals. The results are provided in Table 7. No significant deviations from the pre-qualification test. The same input ranges of the rate mode which met the 0.1% accuracy in pre-qualification show no degradation in post-qualification. Test results show accumulate mode meets its specification of less than 0.1% accuracy.

Table 6 – AI4K Rate Mode Accuracy Test Results

HFC-AI4K	Rate Mode		
Input Freq. (Hz)	Ch1	Expected	Accuracy (%)
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]

Table 7 – AI4K Accumulate Mode Accuracy Test Results

HFC-AI4K	Accumulate Mode				
Input Freq. (Hz)	Start	Final	Difference	Expected	Accuracy (%)
[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ] Average	[ ] [ ]

4.1.2 Response Time Test Results

4.1.2.1 Digital Response Time

[

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Table 8 – Digital Response Time Test Results

Results	**S2871030 SOE File**				
Algorithm	**Log Point**	**Minimum**	**Average**	**Maximum**	**Avg/14**
Free-Running	[ ]	[ ]	[ ]	[ ]	[ ]
Algorithm	[ ]	[ ]	[ ]	[ ]	[ ]
Trip Response	[ ]– [ ]	[ ]	[ ]	[ ]	

4.1.2.2 Analog Response Time Test

Same test algorithm was used as in pre-qualification test. See Figure 6. Since the HAS logger is limited to a one-second update rate, the SOE logger was used to record the data for this test. In order to produce signals that could be detected by the SOE input card, an external module triggered a relay at the leading and trailing edge of the analog trip signal.

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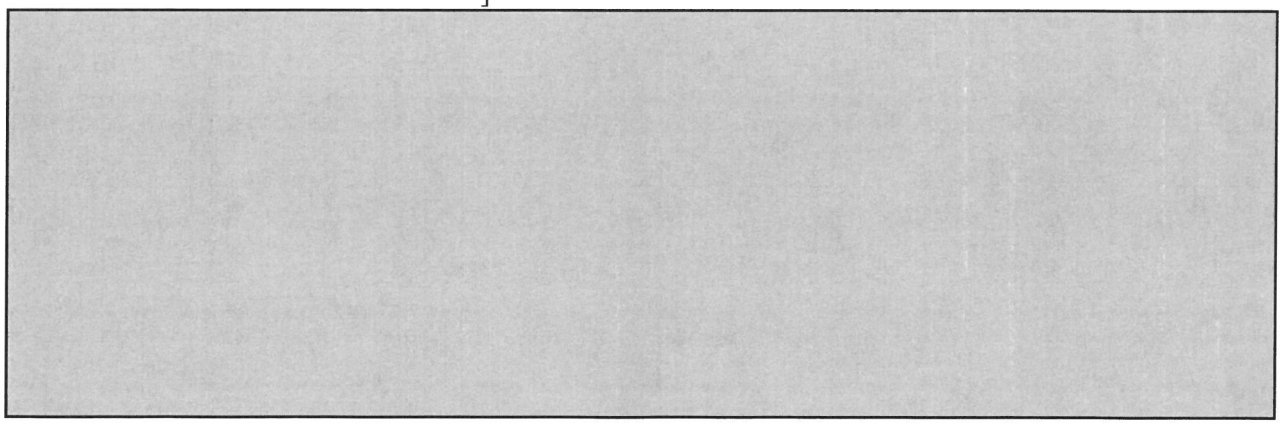

***Figure 6* – Analog Response Time Test Algorithm**

Table 9 – Analog Response Time Test Results

Response Delay	[ ]to [ ]		[ ] to [ ]	
	Leading Edge	**Trailing Edge**	**Leading Edge**	**Trailing Edge**
Response – S2871057, S2871058, S2871101 SOE File				
Minimum	[ ]	[ ]	[ ]	[ ]
Average	[ ]	[ ]	[ ]	[ ]
Maximum	[ ]	[ ]	[ ]	[ ]

4.1.3 Discrete Input Operability Test

The Discrete Input Operability test demonstrates the capability of each type of discrete input channel to detect a transition in the signal being monitored. In order to accomplish this, DI channels under test are subjected to an input signal whose voltage level is controlled by a manual rheostat. During the test, the set voltage level and the reset voltage level for each DI channel type were measured.

One channel of each DI card type to be qualified is tested for the following characteristics while the card is operating in the Test Specimen chassis:

- Set Voltage Threshold – the lowest voltage level that the DI image is switched from off to on.
- Maximum Input Voltage – the maximum voltage level the DI channel to remain stable.
- Dropout Voltage (reset voltage level) – is the voltage level that the DI image is switched from on to off and remained reset.
- The voltage to the DI channel was dropped from the reset voltage level to 0 to prove the channel remains reset.
- Each DI channel being tested was turned on to prove input signal isolation.

Same channels as in pre-qualification test were used for each digital input card type.

Table 10 – Discrete Input Channel Test Results

Test	Test Results (Average on 3 measurements)		
	DI16I	DC33	DC34
Set Voltage Threshold	[ ]	[ ]	[ ]
Maximum Input Voltage	[ ]	[ ]	[ ]
Dropout Voltage	[ ]	[ ]	[ ]

The results of the discrete input operability test show the following:

- [

]

4.1.4 Discrete Output Operability Test

The Discrete Output Operability test demonstrated the capability of each type of discrete output channel to operate within its specified range of loading conditions. In order to accomplish this, the channel under test was energized while connected to a simulated field load that imposes maximum loading on the channel. The test demonstrated the capability for individual channels to sustain such maximum loading conditions without failure and without affecting operation of adjacent channels.

4.1.4.1 Relay DO Channel Operability Test

Same test method as in pre-qualification was used. The average resistance for all eight channels was recorded and listed in Table 11.

Table 11 – DO8J Relay DO Output Characteristics

Card Type Under Test	HFC-DO8J
Contact Resistance (Average of 4 channels)	[ ]
Test Load Applied	[ ]
Each Channel Switches Under Load	[ ]

The results show all 8 DO channels of DO8J meet their required performance criteria.

4.1.4.2 120 VAC DO Channel Operability

Same test method as in pre-qualification was used. Data was collected and screen captures were recorded from an oscilloscope during the post-qualification tests. Based on the results collected, the 120 vac discrete output channel operates over the range of 90 vac at 47 Hz to 130 vac at 63 Hz as expected.

4.1.4.3 125 VDC DO Channel Test

Same test method as in pre-qualification was used. Data was collected and screen captures were recorded from an oscilloscope during the post-qualification tests. Based on the results collected, the 125 vdc discrete output channel operates over the range of 90 vdc to 130 vdc as expected.

4.1.5 Communication Operability Test

The Communication Operability Test was conducted during the pre-qualification phase of testing and then repeated before, during and after each qualification test.

The HFC-6000 control system includes [

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This test used link error counters to provide a basis for evaluating the quality of communication on these links. The overall test method consisted of recording the count value of the error counters at the start and end of a test period and interpreting the total accumulated error count as the measure of communication reliability. The automatic tests were run to provide background activity for the communication test.

4.1.5.1 ICL Error Counters

The ICL link error counters can be read through an HFC software utility – [

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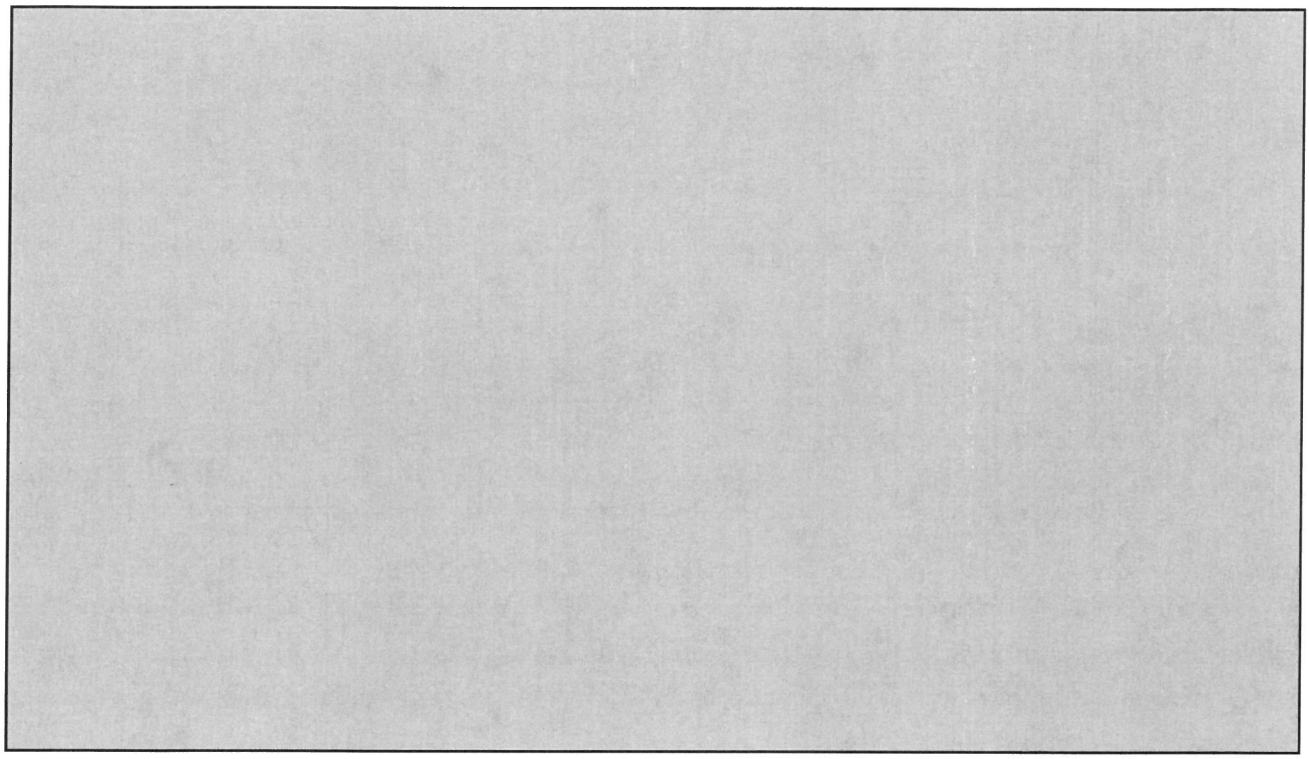

Figure 7 – Memory Editor Screenshots before and after Post-Qualification Tests

Figure 7 shows the screen captures of HFC memory editor before and after post-qualification tests. As indicated in the figures, the ICL error counter did not increase during the post-qualification tests. Therefore, no ICL communication errors were reported. The ICL communication was validated in accordance with the acceptance criteria.

4.1.5.2 C-Link Error Counters

[

] The HAS database showed the values of these two counters remained zero during the operability tests for the ERD111 test specimen. Therefore, C-Link communication also met the acceptance criteria for the communication operability test.

4.1.6 Timer Test

Same test method as in pre-qualification was used. The results of the automated timer test are shown in the following table:

Table 12 – Time Test Results

Averaged Period	[ ]		[ ]	
	Avg Value	**Accuracy**	**Avg Value**	**Accuracy**
On	[ ]	[ ]	[ ]	[ ]
Off	[ ]	[ ]	[ ]	[ ]
Period Total	[ ]	[ ]	[ ]	[ ]

The specified acceptance criterion for the timer function is that timer accuracy shall vary by no more than ±1% of the preset value or by more than ±3 scan cycles. Table 12 indicates that the *averaged* accuracy meets the ±1% acceptance criterion for all timer periods: 1s OFF to ON, 1s ON to OFF, 5s OFF to ON, 1s OFF to ON.

4.1.7 Test of Failure to Complete Scan

This test validated that the system could be configured for failover to the redundant controller when an application did not complete a full scan within one context switch. [

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4.1.8 Failover Operability Test

The purpose of this test was to verify proper failover of the redundant controllers. A screen capture of the oscilloscope for Sane signal of channel 1 (primary controller) and PRI signal of channel 2 were taken during the failover tests. This screenshot shows the delay was about 66.0µs. See the following figure.

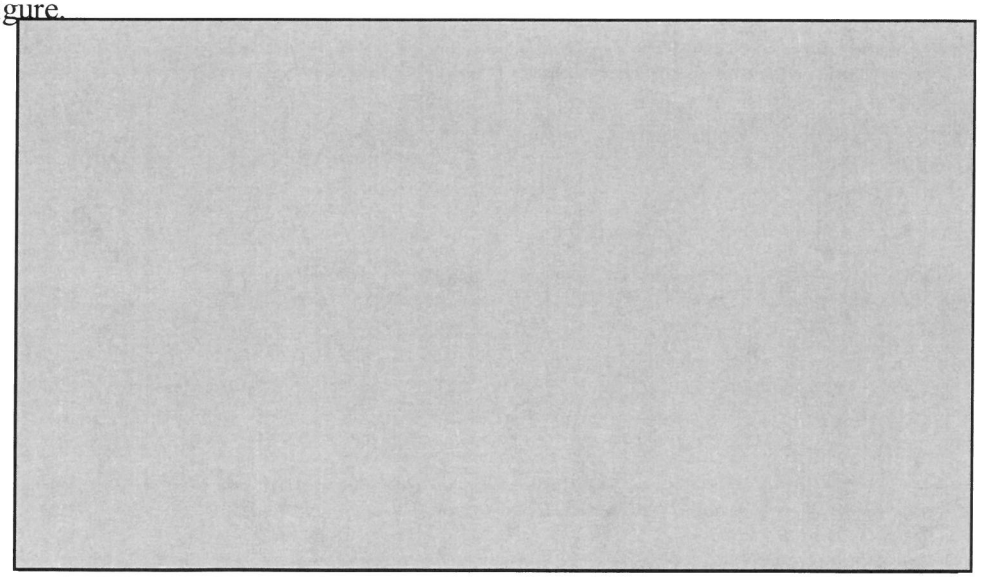

Figure 8 – Failover Primary SANE and Secondary PRI signals

Tests were also performed to measure the effect of the failover on both digital and analog loops. These failover tests focused on capturing the magnitude of disruption to analog and additional values from the I/O cards and system performance during failover.

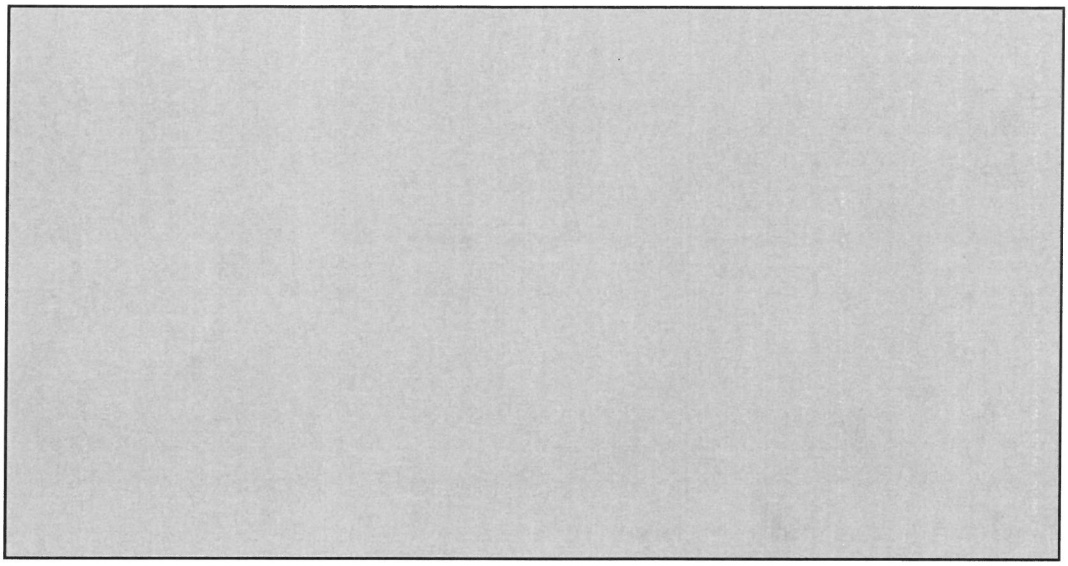

Figure 9 – AI16F Accuracy During Failover

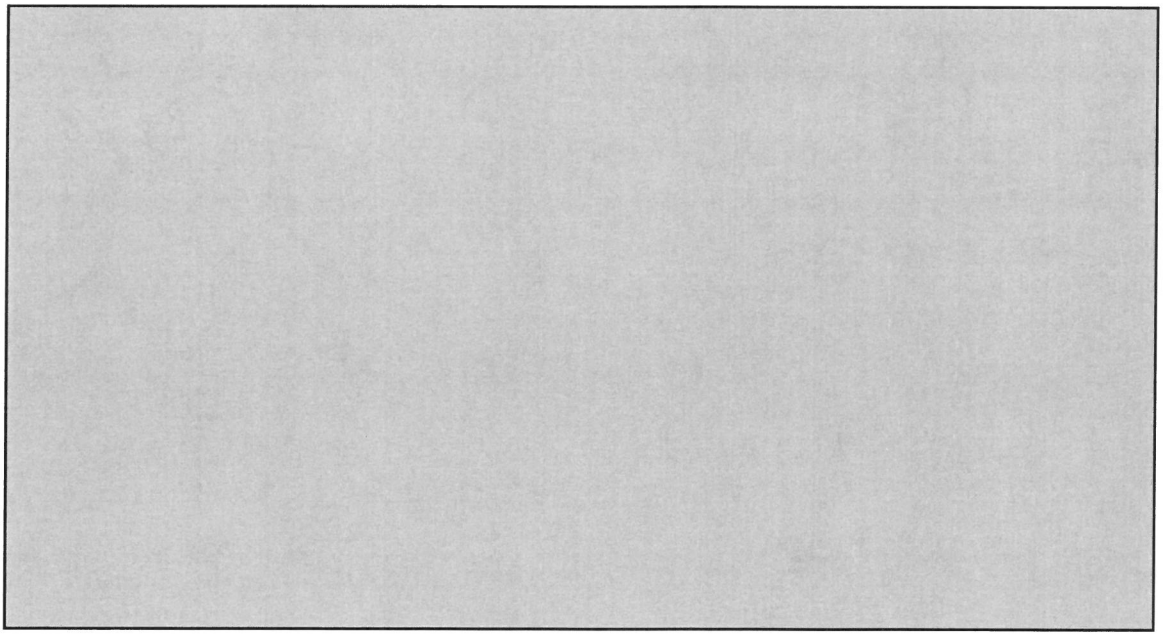

Figure 10 – AI8M Accuracy During Failover

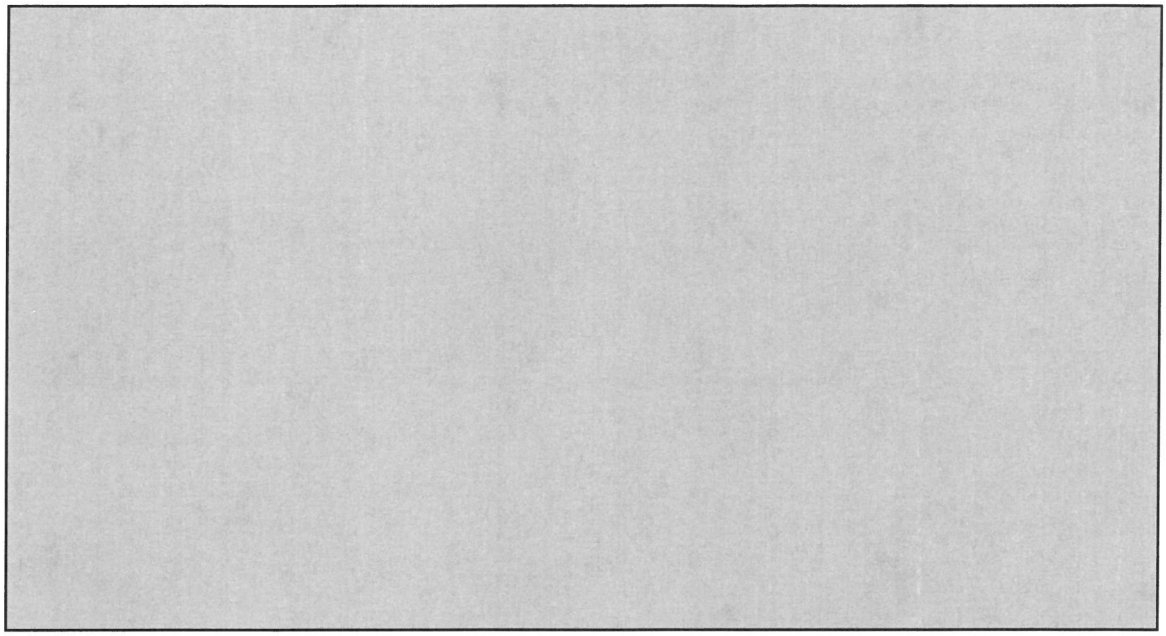

Figure 11 – AO8F Accuracy During Failover

These figures show there was no impact on stable analog values or analog values in transition during failover.

[

] No significant difference between the settling of the PV time with and without a failover event.

[

] No impact of the failover event was found.

All these tests and test results provided sufficient data that the ERD111 specimen meets the failover operability acceptance criteria.

4.1.9 Loss of Power Test

The purpose of the test was to demonstrate that output channels went to their inactive levels when power was lost and that they remained in those states until the controller completed its internal initialization. This test was run during post-qualification, at the end of the high temperature and low temperature phases of the environmental stress test.

The acceptance criterion in EPRI TR 107330 stated that all output channels return to de-energized state during power loss and all output channels remain in failsafe state until operator initiates operation. The manual data taken in Table 13 verified that these reactions were taking place and that the system handled loss of power properly.

Table 13 – Loss of Power Manual Data

Verification Criteria	Points Tested
AO channels are open (0 mA output)	[ ]
Power Outputs are open (120 vac, 125 vdc)	[ ] and [ ]
DO channels are de-energized	[ ]

The following figures show the automated algorithms resume operation without operator intervention.

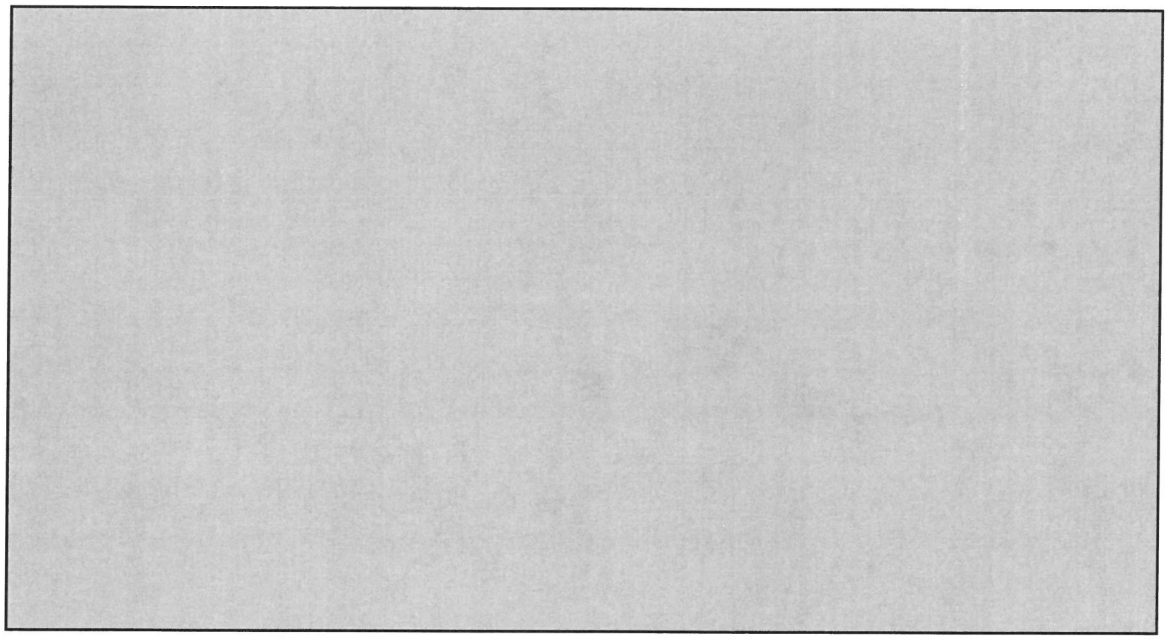

Figure 12 – AI16F Automated Accuracy During Power Loss

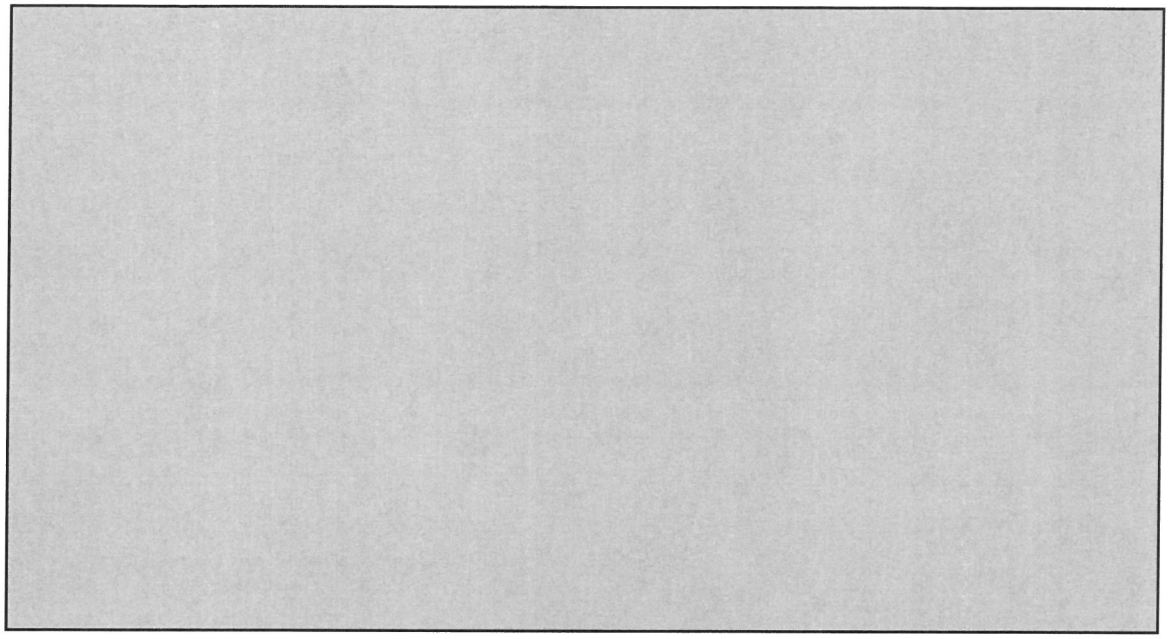

Figure 13 – AI8M Automated Accuracy During Power Loss

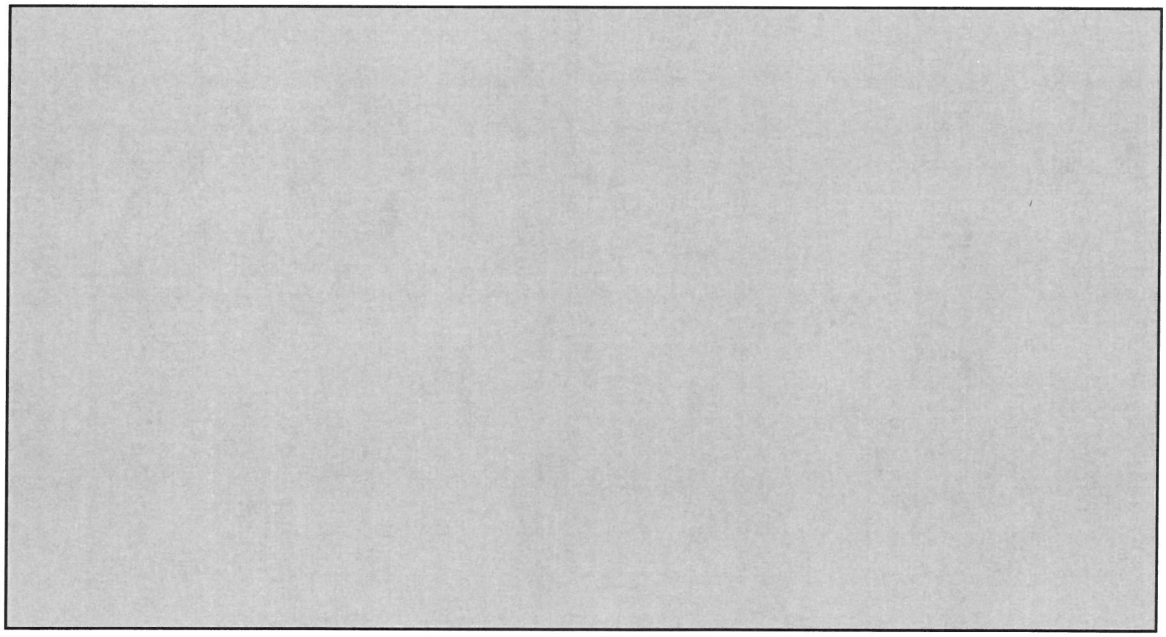

Figure 14 – AO8F Automated Accuracy During Power Loss

[

] The SOE records were started during the power outage and recorded data for several minutes after power was restored. No output from the ERD111 test system was logged by either the SOE or the HAS during the power outage. During the first several minutes following restoration of power, the following transitions are noted to occur:

- [

]

The test results showed that after the loss of power:

1. All AO channels are open.
2. All power output channels are open.
3. All solid state relay DO channels are open.
4. All mechanical relay DO channels are de-energized.

After power is restored, all operations come back to normal:

- The performance ranges of the digital and analog response time algorithms are within the limits previously received.
- The averaged values for the timer test are within the ranges previously recorded.

These test results provide evidence that the ERD111 test specimen meets the acceptance criteria for loss of power.

4.1.10 Power Interruption Test

The power interruption test subjects the system to a 40ms interruption in source AC power to demonstrate the capability of the system to continue functional operation during switchover to a backup power source. The test was conducted during post-qualification, during the high temperature and low temperature phases of the environmental test with the following background conditions configured:

- Static points were configured to known states.
- Automatic accuracy test, response time test, and timer test were running.

The following acceptance criteria are specified for this test:

- No controller resets.
- No static DO channel changes state.
- No static AO point changes its value by more than 5%.
- Logged parameters for all of the automated tests remain within tolerance

The controller did not reset during the power interruption. The following tables and figures show the test results satisfy the acceptance criteria for the power interruption tests. Jasper 24V power supply provided support of 40ms interruption time without failure.

Table 14 – Timer Functions During Power Interruption Test

S2891314	Averaged Period	[ ]		[ ]	
		Avg Value	Accuracy	Avg Value	Accuracy
During Interruption	On	[ ]	[ ]	[ ]	[ ]
	Off	[ ]	[ ]	[ ]	[ ]
	Total	[ ]	[ ]	[ ]	[ ]

Table 15 – Digital Response Time during Power Interruption Test

SOE File S2891314	During Interruption			
Algorithm	Log Point	Minimum	Average	Maximum
Response Time	[ ]–[ ]	[ ]	[ ]	[ ]

Table 16 – Analog Response Time during Power Interruption Test

SOE File S2891314	During Interruption			
Algorithm	Log Point	Minimum	Average	Maximum
Response Time	[ ]–[ ]	[ ]	[ ]	[ ]

The above tables and figures show that during power interruption, no impact was made to the system. System performance data were all in line with data collected when power input was stable.

In addition to the above dynamic test results, all the static points monitoring by HAS did not show any variation. No anomalies were found during the power interruption test.

4.2 Prudency Tests (TP0403)

The prudency testing validates the PLC/PCB system performance in highly dynamic conditions. In addition, data collected from the Burst of Events (BOE) for analog input and output cards provide different sets of performance data.

The Prudency test was conducted again during the post qualification phase of testing to compare against the establish baseline. During subsequent qualification tests, the BOE test and the other tests were repeated at various points in accordance with the EPRI standards to identify any performance degradation from the performance baseline.

- **Burst of Events Test** - This test consisted of the simultaneous activation of a significant proportion of input and output channels in accordance with EPRI TR-107330 paragraph 5.4.A. This test was automated and was typically run as a continuous background operation for selected qualification tests.

- **Serial Port Failure Test** – The test specimen has two redundant serial communication links. For each redundant link, this test imposed three simulated failures on one cable at a time: link open, transmit line shorted to ground, and transmit line shorted to receive line.

- **Serial Port Noise Test** - This test introduced a white noise signal on each of the serial links one port at a time.

- **Fault Simulation Test** – This test covered introduction of a simulated failure condition to trigger failover from the primary to the secondary controller. The intent of this test was covered by the Failover Operability Test (TP0402), and has not been duplicated in this test.

4.2.1 Digital Input/Output BOE Test

The digital BOE test was logged a number of times during the execution of the Prudency tests. Apart from some contact bounces, every transition was present within the stipulated tolerance of 1.000±10% second, and no link or station alarm was present during the test interval. (The greatest average deviation recorded was 0.0426 second.)

These tables were divided into two sets of points. These two sets of points represent the different phase relationship between the BOE driving signals. [
] These signals were slightly asymmetric due to the characteristics of the timer function in the HPAT. This deviation produced a small part of the reported deviation, and the remainder was produced by the processing of the ERD111 Test Specimen and the TSAP logic. Entries with * indicate that contact bounces occur on the channel during the BOE tests.

Table 17 – S2910831 – 10/18/2010 at 8:31AM

Signal Source	Point Logged	Time HI	Time LO
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
Signal Source	**Point Logged**	**Time HI**	**Time LO**
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]

Table 18 – **S2910909 – 10/18/2010 at 9:09 AM**

Signal Source	Point Logged	Time HI	Time LO
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
Signal Source	**Point Logged**	**Time HI**	**Time LO**
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]

Table 19 – S2910922 – 10/18/2010 at 9:22 PM

Signal Source	Point Logged	Time HI	Time LO
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
Signal Source	**Point Logged**	**Time HI**	**Time LO**
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]

4.2.2 Analog BOE Test

The analog BOE test is based on two different hardware arrangements and two different TSAP arrangements to produce three different test channels as follows:

- [

  ]

The test channels are driven by the same HPAT algorithm, and all three are logged by the HAS. The following HAS log points are used for this test:

- [

  ]

The test configuration used the same algorithm to process the digital data and any difference between data entries was the result of the hardware processing the data or the path through the application code.

Table 20 – BOE Algorithm – HPAT to AI16F, AO8F to HPAT

[ ]		[ ]			[ ]		
Time	**Value**	**Time**	**Value**	**Δ**	**Time**	**Value (Avg)**	**Δ**
[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]

No significant deviations from the pre-qualification analog BOE test results.

4.2.3 Serial Port Failure Tests

The Serial Port Failure test was designed to simulate the failure of the transmit line and the receiver line. The transmit line was left floating for 5 to 10 seconds, and then shorted to ground for 5 to 10 seconds and then shorted to the receive line for 5 to 10 seconds.

Since HFC-6000 safety platform supports redundant communication, the failure of single serial port will have no impact to the overall performance. The results of the simulated C-Link and ICL failure tests are shown in the following sections. There was no impact to the BOE performance during those simulated failure tests.

4.2.3.1 C-Link Failure Tests

Tables below from Table 21 to Table 23 contain a summary of SOE reports logged during execution of the C-Link failure tests. These logs reflect the results obtained under the following test conditions: TX-line open; TX line shorted to ground; TX line shorted to RX line. An examination of these tables indicates that all averaged values remain within the 1.000±10% acceptance criterion for the BOE test without any stress or failure condition applied. Entries with * indicate that contact bounces occur on the channel during the BOE tests.

Table 21 – S2910932 – TX Line Open– 10/18/2010 9:32 AM

Signal Source	Point Logged	Time HI	Time LO
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
Signal Source	**Point Logged**	**Time HI**	**Time LO**
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]

Table 22 – S2910935 – TX Line Short to GND– 10/18/2010 9:35 AM

Signal Source	Point Logged	Time HI	Time LO
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
Signal Source	**Point Logged**	**Time HI**	**Time LO**
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]

Table 23 – S2910938 – TX Line Short to RX– 10/18/2010 9:38 AM

Signal Source	Point Logged	Time HI	Time LO
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
Signal Source	**Point Logged**	**Time HI**	**Time LO**
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]

4.2.3.2 ICL Failure Tests

Table 24 – S2910956 – ICL TX Line Open–10/18/2010 9:56 AM

Signal Source	Point Logged	Time HI	Time LO
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
Signal Source	**Point Logged**	**Time HI**	**Time LO**
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]

Table 25 – S2911000 – ICL TX Line Short to GND–10/18/2010 10:00 AM

Signal Source	Point Logged	Time HI	Time LO
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
Signal Source	**Point Logged**	**Time HI**	**Time LO**
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]

Table 26 – S2911015 – ICL TX Line Short to RX– 10/18/2010 10:15 AM

Signal Source	Point Logged	Time HI	Time LO
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
Signal Source	**Point Logged**	**Time HI**	**Time LO**
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]

4.2.4 Serial Link Noise Test

The Serial Port Noise test was designed to superimpose a white noise signal on the transmit or the receive signal line of each serial link (one channel of the redundant pair) one at a time.

The acceptance criterion for this test is that the BOE signal characteristics do not deviate by more than ±10% while the failure condition is being imposed. Failure to communicate over the link under test while the failure is imposed does not constitute failure of the test. The C-Link noise and ICL noise test results are listed in the following.

4.2.4.1 C-Link Noise Test

Table 25 contains a summary of SOE data logged during execution of the Prudency C-Link noise test, during which a large amplitude noise signal was injected into the communication link of the test specimen. All records were within the specified 1.000±10% tolerance for BOE transitions.

Table 27 – S2911054 – C-Link Noise Test – 10/18/2010 10:54 AM

Signal Source	Point Logged	Time HI	Time LO
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
Signal Source	**Point Logged**	**Time HI**	**Time LO**
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]

4.2.4.2 ICL Noise Test

Table 28 – S2911058 – ICL Noise Test – 10/18/2010 10:58 AM

Signal Source	Point Logged	Time HI	Time LO
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
Signal Source	**Point Logged**	**Time HI**	**Time LO**
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
Note: * Entry contains contact bounce record.			

Table 28 contains a summary of SOE data logged during execution of the Prudency ICL noise test. All records were within the specified 1.000±10% tolerance for BOE transitions.

4.2.5 Fault Simulation Test

The Fault Simulation Test covers introduction of a simulated condition to trigger failover from the primary to the secondary controller. Demonstration of the failover function is covered by the Failover Operability test in the Operability Test Procedure (TP0402). Therefore, this test was not intended to be run as a part of the Prudency Test Procedure (TP0403).

4.3 Anomalies

No anomalies found during the post-qualification test. Similar to pre-qualification test, only contact bounces were found during the digital BOE tests. These contact bounces could be filtered out easily using HFC-6000 EWS software tools.

5.0 Summary

The post-qualification test sequences were executed in the following order:

1. Operability Test
2. Prudency Test

For each test, test results and data were analyzed. All tests were found to meet their respective acceptance criteria. No substantial degradation of the system after the qualification tests were performed in accordance with the standards.

6.0 Quality Records

This document and related test results shall be preserved as nuclear records in accordance with QPP 7.1 "Quality Records".

7.0 Attachments

None