HF Controls

HFC-6000 Control System

ERD1192 – Control System Qualification Project

Operability Test Procedure Remote 03 FPC08

TP901-301-06 Rev B

Effective Date _____

Author _____

Reviewer _____

Approval _____

[XXXXXXXXXXXX]

Revision History

Date	Revision	Author	Changes
11/7/11	A	R. McClanahan	Initial Release
03/27/12	B	D. Briner	CR 2012-0143

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1.0 PURPOSE AND SCOPE

Selected components of the HFC-6000 product line will be configured as a redundant controller (Test Specimen) including redundant HFC-FPC08 controllers and I/O modules mounted in a single chassis and housed in the same cabinet assembly. The complete Test Specimen (controllers, I/O modules, and cabinet assembly) will be subjected to a battery of tests intended to qualify it as a controller configuration to be used in safety-related applications. The following set of Operability tests were developed from test requirements defined by EPRI TR-107330.

- **Accuracy Test** - This test verifies that analog I/O modules in the test specimen meet the accuracy and linearity requirements. (EPRI TR-107330 references: 4.3.2.1, 4.3.3.1, 5.3.A, 6.2.2.B.2, B.6, and B.8)

- **Response Time Test** – This test will measure the response time for discrete and analog inputs from the leading edge of the input to the leading edge of the resulting output. (EPRI TR-107330 references: 4.2.1.A, 5.3.B, 6.2.2.B.5)

- **Discrete Input Operability Test** - This test will verify the capability of discrete input channels to respond to simulated input signals. (EPRI TR-107330 references: 5.3.C, 6.2.2.B.6)

- **Discrete Output Operability Test** - This test will verify the capability of discrete output channels to produce output signals having specified voltages and currents. (EPRI TR-107330 references: 5.3.D, 6.2.2.B.8)

- **Communication Operability Test** – This test will verify reliable data transfer over all serial communication links associated by the Test Specimen. (EPRI TR-107330 references: 5.3.E)

- **Timer Test** – This test will verify the accuracy of the timer function accessible to the TSAP. (EPRI TR-107330 references: 5.3.G, 6.2.2.B.3)

- **Failure To Complete Scan Detection** – This test will verify the capability of the system software to detect failure to complete at least one execution of the application program during each context switch interval. (EPRI TR-107330 references: 4.2.3.7.A, 4.4.6.3.C, 5.3.H)

- **Failover Test** – This test demonstrates operability of the failover hardware for redundant controllers (EPRI TR-107330 references: 4.3.4.7, 5.3.H).

- **Loss of Power Test** – This test will demonstrate correct response of all I/O channels to loss of source power followed by reapplication of power to the system. (EPRI TR-107330 references: 5.3.J)

- **Power Interruption Test** – This test will demonstrate the capability of the power modules to sustain system operation during a temporary (transient) power interruption. (EPRI TR-107330 references: 4.6.1.1.F, 5.3.K)

- **Power Quality Tolerance Test** – This test will demonstrate the capability of the Test Specimen to continue normal operation over a range of source power voltages and frequencies. (EPRI TR-107330 References: 4.2.3.7.B, 4.6.1, 6.4.3, 6.4.4.F)

These tests are designed to exercise control system functions to provide a basis for evaluating its performance. The complete set of tests will be run prior to the actual qualification tests to establish a performance baseline for the system. This performance baseline will then be used as the basis for evaluating system performance during and/or following each of the qualification tests to be accomplished.

2.0 REFERENCES

2.1 INDUSTRY STANDARDS

EPRI TR-107330	Generic Requirements Specification for Qualifying a Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants, December 1996

2.2 RELATED PLANS AND PROCEDURES

TP901-301-02	ERD1192 Integration Test Procedure, Rev. B
VV901-300-02	ERD1192 Master Test Plan, Rev. B
VV901-304-01	ERD1192 Master Configuration List, Rev. A
VV901-304-03	ERD1192 Test Specimen Design Specification Remote 3 FPC08, Rev. A

2.3 SUPPORT DOCUMENTATION

500620-01	ERD1192 Remote Loop Layout, Rev. G
500621-01	ERD1192 Power Distribution, Rev. F
500640-03	ERD1192 TSAP Logic Diagrams Remote 3, Rev. C
500638-01	ERD1192 HPAT Schematic Wiring Diagrams Remote 2, Rev. D

2.4 HFC INTERNAL STANDARDS AND PROCEDURES

Implementation of HFC test programs is based on the current version of the following internal procedures:

QPP 5.1	Review and Approval of Quality Documents
QPP 5.2	Preparation of Procedures
QPP 11.1	Test Control
WI-ENG-003	Configuration Management
WI-ENG-205	Develop Software/Firmware Test Procedure

2.5 SPECIAL TERMS, ABBREVIATIONS, AND ACRONYMS

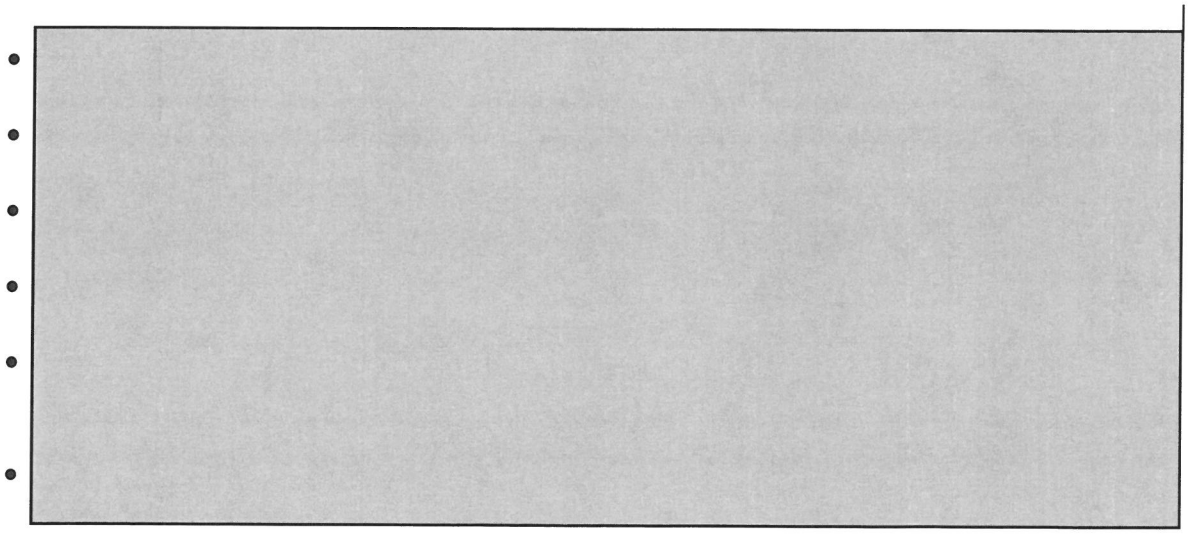
C-Link	Communication Link
BOE	Burst of Events
HAS	Historical Archiving System
HPAT	HFC Plant Automated Tester
ICL	Intercommunication Link
M&TE	Measuring and Test Equipment
RH	Relative Humidity
SOE	Sequence of Events
Test Specimen	A specific combination of hardware and software components to be subjected to specified test conditions
TSAP	Test System Application Program

3.0 PREREQUISITES

The following paragraphs provide detailed instructions for setup and performance of each Operability test. Operability tests may be run individually or concurrent with other tests. To the maximum extent possible, the individual Operability tests will be automated so that a test engineer can start/stop the selected tests while a qualification test is in progress. However, certain portions of operability test will either disrupt operation of the Test Specimen as a whole or will require direct access to the Test Specimen hardware. Such a test will not be automated or run concurrently with any other test.

3.1 EQUIPMENT REQUIRED

A detailed listing of hardware and software components of the Test Specimen is provided in VV901-302-02, Master Configuration List. Detailed requirements for component assembly and interconnection are provided by the engineering drawing package. The equipment listed below will be required during performance of this test. Test personnel shall verify that all test and measuring equipment are capable of producing the level of accuracy required by the specific test being performed and that the calibration for the M&TE to be used is current.



- [redacted]
- [redacted]

Record all test equipment used during execution of this test in attachment 7.1, Test Equipment Log.

3.2 ENVIRONMENTAL CONDITIONS

This test will be conducted under various environmental conditions. During prequalification testing, the test will be conducted under normal operating conditions for the Test Specimen, as indicated below. During the qualification tests, required environmental conditions are stipulated within the procedures governing those tests.

Temperature	50 deg to 104 deg F
Relative Humidity	7% to 90% non-condensing

3.3 TEST PERSONNEL

The set of Operability tests will be conducted at the in-house test facility of HFC following completion of the TSAP Validation Test and at vendor facilities during qualification testing. All of the testing and monitoring functions will be conducted by one or more qualified HFC test engineers/technicians both at the HFC facility and at vendor facilities during qualification testing.

3.4 PRECAUTIONS

WARNING

Certain I/O circuits are energized with high voltages and may carry potentially hazardous current loads. Exercise caution whenever working around exposed terminals or circuitry.

3.5 RED-LINE POLICY

The HFC policy for entering red-line corrections into a test procedure are presented in WI-ENG-815, "Red Line" Procedure. Such entries may be used to correct errors of content and procedural sequence in test documents or in engineering drawings to prevent disruption of a test in progress.

3.6 TEST SETUP REQUIREMENTS

3.6.1 Test Specimen Setup

1. Verify that the copy of the Operability Test Procedure test in hand is a controlled copy of the latest revision according to Document Control records.

2. Verify that all integration testing has been completed successfully.

3. Verify that the TP901-301-04, ERD1192 TSAP Validation Test Remote 3 FPC08, has been completed successfully.

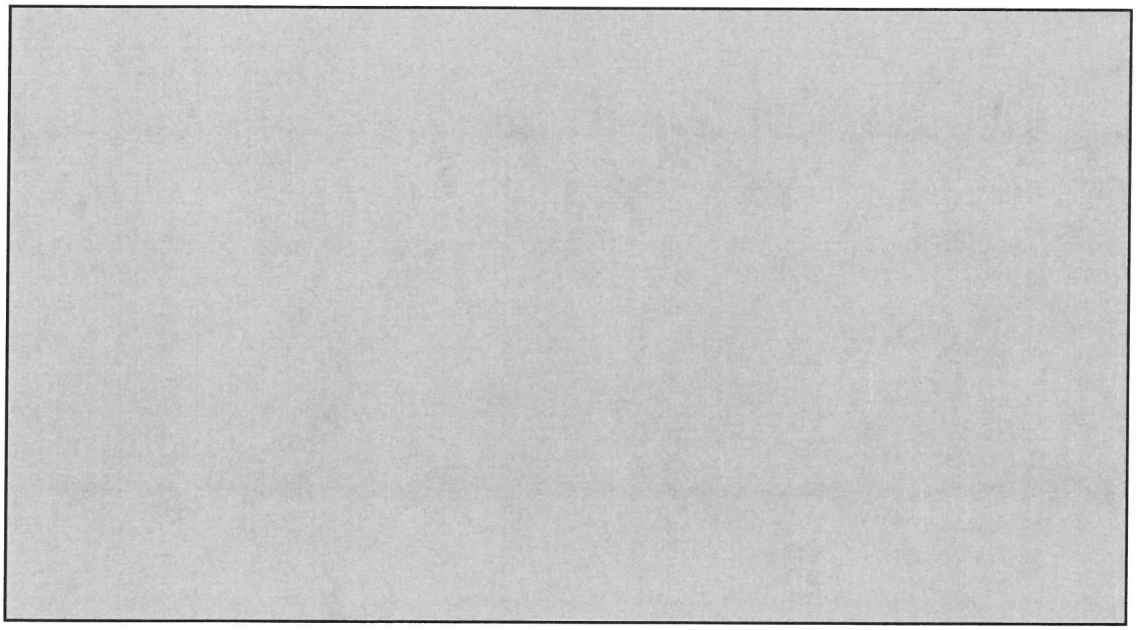
Test setup is complete: _____
Name/Date

3.6.2 SOE Point Configuration

An SOE logger will be used to monitor high speed (up to ±1 ms resolution) logic transitions of selected DO and AO channels during operation of the Operability tests. Table 1 lists SOE point assignments for both Operability and Prudency test points. The following procedure describes the sequence of steps necessary to configure the SOE logger prior to running the Operability tests for the first time or following reassembly of the Test Specimen in a vendor's test facility.

Use the SOE Logger utility of the EWS to configure the SOE as follows:

1.
2.
3.
4.
5.



SOE setup is complete: _____
Name/Date

Table 1. ERD1192 FPC08 Points Configured for SOE Logging

Description	Output Point	Input Point	HPAT SOE Log Point	Chatter Box Point
Digital Response Time Test				
Analog Response Time Test				
Timer Operability Test				
Failure to Complete Scan Operability Test				
Digital BOE Test				

3.6.3 HAS Configuration

The HFC HAS software utility will be used for logging the value of analog signals as well as digital signals that do not require a time resolution of less than 1 second. Table 2 lists the combination of points selected for HAS logging. (Table 2 includes log points for both Operability and Prudency BOE tests.) The HAS log points shall be configured and verified during the first execution of the Operability and Prudency tests.

1.

2.

3.

Table 2. Points Configured for HAS Logging

Description	Output Point	Input Point	HAS Log Point	Chatter Box Point
Analog Accuracy Test Points				
Communication Operability Test				
Equation Operation				
Static Analog Loops				
PID Loop Static Test				
Analog BOE Test				

HAS setup for ERD1192 is complete: _____

Name/Date

4.0 OPERABILITY TEST PROCEDURE

Each of the Operability tests provides a separate evaluation for a specific aspect of the Test Specimen performance and operation. No fixed sequence of execution is assumed or implied by the order of specific tests in this document.

4.1 ACCURACY TESTS

The TSAP contains a stair-step analog algorithm (Figure 1) to support automated testing of analog I/O channels. This wave form drives one AO point associated with each remote, and the resulting analog output signal is fed back into a separate AI point for each remote. The AO channels are rated for 4 to 20 mA, but the AI channels are rated for 0 to 5 v. Hardware modules inside the test cabinet provide the necessary signal conversion. The test algorithm is fully automated and will be run under two conditions:

- Under normal operating conditions with no abnormal stress applied
- While specified qualification tests are in progress

This procedure includes both manual and automated test sequences. The complete accuracy test will be conducted during both pre-test and post-test phases. Only the automated test sequences will be executed during the qualification tests. Table 2 lists which signal images will be logged by the HAS. Repetition of a manual accuracy test prior to the start of a qualification test will not be necessary unless the AO module must be replaced.

A similar test algorithm cannot be configured for RTD and TC AI points. A simulated signal source will be used for manual verification of module accuracy during the pre test phase. During qualification tests, one each of these channels will be connected to an actual input device (RTD element or E-type thermocouple), and the real devices will measure the ambient temperature inside the cabinet.

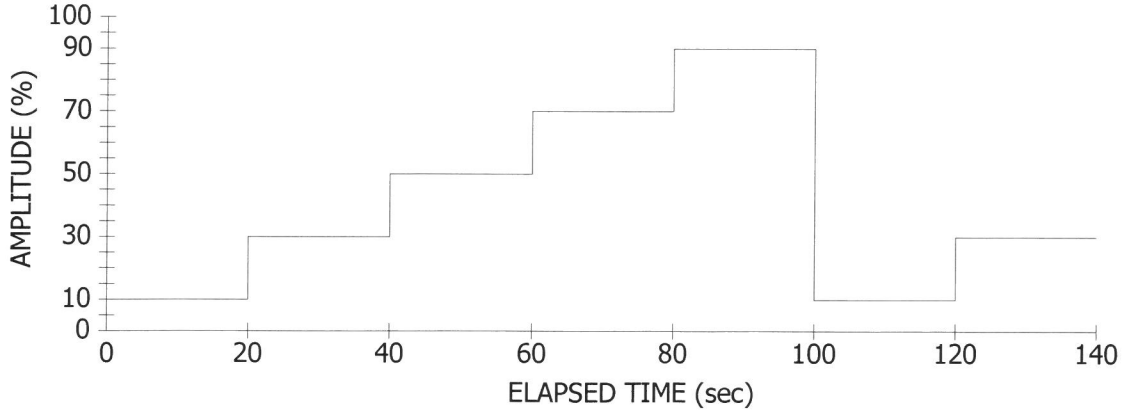


Figure 1. Algorithm for 4- to 20 mA Analog Channel Accuracy Test

4.1.1 Manual Analog Accuracy Test

The waveform shown in Figure 1 is generated by an algorithm running in the TSAP. The resulting image controls the signal level of an AO channel, and that signal is connected back to an AI channel of the same remote. As a minimum, manual execution of this test will be conducted during the prequalification and post qualification phases. The purpose of the initial execution of the test is twofold:

- This data will serve to eliminate any inaccuracy introduced by the configuration of the test circuitry.
- The initial test will establish the baseline characteristics for comparison with system performance throughout the qualification tests.

1. Reference the I/O signal lines from the terminal for 3,AI,5, and use a multimeter to measure the voltage being produced by the AO channel and signal conversion circuit. _____

2. Start the analog accuracy test via the MCRT. Open the Equation Editor program, and locate the ANO block controlling 3,AO,1 (3,BL,56). Display the block edit window. _____

3. Use a multimeter to measure the output signal produced by 3,AO,1. Record the block count value and the resulting voltage level in attachment 7.2.1. If the output signal exhibits any deviation, record a minimum of three values. _____

4. Repeat step 3 for ANO values of 30%, 50%, 70%, and 90%. _____

5. Reconnect the signal wire to the terminal for 3,AI,5. _____

6. Display the block edit window for the AIC block associated with 3,AI,5 (3,BL,51). Record the block value and the count value for the signal being received level in attachment 7.2.1. If the values exhibit any deviation, record a minimum of three values for both parameters. _____

7. Repeat step 6 for ANO values of 30%, 50%, 70%, and 90%. _____

8. Verify that the AIC block exhibits the step wave pattern. _____

9. Record the best AI value for each step level in attachment 7.2.1. Take a minimum of three readings for each step level to establish repeatability. _____

10. Use the MCRT to stop the automated accuracy test. _____

4.1.2 Manual RTD AI Accuracy Test

RTD cards provide a separate constant current output for each RTD channel and include input contacts for three-wire RTD elements. Real RTD elements are connected to 3,AI,17 and 3,AI,18, and the values of these inputs will be logged during qualification testing. During prequalification testing, a Fluke 743B will be used to simulate the operation of an RTD element. The following steps provide the manual test sequence.

1. Connect a Fluke 743B to the terminals for 3,AI,19 as follows:

   Fluke 743B + to 3,6,8:7 terminal
   Fluke 743B – to 3,6,8:8 terminal _____

2. Take measurements for the following five temperature levels:[XXXXX XXXXXXXXXXXXXXXXXXXXX] _____

3. Record the raw count value and the scaled temperature value (3,BL,79) in attachment 7.2.3. Take a minimum of three readings for input level for the channel under test. _____

4. Disconnect the Fluke 743B from the channel under test. _____

4.1.3 Automated Analog Accuracy Test

The test waveform for the 4 to 20 mA AO channels is generated by an algorithm running in the TSAP on command from the MCRT. No special configuration is required prior to running this automated test. The RTD module has two channels configured with RTD elements, and the TC module has two channels configured with T/C input devices. Values for the configured TC and RTD channels will be logged continuously by the HAS.

The automated test sequence will be executed after initial execution of the manual test sequences during prequalification testing, and then it will be repeated at specified points throughout qualification testing.

1. On the EWS work station start the HASLOGGER program. _____

2. Use the MCRT on ERD1192 to start the FPC08 Remote 3 Analog Accuracy test. _____

3. Allow the test to run for a minimum of three complete cycles of the test waveform (5 minutes) or the duration of the qualification test being run. _____

4. Use the MCRT to stop the automated accuracy test. Record the time at which the automated analog accuracy test was run in attachment 7.2.2. _____

4.2 RESPONSE TIME TEST

The TSAP contains algorithms to support direct measurement of response time for analog and for digital logic components. Both test algorithms can be started and stopped from the MCRT workstation, and test points are configured in the SOE logger to support automatic recording of test data.

Execution of the manual response time tests prior to running the specified qualification tests is not necessary unless one of the modules involved with this test had to be replaced due to component failure.

4.2.1 Digital Response Time Measurement

The algorithm for digital response time measuring consists of two parts: a round-robin discrete input/output/input/output program pattern composed of four DI channels and four DO channels and a digital trigger signal. (See Figure 2.) [XXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXX]. In addition, the TSAP also includes a free-running square wave generator that produces a trigger pulse (DO,8 in Figure 2) that controls the image of DI,22. This arrangement provides a mechanism for measuring both the stability of the processing cycles and the response time of the digital processing logic. The resulting response time measurement will include the time required for the following processing steps:

- Input filtering and signal conditioning
- Input processing by the I/O card processor
- Transfer over the internal system ICL to the controller
- Transfer over the internal system ICL to the DO card
- Output processing of the DO processor

The average processing cycle time for the cascaded DI/DO pattern is [XX] of the total period of the free-running square wave produced by the TSAP algorithm (SOE log point 3,DO,12). The digital logic response time is measured directly by the transition of the TEST TRIGGER signal to the TRIP OUTPUT signal (SOE log points 3,DO,8 and 3,DO,25). The following parameters will be recorded as system baseline values following the initial execution of the digital response time test.

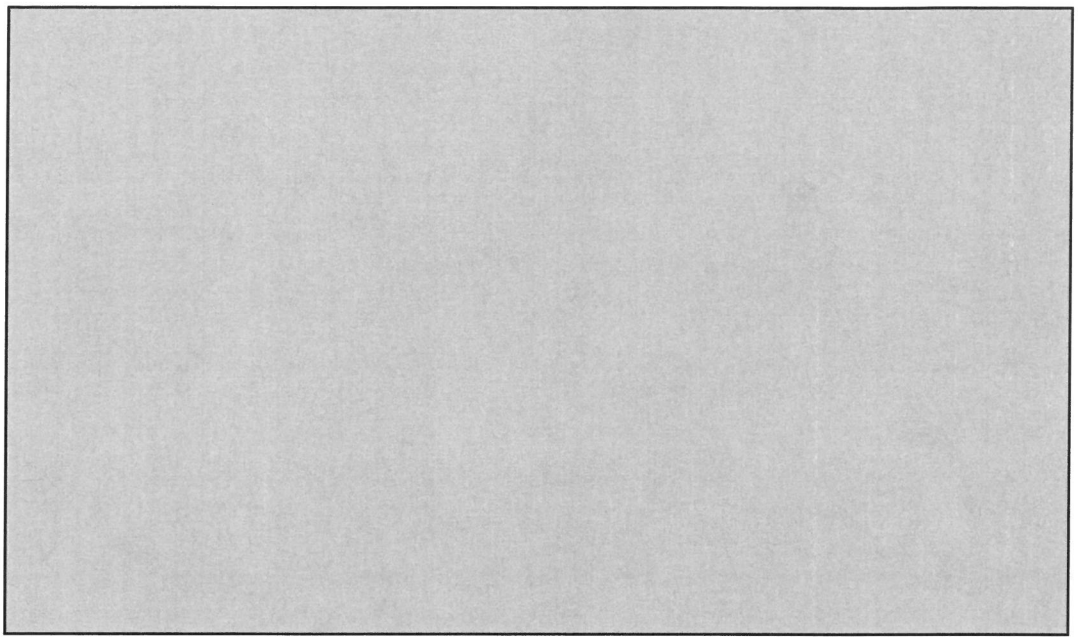


Figure 2. TSAP Algorithm for Digital Response Test

- The amount of time that 3,DO,12 is TRUE.
- The amount of time that 3,DO,12 is FALSE.
- The amount of time from the FALSE-to-TRUE transition of the trigger pulse 3,DO,8 (leading edge) to the FALSE-to-TRUE transition of the trip output 3,DO,25.
- The amount of time from the TRUE-to-FALSE transition of the trigger pulse 3,DO,8 (trailing edge) to the TRUE-to-FALSE transition of the trip output 3,DO,25.

Because the trigger pulse is not synchronized with the operation of the Test Specimen remotes, a range of response times will be observed. This range corresponds to the difference between best case and worst case synchronization of processing cycles. The test algorithm will be logged by the SOE for a minimum of 1 minute, and the resulting data will provide the basis for calculating averaged values for the above intervals.

4.2.2 Analog Response Time Measurement

The TSAP provides a test algorithm (Figure 3) composed of two blocks and a simulated trip memory to support system response time measurements for analog components.
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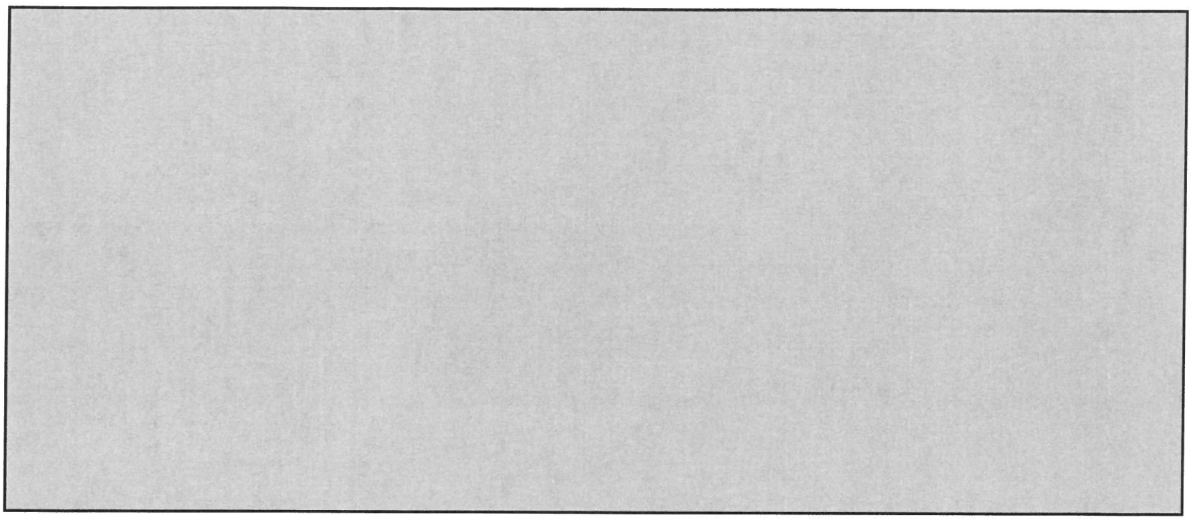


Figure 3. Simplified Algorithm for Analog Response Testing

Because the AO channel is rated for 4- to 20-mA and the AI channel is rated for 0- to 5-v, the test configuration requires signal conversion circuitry. Part of this circuitry converts the 4 to 20 mA signal a 0 to 5 v input for the AI channel. Additional signal conditioning circuit triggers a relay each time the AO channel switches so the transition can be logged on the SOE. During prequalification testing, an oscilloscope will be used to measure and record the transfer delays introduced by the signal conversion circuits, but the response time delay will be logged directly by the SOE. During qualification tests, the SOE logger will record the test data, and the results from the prequalification test will be used to adjust for delays inherent in this test configuration. Analysis of the data recorded during the test will produce values for both the leading edge and training edge response times for analog signals.

4.2.3 Manual Test Sequence

All points of interest for the digital response time test are recorded by the SOE logger, so no manual execution is necessary. The analog trip signal and the digital output are also logged, but the analog signal requires conditioning to permit logging. Consequently, the transfer delay through the conditioning circuit must be measured in order to obtain a more accurate value for the actual ERD1192 FPC08 analog response time.

1. Connect channel 1 of the oscilloscope to TB1-10 (+) and TB1-11 (-) (AO input) of the signal adapter board ECS-TC-SRT #1 for the ERD1192 FPC08. _____ |
2. Connect channel 2 of the oscilloscope to TB1-3 (-) and TB1-8 (+) of the ECS-TC-SRT #1 (SOE input signal). _____ |
3. Use the MCRT to start the Analog Response Time test algorithm. _____
4. Position traces 1 and 2 to display the relation between the AO signal and the SOE input signal. Take a screen capture. _____

5. Use the measure function of the oscilloscope to calculate the delay between the transition of the AO signal and that of the SOE input signal. Record this value in attachment 7.3.1. Take a minimum of three measurements for both the leading edge and the trailing edge transitions. _____

4.2.4 Automated Response Time Test Sequence

The automated response time test will be conducted during the prequalification phase of testing after completion of the manual test, and it will be repeated at specified points during the qualification tests. While the test is running, logic transitions will be recorded automatically by the SOE logger.

1. On the MCRT start the Response Time tests. (Analog and digital response time tests may be run together or individually.) _____
2. While both response time test algorithms are running, SOE log points 1 through 5 show activity. (See Table 1.) _____
3. Allow the test to run for a minimum of 1 minute. _____
4. On the MCRT stop the response time test. _____
5. Verify that the SOE logger generates a report automatically. _____
6. Verify that the SOE report file contains the expected data, and then record the name of the SOE report file in attachment 7.3.2. _____

4.3 DISCRETE INPUT TEST

The discrete input operability test demonstrates the capability of each type of discrete input channel in the Test Specimen to detect a transition in the signal being monitored. In order to accomplish this, the channel under test will be subjected to an input signal whose voltage level is controlled by a manual rheostat (or variable DC power supply). The peak value of the input will be at the rated value for the channel, and the minimum value will be 0 volts. During the test, the set voltage level and the reset voltage level for each DI channel type will be measured. The test will be conducted during the prequalification phase of testing to establish a performance baseline, during the environmental stress test, and then during post qualification testing.

1. Connect 3,DI,24 to a rheostat (or variable DC power supply) to control the magnitude of the input voltage level. _____
2. Select Repeat mode operation of the Memory Editor. Display the status of the DI images beginning with 3,DI,17. (The normal "OFF" state image is 0100_H; the normal "ON" state image is 8100_H.) _____

3. Slowly increase the input voltage level from 0 v up to the point where the image for 3,DI,24 switches from "OFF" to "ON." Record this voltage level in attachment 7.4. _____

4. Slowly increase the input signal from turn-on threshold up to a maximum of 24 v. Verify that the DI image remains stable throughout this range. _____

5. Slowly reduce the input voltage level until the DI image switches from "ON" to "OFF." Record this voltage level in attachment 7.4. _____

6. Decrease the input from the reset voltage level to 0. Verify that the DI channel remains "OFF." _____

7. Cycle the input voltage a total of three times. Record the "ON" and "OFF" voltage levels for each cycle. Verify that no other DI channel is affected by the input signal being manipulated. _____

4.4 DISCRETE OUTPUT TEST

The discrete output operability test demonstrates the capability of each type of discrete output channel in the test specimen to operate under load. In order to accomplish this, one pair of the Digital Response Time Test cascaded points will be used to supply a DO channel under load. The test will be conducted during the prequalification phase of testing to establish a performance baseline as well as each time the automated response time test is run.

1. The ERD1192 FPC08 has only one type of DO channel. 3,DO,31 is connected to the SOE point 2,DI,399. _____

2. Use the MCRT to start the Digital Response Time test. _____

3. Verify that the DO channel cycles "TRUE" and "FALSE". _____

4. Verify that the status LED for this channel accurately indicates channel status. Record this data in attachment 7.5. _____

4.5 COMMUNICATION TEST

1. Ensure the HAS Server is running. _____

2. Ensure the "Auto SOE Trigger" is set. _____

3. Ensure the SOE Logger program is running and it is set to "Auto Start". _____

4. Open the Telnet program in a DOS window on the EWS and Open a connection to the primary HFC-FPC08 controller. (I.E. – "open 192.168.1.249") _____

5. After opening the connection, login using "root" as the login name and password. _____

6. To access the IO diagnostic information, use the following command. "./ioDiag 0 0 11" This command will read all 11 IO cards diagnostic information. _____

7. Table 3 defines the detailed contents of the IO diagnostic structure.

8. Save a screen capture of this information to an external file and record date and time screen capture was taken. _____

9. Since the HFC-FPC08 does not currently support C-Link error counters 10 and 11, this test will prove the C-link communication quality using the equation execution counter 10. _____

10. Open the DDB trend program and configure the program to read 3,BL,10 and set the Min value to 0, the Max value to 7000 and the Frequency to 1 second. _____

11. Let the DDB trend program run for about 70 seconds then save a screen capture of this information to an external file. Record date and time screen capture was taken. _____

12. On the MCRT graphic, actuate the START buttons for the Accuracy, Response Time Test, and Burst of Events test to provide a level of background operation. _____

13. Allow the test to run for a minimum of 5 minutes or the duration of the qualification test being run. _____

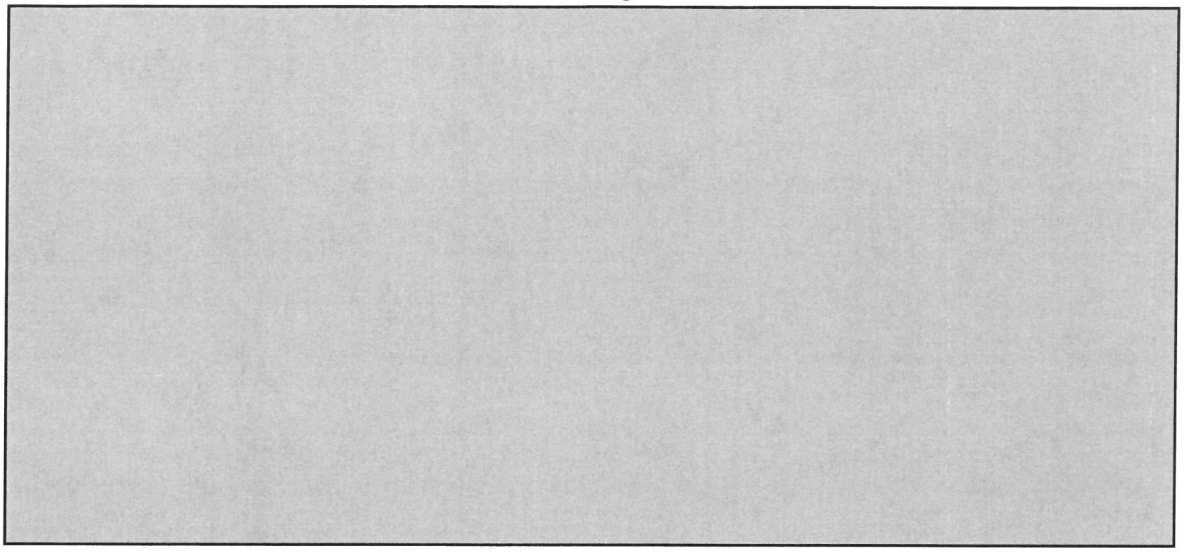
14. Save another screen capture of the DDB Trend program window to an external file. Record date and time screen capture was taken. _____

15. Execute the ./ioDiag 0 0 11 command in the Telnet DOS window again and save a screen capture of this information to the external file. Record date and time screen capture was taken. _____

16. On the MCRT graphic, actuate the STOP buttons for the Accuracy, Response Time Test, and Burst of Events test. _____

17. Record the SOE log files and HAS files using attachment 7.6 _____

Table 3. ICL Diagnostic Structures



Validation of Communication Operability Test: _____
Test Engineer/Date

4.6 TIMER TEST

The timer test will be based on logic completely contained within the TSAP. This logic consists of four pulse timers configured to control two separate free-running square waveforms. The output from one set of timers will be "ON" for 1 second and "OFF" for 1 second; the waveform from the second set will be "ON" for 5 seconds and "OFF" for 1 second. The two waveforms will drive separate DO channels that are routed to separate SOE input channels (Table 1) to permit automatic recording of the signal transitions.

1. Use the MCRT to start the timer test function. Additional tests may run concurrently. _____

2. Allow the test to run for a minimum of 1 minute or the duration of the qualification test being run. _____

3. Use the MCRT to stop the timer test function. _____

4. Generate the SOE report file for the data points being logged. _____

5. Open the SOE report file and verify that the expected data is present. Record the name of the SOE report file in attachment 7.7. _____

4.7 FAILURE TO COMPLETE SCAN

The Failure to Complete Scan test introduces a loop in the TSAP to cause the Failure to Scan condition to occur. This test will be executed during prequalification testing, at the end of the high temperature phase, the end of low temperature phase of the environmental test, and after the SSE seismic test.

1. As a minimum, ensure that the automated accuracy, timer, and BOE tests are running in the background. _____
2. Activate Failure to Complete Scan for Remote 3. _____
3. Verify that the digital output led tied to the failure to scan flag (3,DO,32) lights after a brief delay. This is your visual indication that the fail to scan flag was activated. _____
4. Verify that all automated functions activated in step *1* continue operating normally. _____
5. Use the MCRT to stop all automated tests, including failure to complete scan. _____
6. Verify that the SOE logger generates the report file automatically. _____
7. Verify that the report file contains the expected data. _____
8. Record the date and time that the test was run and the name of the SOE report file in attachment 7.8. _____

4.8 FAILOVER TEST

When running as a redundant pair, the FPC08 monitors the other card's status. If the secondary detects the primary has stopped updating its mailbox, the secondary will become primary. This test measures the amount of time the secondary takes to detect primary failure and assume primacy.

1. Connect a (minimum) three channel oscilloscope to the ICL link, and the Primary indication LED of the secondary (R113 – side closest to front edge of PCB). Configure the scope to trigger when the LED turns on. _____
2. Ensure the HAS Server is running. _____
3. Ensure the "Auto SOE Trigger" is set. _____
4. Ensure the SOE Logger program is running and it is set to "Auto Start". _____
5. On the MCRT graphic, actuate the START buttons for the Accuracy, Response Time Test, and Burst of Events test to provide a level of background operation. _____
6. Open the Telnet program in a DOS window on the EWS and Open a connection to the primary HFC-FPC08 controller. (I.E. – "open 192.168.1.249") _____

7. After opening the connection, login using "root" as the login name and password. _____

8. Ensure both FPC08's are running redundantly. _____

9. To force failover, execute the following command on the primary controller. "./command 0". _____

10. Use the scope to measure the amount of time between when the ICL commands from the primary stopped, and the ICL commands from the new primary starts. _____

11. On the MCRT graphic, actuate the STOP buttons for the Accuracy, Response Time Test, and Burst of Events test. _____

12. Record the SOE log files and HAS files using attachment 7.9 _____

Validation of Failover Test: _____
Test Engineer/Date

4.9 LOSS OF POWER TEST

During this test, power is removed from the Test Specimen for a minimum period of 30 seconds, and then the power is restored. The purpose of the test is to demonstrate that all I/O channels transition to power-off states when power is removed and then hold these states following restoration of power until system initialization has been completed. This test will disrupt the operation of the ERD1192 FPC08 for up to 5 minutes. It will be executed at specified points during the environmental test but not in conjunction with other tests.

1. Use the memory editor or database editor to set static points 3,AO,5 (BL,57) and 3,AO,6 (BL,87) to mid range (50). Set PID Loop 1 and Loop 2 to mid range. _____

2. Start all of the automated tests **except** Failure to Complete Scan and BOE. _____

3. Verify that the automated tests are running. _____

4. Disable the ac power source for the Test Specimen power supplies for a minimum of 30 seconds. Record the time when power was removed in attachment 7.10. _____

5. While power is out, the C-Link and all automated tests will also be disabled. _____

6. Restore ac power to the Test Specimen power supplies. Record the time when power was restored in attachment 7.10. _____

7. Verify the following:

   - Test Specimen output channels remain disabled while initialization tests are in progress.
   - After initialization tests are completed, the automated tests that had been running will remain disabled. _____

8. Verify that the SOE logger automatically generates a report. _____

9. Open the SOE report and verify that it contains the expected data. _____

10. Record the name of the SOE report file in attachment 7.10. _____

4.10 POWER INTERRUPT TEST

During this test, the ac power feed to the power supplies will be interrupted for a period of 40 ms to simulate a power transient or transfer to an emergency backup power source. The purpose of the test is to demonstrate that the Test Specimen power supplies can hold their output voltage above the minimum level necessary to sustain reliable controller operation. Because this test could disrupt any automated test that may be running, the power interruption test will be executed only during pre test and at specified points during the qualification tests.

1. Connect the power source to the Test Specimen power supplies through a timer relay. All power supplies shall be connected to the same power source. _____

2. Configure the timer relay to interrupt power flow to the Test Specimen for a fixed interval of 40 ms. _____

3. Set power to the Test Specimen on. Record the time when power was applied to the Test Specimen in attachment 7.11. _____

4. Use the CQ4 editor to set static points (3,BL,57 and 3,BL,87) to mid range. _____

5. Enable the automated accuracy, response time, and timer operability tests to provide a minimum set of dynamic operations. _____

6. Initiate the 40-ms interruption in source power. _____

7. Allow the system to continue logging data for a minimum of 30 seconds after the power interruption. _____

8. Disable the automated tests. Record the time when the test was ended in attachment 7.11. _____

9. Verify that the SOE logger generates a report file automatically. _____

10. Open the SOE report file and verify that it contains the expected data. _____

11. Record the name of the SOE report file in attachment 7.11. _____

4.11 POWER QUALITY TOLERANCE TEST

The cabinet is designed to contain redundant modules for 24-VDC logic power as well as redundant Auxiliary modules for 24-vdc excitation power. This test will verify the capability of these power supplies to continue providing adequate operating power to the control system under varying conditions of source power quality.

This test is not a regular part of the Operability tests. It shall be conducted at the end of the high temperature phase of the environmental stress test, and after completion of the SSE seismic test. Execution of this test is not required before, during, or after any of the other qualification tests.

1. Power down the Test Specimen, and connect a variable power source to the power feed for the power supply chassis. All of the power supplies shall be connected to the same power source. _____

2. Set the power source to supply [XXXXXXX], and enable operation of the Test Specimen. _____

3. Set static points (3,BL,57 and 3,BL,87) to mid range. Set PID Loop 1 (3,BL,43) and Loop 2 (3,BL,44) to mid range. _____

4. Enable the automated accuracy, response time, and timer operability tests to provide a minimum set of dynamic operations. _____

5. Record the starting time for this test in attachment 7.12. _____

6. If the cabinet is accessible, use a multimeter to measure the output voltage level produced by each power supply with power source set for [XXXXXXXXX]. Record these values in attachment 7.12. _____

7. Verify low voltage operation as follows:

   a. Reduce the output from the variable power source to [XXXXXXX].
   b. Record the output voltage levels produced by both logic and excitation voltage power supplies. (Rated output voltage for each power supply is 24 vdc.)
   c. Record the output voltage levels produced by the each power supply in attachment 7.12. _____

8. Verify power supply operation with power source at high frequency limit:

   a. Increase the variable output source frequency to [XXX].
   b. Record the output voltage levels produced by each module in attachment 7.12. _____

9. Verify system response to undervoltage trip condition:

   a. Reduce the output from the variable power source to [XXXXX].
   b. Verify that undervoltage protection forces all power supplies off.
   c. Verify that Test Specimen LEDs are all off. _____

10. Verify power supply recovery:

    a. Set the variable power source to [XXXXX].
    b. Record the output voltage levels produced by each power supplies. _____

11. Restore the original setup conditions as described in step ***3***. _____

12. Verify high voltage operation as follows:

    a. Increase the output from the variable power source to [XXXXX XXX].
    b. Record the output voltage levels produced by each power supply in attachment 7.12. _____

13. Verify power supply operation with power source at high frequency limit:

    a. Increase the variable output source frequency to [XXX].
    b. Record the output voltage levels produced by each power supply in attachment 7.12. _____

14. Verify system response to overvoltage trip condition:

    a. Increase the output from the variable power source until the power supplies trip or the output is [XXXX]. _____

15. Restore the normal operation configuration:

    a. Set the variable power source to [XXXXX].
    b. Record the output voltage levels produced by each power supply in attachment 7.12. _____

16. Record time of test completion in attachment 7.12. _____

17. Verify that the SOE logger automatically generates an SOE report, and verify that it contains the expected data. _____

18. Record the name of the SOE report file in attachment 7.12. _____

19. Power down the test specimen, and disconnect the variable power supply from the power feed. _____

5.0 ACCEPTANCE CRITERIA

Acceptable results for the operability tests are defined by EPRI TR-107330, which has been used for guidance in developing the qualification test program. The following list presents the design standards for each parameter as published in the HFC specifications for the HFC-6000 product line as well as deviation limits for performance during the qualification tests. A preliminary set of results obtained during the prequalification phase of testing will establish baseline performance characteristics for the ERD1192 FPC08 Test Specimen. Subsequent performance of the operability tests during the qualification tests will disclose any deterioration from the baseline performance caused by the stress conditions being imposed.

Accuracy Tests Acceptance Criteria

0- to 5-v AI Channels

HFC Design Specification	15 bit AI image Accuracy within ±0.1% of span over the entire range
During qualification test	Accuracy within ±0.35% of span over the entire range

4- to 20-mA AO Channels

HFC Design Specification	12 bit AO image Accuracy within ±0.1% of span over the entire range
During qualification test	Accuracy within ±0.32% of span over the entire range

100-ohm RTD Input Channels

HFC Design Specification	15 bit AI image 0° to 200° C design operating range Accuracy within ±0.1% of range over the entire range
During qualification test	Accuracy within ±2° C (3.6° F) over the entire range

Type E Thermocouple Input Channels

HFC Design Specification	15 bit AI image -30° to 500° C design operating range Accuracy within ±0.1% of range over the entire range
During qualification test	Accuracy within ±3° C (5.4° F) over the entire range

Response Time

Digital Circuit	Average response time shall be 100 ms or better from activation of the trip condition to output of the trip DO signal
Analog Circuit	Average response time shall be 300 ms or better from activation of the trip condition to output of the trip DO signal
During Qualification Test	The maximum response time shall not increase by more than 10% from measured baseline value.

Discrete Input Operability

DI set voltage level	Guaranteed DI "ON" level is 20 v at 25° C
DI dropout voltage	Guaranteed DI "OFF" level is 12 to 15 v at 25° C
Maximum input voltage	Maximum input voltage for ERD1192 is 24 v at 25° C

Discrete Output Operability

Solid State DO channels	Switches 24-vdc excitation power

Communication Operability

C-Link	Overall system operation continues in the presence of stress conditions.
ICL	I/O scanning continues in the presence of stress conditions.

Timer Test

Timer accuracy shall vary by no more than ±1% when averaged over 10 cycles.

Fail To Complete Scan

Remote under test triggers reset within 1 sec after activation of fault.

Normal operation resumes automatically following reset of controller.

Failover Test

(EPRI TR 107330 4.3.4.7 A & D)

a. Transfer to secondary controller shall trigger an alarm
b. Secondary controller shall continue to run in normal operation mode
c. The transfer shall ensure the following:
    i. Shall occur with 200 ms (2 main processor scan cycle times)

ii. Shall not cause I/O modules to have more than an 0.5% transient shift in the final output signal
iii. Shall not cause a change in the I/O signal that persists for more than 5 ms for DC signals or 1 cycle for AC signals
iv. Shall not cause pulse input modules to lose signal
v. Shall not cause digital I/O to change state for more than 2 ms, and analog I/O signals to change by more than 5%

Loss of Power Test

All output channels return to the deenergized state on loss of power.

On restoration of power, controller operation resumes automatically.

Power Interruption Test

No ERD1192 controller becomes reset.

No static DO channel changes state.

No static AO channels changes its output signal by more than 5%.

Logged parameters of all automated tests remain within tolerance.

Power Quality Tolerance Test

While source power is between 90 to 150 vac and 57 to 63 Hz, the output voltage level produced by the power supply remains within ±1% of its setpoint level.

No power supply dropout alarm occurs while source power is within the above specified range.

Undervoltage protection trips the power supply output.

Overvoltage protection trips the power supply output.

Power supply recovers from overvoltage and undervoltage conditions automatically.

6.0 QA RECORDS

All data generated by execution of the tests covered by this procedure will become QA records. Manually recorded test data shall be entered on the appended Test Data Record sheets. Results for the automated portions of the Operability tests will be recorded in a set of SOE report files and an HAS database. The electronic records shall be transferred to CDs to provide a permanent, unchangeable record of test results for subsequent analysis. Both the manually generated test data records and the CDs produced during the qualification phase of testing will be retained as a permanent record of test execution.

7.0 ATTACHMENTS

The following Test Data Record forms are attached to this document. These forms shall be filled out by the test engineer while the tests are being executed.

Attachment 7.1	Test Equipment Log
Attachment 7.2	Analog Channel Accuracy Test Records
Attachment 7.2.1	HFC-AO8FD to HFC-AI16RD Manual Test Record
Attachment 7.2.2	HFC-AO8FD to HFC-AI16RD Automated Test Record
Attachment 7.2.3	Manual RTD Accuracy Test Record
Attachment 7.3	Response Time Test
Attachment 7.3.1	Manual Test Sequence
Attachment 7.3.2	Automated Response Time Test
Attachment 7.4	Discrete Input Test
Attachment 7.5	Discrete Output Test
Attachment 7.6	Communication Test
Attachment 7.7	Timer Test
Attachment 7.8	Failure to Complete Scan Test
Attachment 7.9	Failover Test
Attachment 7.10	Loss of Power Test
Attachment 7.11	Power Interruption Test
Attachment 7.12	Power Quality Tolerance Test

ATTACHMENT 7.1 TEST EQUIPMENT LOG

Test Equipment	Instrument ID	Cal Due Date

Test Engineer _____ Date _____

ATTACHMENT 7.2 ANALOG CHANNEL ACCURACY TEST RECORDS

7.2.1 HFC-AO8FD to HFC-AI16RD Manual Test Record

3,AO,1			3,AI,5	
Set Value	**Count Value**	**Measured AO Signal (V)**	**AI Image (Count Value)**	**AIC Block Value**
10%				
30%				
50%				
70%				
90%				

Test Engineer _____ Date _____

7.2.2 HFC-AO8FD to HFC-AI16RD Automated Test Record

All data for the automated AO-AI accuracy test is logged by the HAS. Record time (hour/minute) and date for each execution of the automated accuracy test.

Start Time	Stop time

7.2.3 Manual RTD Accuracy Test Record

3,AI,19: Count Value:_____ Scaled AIC Value:_____

Input (° C)	Expected Count	3,AI,19	
		Count Value	Scaled AIC Value
[XX]	[XX]		
[XX]	[XX]		
[XX]	[XX]		
[XX]	[XX]		
[XX]	[XX]		

Test Engineer _____ Date _____

ATTACHMENT 7.3 RESPONSE TIME TEST

7.3.1 Manual Test Sequence

3,AO,2 to SOE leading edge delay

_____ _____ _____

3,AO,2 to SOE trailing edge delay

_____ _____ _____

SOE Report File Name(s):

7.3.2 Automated Response Time Test

SOE Report File Name(s):

ATTACHMENT 7.4 DISCRETE INPUT TEST

Card Type Under Test	_____		
Input Channel Rating	_____		
ON Voltage Threshold (3 cycles minimum)	_____	_____	_____
Maximum Input Voltage (3 cycles minimum)	_____	_____	_____
OFF Voltage (3 cycles minimum)	_____	_____	_____

ATTACHMENT 7.5 DISCRETE OUTPUT TEST

Card Type Under Test	_____
DO Status "ON" verified	_____
DO Status "OFF" verified	_____

Test Engineer _____ Date _____

ATTACHMENT 7.6 COMMUNICATION TEST

(Append Memory Editor screen captures)

	C-Link	ICL
Time at Start of Test		
Time at end of Test		
Duration		
Append Screen Captures of ICL Diagnostic Structure and DDB Trend Program		

ATTACHMENT 7.7 TIMER TEST

Record SOE Report file name(s) for test execution.

ATTACHMENT 7.8 FAILURE TO COMPLETE SCAN TEST

Date and time of test execution: _____

Record SOE Report file name(s) for test execution.

ATTACHMENT 7.9 FAILOVER TEST

Date and time of test execution: _____

Record SOE Report file name(s) for test execution.

Test Engineer _____ Date _____

ATTACHMENT 7.10 POWER LOSS TEST

Date and Time of Test Execution: Start _____ Finish _____

Power Off Time_____ Power Restored Time _____

Record SOE Report file name.

ATTACHMENT 7.11 POWER INTERRUPTION TEST

Date and Time of Test Execution: Start _____ Finish _____

Name of SOE Report file:

ATTACHMENT 7.12 POWER QUALITY TOLERANCE TEST

Date and Time of Test Execution: Start _____ Finish _____

Record Power supply Output Voltage Levels:

Power Feed	Power Module B		Power Module A	
	24-vdc logic	24 vdc Aux	24 vdc logic	24 vdc Aux
[XXXXXX]				
[XXXXXX]				
[XXXXXX]				
[XXXXXX]				
[XXXXXX]				
[XXXXXX]				
[XXXXXX]				
[XXXXXX]				
[XXXXXX]				

Name of SOE Report file:

Test Engineer _____ Date _____