HF Controls

HFC-SBC04A SLC Control System

TSAP Validation Test Procedure

TP901-203-03 Rev B

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Revision History

Date	Revision	Author	Changes
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1.0 PURPOSE AND SCOPE

The SLC has been assembled from components of the HFC-6000 product line configured as a triple-redundant safety control system (Test Specimen). A synthetic application program (TSAP) has been configured for the single loop controller (SLC) to support functional and qualification stress testing of the system. This procedure covers validation of the program code and functional operation of this TSAP as follows:

- **Source Code Verification** – The source code file generated by the HFC One-Step utility will be examined line by line and compared with the graphic representation of logic diagrams 705005-09.

- **Operability Test Support** - This test will verify functional operation of the TSAP code designed to support Operability testing and verify that the test design will produce the expected data. The automated Operability tests will be started/stopped from the MCRT through a redundant HFC-SBC06 controller system which interacts the algorithms executed within the TSAP. Execution of this test will exclude extensive recording or logging of test results, which will be accomplished during execution of the Operability tests.

- **Prudency Test Support** - This test will verify functional operation of the TSAP code designed to support the automated Prudency tests. The automated Prudency tests will be started/stopped from the MCRT through a redundant HFC-SBC06 controller system which interacts the algorithms executed within the TSAP. Execution of this test will exclude extensive recording or logging of test results, which will be accomplished during execution of the Prudency tests.

Functional testing of the TSAP code will be conducted after TP901-203-02, HFC-SBC04A SLC Integration Test Plan is completed.

2.0 REFERENCES

2.1 INDUSTRY STANDARDS

This test procedure constitutes part of the prequalification testing for the HFC-6000 control system. These tests have been developed to document the baseline performance of the control system Test Specimen prior to the start of qualification stress testing.

EPRI TR 107330 Generic Requirements Specification for Qualifying a Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants, 1996

2.2 HFC DOCUMENTATION

705005-04	TMR DMR Logic Diagram, Rev. A
705005-09	HFC-SBC04A SLC Logic Diagram, Rev. A
RS901-201-03	HFC-SBC04A TSAP Requirements Specification, Rev. A
DS901-201-03	HFC-SBC04A TSAP Design Specification, Rev. A
TP901-300-00	ERD921/ERD111 Master Test Plan, Rev. B
TP901-203-02	HFC-SBC04A SLC Integration Test Plan, Rev. A
TP901-203-04	HFC-SBC04A SLC Operability Test, Rev. A
TP901-203-05	HFC-SBC04A SLC Prudency Test, Rev. A
VV901-303-02	HFC-SBC04A SLC Master Configuration List, Rev. A

2.3 HFC INTERNAL STANDARDS AND PROCEDURES

QPP 5.1	Review and Approval of Documents
QPP 11.1	Test Control
WI-ENG-003	Configuration Management
WI-ENG-815	Red Line Procedure

2.4 SPECIAL TERMS, ABBREVIATIONS, AND ACRONYMS

DMT	Dead Man Timer
EWS	Engineering Workstation (HFC PC software utility)
LED	Light Emitting Diode
MCRT	Microsoft/Windows CRT (HFC PC software utility)
PC	Personal Computer
Test Specimen	A specific combination of hardware and software components to be subjected to specified test conditions
TSAP	Test Specimen Application Program

3.0 PREREQUISITES

The following paragraphs define the equipment, setup, and configuration requirements for conducting the TSAP Validation Tests.

3.1 EQUIPMENT REQUIRED

This test will be conducted after successful completion of TP901-203-02 during the acceptance phase of pre-qualification testing. Minimum equipment requirements for running this test are as follows:

- Fully integrated HFC-SBC04A SLC Test Specimen as validated by TP901-203-02

Record all test equipment used during this test in attachment 7.1.

3.2 ENVIRONMENTAL CONDITIONS

The TSAP validation test will be conducted in the HFC testing facility without any external stress applied. The normal ambient environment in this facility is as follows:

Temperature	50° to 104° F
Relative Humidity	7% to 90% noncondensing

3.3 TEST PERSONNEL

All of the testing functions covered by this document will be conducted by a qualified HFC test engineer or technician at the HFC facility.

3.4 PRECAUTIONS

WARNING

Certain I/O circuits are energized with high voltages and may carry potentially hazardous current loads. Exercise caution whenever working around exposed terminals or circuitry.

3.5 RED-LINE POLICY

The HFC policy for entering red-line corrections into a test procedure shall be done in accordance with WI-ENG-815, "Red-Line Procedure".

3.6 TEST SETUP REQUIREMENTS

1. Verify that the copy of the TSAP Validation Test Procedure in hand is a controlled copy of the latest revision according to Document Control records.

2. Verify that equipment setup is complete.

3. Verify that execution of TP901-203-02 is complete.

4. Verify the following:

   a. Verify that the Test Specimen and the redundant HFC-SBC06 remote supporting the test specimen are all powered up.

   b. At the PC workstation, start the Equation Editor program.

   c. Open the equation file for loop 0291 (main Test Specimen controller). Verify that the Equation Editor opens the local file without indicating any discrepancy. (This indicates that the file in the controller matches the equation file in the PC memory.) Verify that the compilation date and CRC matches the record in the MCL.

Test setup is complete: _____

Test Engineer/Date

4.0 TEST SEQUENCE

The overall validation test will be accomplished in two stages: source code verification and system functional test. During source code verification, the content of the source code text files will be validated against the logic diagrams from which they were created. During the functional test, the application code installed in the controller will be validated for the support for the Operability tests, Prudency Burst of Events tests, and simulated MFT logic. Use attachment 7.2 to record the summary of the validations.

4.1 SOURCE CODE VERIFICATION

1. Obtain a printout of the latest revision of the TSAP logic diagrams, 705005-09. _____
2. To ensure that the source code listings are identical to those in the Test specimen, print a copy of the TSAP equations source code files from the EWS workstation. _____
3. Verify the following items for each logic symbol represented on the TSAP logic diagram:
   - The point type and point number in the source code printout matches the logic symbol in the diagram.
   - The symbol in the logic diagram matches the function (AND, OR, NOT timer, memory, block, etc.) represented in the source code.
   - Each timer preset represented on the logic matches the preset statement in the source code.
   - Each timeon/timeoff/pulse timer on the logic diagram is correctly translated into program source code. _____
4. Trace each connection line represented on the logic diagram from source node to input node, and verify that the link is accurately represented in the source code. _____
5. Verify that each configured output channel (DO/AO) is controlled by a corresponding statement in the source code. _____

_____

Test Engineer / Date

4.2 TSAP OPERABILITY/PRUDENCY SUPPORT LOGIC

The TSAP includes program code for supporting the Operability and Prudency tests. The support logic for the Operability and Prudency tests has been designed to establish a performance baseline during the pre-qualification phase of tests for comparison with performance during and after qualification testing. The following tests are intended to verify that both the test algorithms operate as intended.

4.2.1 Accuracy Tests

The algorithm for the accuracy test will permit automated testing of 4- to 20-mA AO and 4- to 20- mA AI channels of the Test Specimen. The TSAP includes a test algorithm that generates a dynamic test waveform. This algorithm drives one AO channel, and the

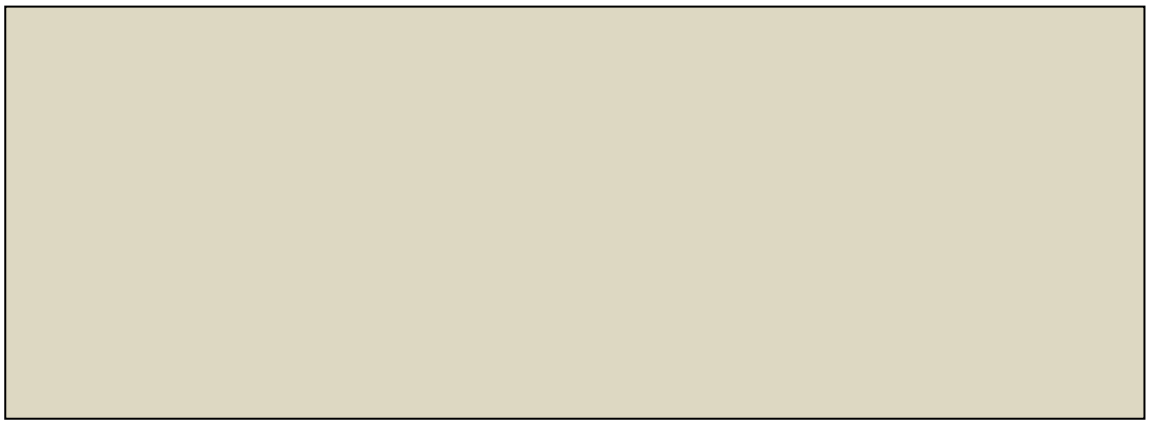

Figure 1 Test Waveform for Automated Analog Channel Accuracy Test

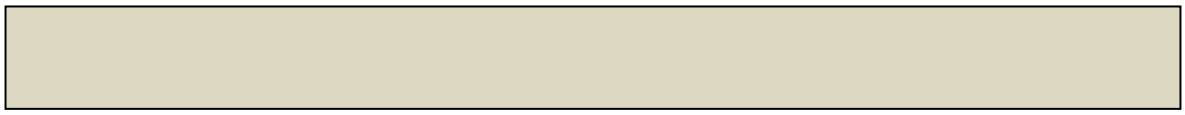

Table 1 TSAP Points for Analog Accuracy Testing

1. Verify that the Test Cabinet, Test Specimen, and PC workstation are all powered up and operating. _____

2. Verify that card edge LEDs for all circuit cards indicate normal completion of initialization. Verify that the card edge LEDs for each I/O card show the following:
   - TX and RX LEDs flash to indicate activity.
   - STATUS LED remains on constantly. _____

3. Open an Equation Editor program to display the TSAP equation files for loop 0291. _____

4. Locate equation containing BL,23 (the ANO block controlling AO,23). _____

5. Use the MCRT to start the Analog Accuracy test. _____

6. Turn equation editor monitoring mode on to display block values, and verify that the test signal generators in the TSAP begin generating the test waveform (Figure 1). _____

7. Locate equation containing BL,41 (the AIC block processing the input from AI,23). Verify that the block exhibits each step of the accuracy algorithm. _____

8. Use the MCRT to stop the Accuracy test. _____

9. Verify that the test waveform stops dynamic operation and returns to its minimum value. (Once the algorithm has started, it will continue running until the current cycle is completed.) _____

_____

Test Engineer / Date

4.2.2 Response Time Test Algorithms

The TSAP includes separate trigger and response algorithms to support measurement of the response time for analog and for digital processing functions. Operation of both test algorithms can be started and stopped from the MCRT workstation.

4.2.2.1 Digital Response Time Algorithm Verification

The TSAP provides a round-robin discrete input/output/input/output program pattern composed of four DI channels and four DO channels. The first DI channel controls the first DO channel, and that signal is physically connected to the next DI channel in sequence. The last DO signal is then fed back to the first DI channel, and a NAND gate in the link from the first DI to the first DO permits the test engineer to start or stop the test from the MCRT workstation. The TSAP also produces a free-running square wave to drive a test trigger signal (DO,1) that controls the input to DI,1, which serves as the input for a simulated trip memory. Table 2 lists significant I/O points associated with this test, and Figure 2 illustrates the arrangement of the logic algorithm.

Table 2 TSAP Digital Points for Digital Response Time Testing

Figure 2 General Arrangement of Digital Response Time Logic

1. Use the MCRT to start the digital response time test. _____
2. Display the TSAP equation using Equation Editor for loop 0291. _____
3. Display DO,1. Verify that this output is a free-running square wave that is TRUE for 8 second and FALSE for 8 second. _____
4. Display the logic for DO,2. Verify that DO,2 is driven by DI,1 and also exhibits a free running square wave signal. _____
5. Use the MCRT to stop the digital response time test. _____
6. Verify that all signals associated with this test become static. _____

4.2.2.2 Analog Response Time Algorithm Verification

The TSAP provides a test algorithm composed of a test trigger generator and analog blocks to process a simulated input signal. The analog processing logic is composed of an AIC block to receive the input signal and a DHA block to detect a high alarm point. (The DHA block is configured with an alarm setpoint of 50% and a deadband of 0.01.) The trigger signal consists of a free-running square wave with a period of 16 seconds (8 seconds true, 8 seconds false). This signal drives DO,10, which is routed to a signal conversion circuit. This signal conversion circuit produces an analog output signal that switches between 0 and 5 v as well as outputs for the SOE logger. The analog signal is routed to AI, 22 of the same remote, and the image of this input serves as the process value for the DHA block. The analog system response time is then measured from the point where the AI signal crosses the 50% level to the leading edge of the DO response. Figure 3 illustrates the TSAP logic and the test waveform, and Table 3 lists the specific I/O points used to support this test.

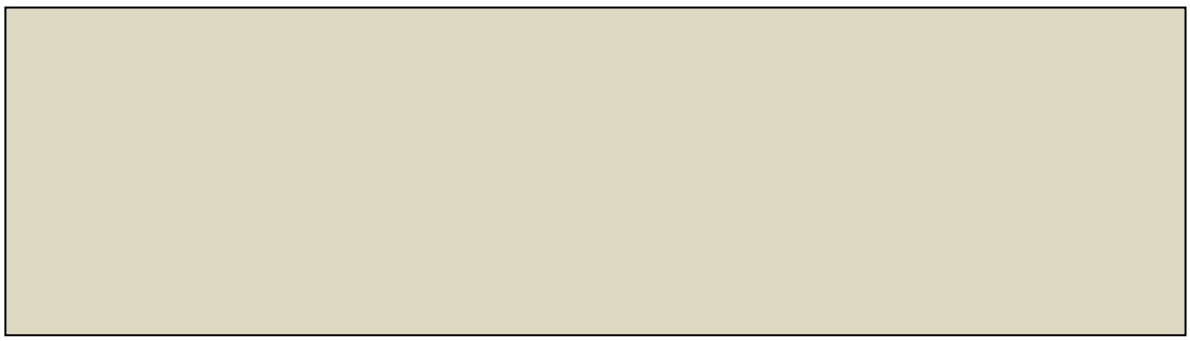

Table 3 TSAP Support for Analog Response Time Testing

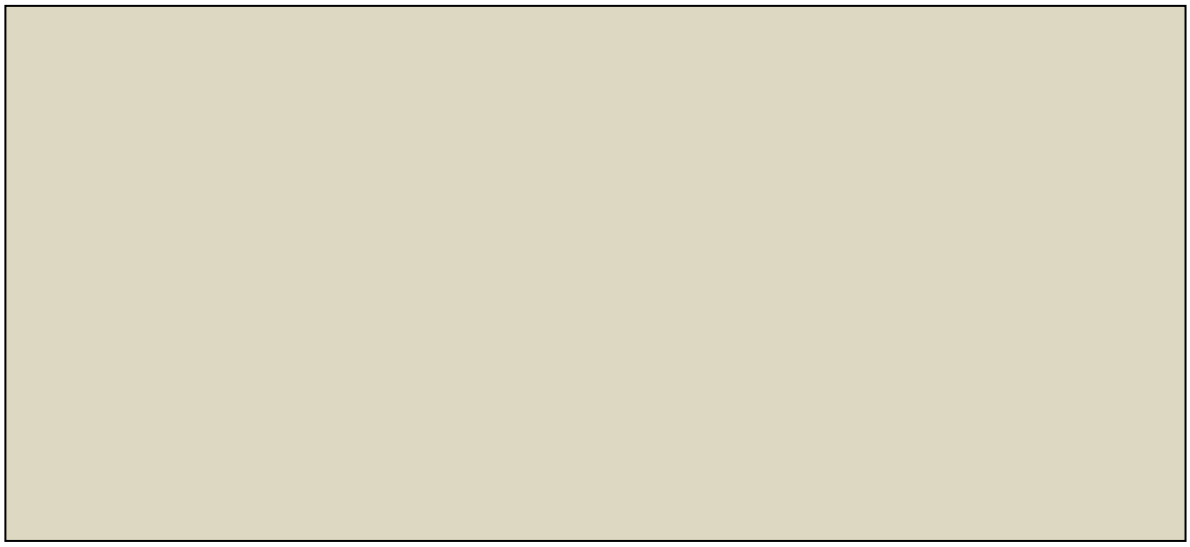

Figure 3 General Arrangement for Analog Response Time Algorithm

1. Use the MCRT to start the response time test. _____
2. Display the TSAP equation file for loop 0291 using the equation editor. _____
3. Display the control logic for DO,2. Verify that the algorithm switches with a period of 8 sec. _____
4. Display the logic controlling AO,22. Verify that both AI,22 and AO,22 show activity. _____
5. Display CO,112. Verify that CO,112 shows activity. _____
6. Use the MCRT to stop the response time test. _____
7. Verify that all I/O points associated with this test become static when the test is not running. _____

4.2.3 Timer Test Algorithm Verification

The timer test uses four pulse timers configured to control two separate free-running square waveforms (Figure 4). The output from one set of timers will be TRUE for 1 second and FALSE for 1 second; the waveform from the second set will be TRUE for 5 seconds and FALSE for 1 second. The two output signals will drive separate DO chan The spec

Figure 4. General Arrangement of Timer Test Algorithm

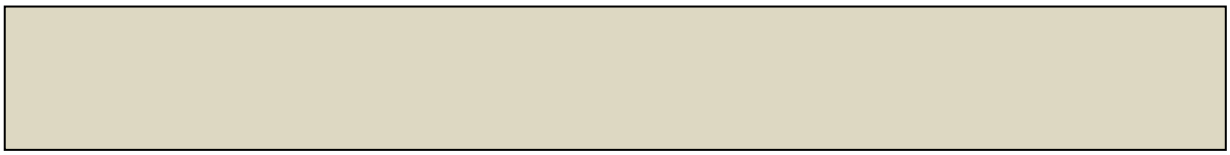

Table 4. TSAP Support for Timer Testing

1. Use the MCRT to start the timer tests.

2. Display the equation file for loop 0291 using the Equation Editor. _____ _____

3. Display the logic controlling DO,2. Verify that a cascaded 1-sec and 5-sec timer are controlling dynamic operation of the output point. _____

4. Display the logic controlling DO,3. Verify that cascaded 1-sec pulse timers are controlling dynamic operation of the output point. _____

5. Use the MCRT to stop the timer test. _____

6. Verify that both DO,2 and DO,3 become static. _____

_____

Test Engineer / Date

4.2.4 Failure to Complete Scan Test

The TSAP includes an algorithm that introduces an infinite loop into the application code on command from the MCRT. When an application cannot completed its one cycle of execution, i.e. "fails to complete scan", the firmware sets FL, 785 to TRUE. The logic is to detect when FL, 785 becomes TRUE when an infinite loop is being executed.

1. Use the MCRT to start the Failure to Complete Scan test. _____
2. Verify using the equation editor that the logic in the loop has FL, 785 turned ON. _____
3. Use the MCRT to stop the Failure to Complete Scan test. _____

_____

Test Engineer / Date

4.2.5 Miscellaneous Functions

4.2.5.1 Loop Counter

The TSAP includes a loop counter CO, 119 that increments once during each processing cycle of the equation interpreter throughout normal operation. The value of this counter can be logged in order to obtain a direct measure for the number of equation processing cycles completed between any two points in time.

1. Verify the display for CO, 119 on MCRT is incrementing. _____
2. Record the counter value and the time when the value was read from the time of day display on the memory editor.

   Counter Value _____ Time of Day _____ _____

3. Wait a few minutes and then repeat step 2.

   Counter Value _____ Time of Day _____ _____

_____

Test Engineer / Date

4.2.5.2 Analog PID Loop

The TSAP includes a simulated closed loop composed of one PID controller. Table 5 lists the analog points in the simulated analog loop. The stability of the circuit will be monitored during the qualification stress tests to determine if the stress conditions cause the circuit to become unstable.

Table 5. Analog PID Loop Point Assignments

1. Configure the MCRT to allow updating CO,102. _____
2. Verify CO,102 is 0 at the start of the test. _____
3. Values of the counter associated with AO,24 & AI,24 should be about 0. _____
4. Update CO,102 to 30. _____
5. Verify that AO,24 and AI,24 change their values to 25 after ~3 minutes. _____
6. Update CO,102 back to 0. _____
7. Verify AO,24 and AI,24 are back to around 0 after about 1 minute. _____

_____

Test Engineer / Date

4.2.6 Burst of Events Test Validation

The Burst of Events test is intended to activate a significant number of I/O points simultaneously. In the case of the SLC, the limitation of available output points limits the number of total channels that can be included. Table 6 lists all channels included in the test. In both cases, the TSAP contains an algorithm that drives the output channels, and each output signal is connected back to an input channel.

Table 6. Burst of Events Test Validation

1. Use the MCRT to start the BOE test. _____
2. Display the equation file for loop 0291 using equation editor. _____
3. Display the logic controlling AO, 21. Verify that the ANO block value switches between 10% and 90%. _____
4. Display the AIC block processing AI, 21. Verify that the block value switches between 10% and 90%. _____
5. Use the MCRT to stop the BOE Test. _____
6. Verify that all signal transitions associated with the BOE test halt. _____

_____

Test Engineer / Date

5.0 ACCEPTANCE CRITERIA

Table 7 lists the acceptance criteria for validating the TSAP.

Table 7. TSAP Acceptance Criteria

Source Code Verification	
	All point types and point designations match those in the logic diagrams.
	All logic connections traced from point to point match the connections shown in the logic diagrams.
	All timer preset values match those shown in the logic diagrams.
	All internal block structures contain the values shown in the logic diagrams.
Accuracy Tests	
	MCRT interface enables test engineer to start/stop the automated accuracy test.
	All AI and AO channels listed for the automated accuracy test exhibit the test waveform while the test is enabled.
Digital Response Time Algorithm	
	MCRT interface enables test engineer to start/stop automated response time test algorithms.
	While response time test is running, the TSAP algorithm produces a free running square wave composed of 1 DI channels and 1 DO channels.
	Algorithm produces a free-running square wave as trigger signal of a period of 16 seconds.
	Trigger signal controls input to simulated trip memory. Trip memory controls simulated trip output.
Analog Response Time Algorithm	
	MCRT interface enables test engineer to start/stop automated response time test algorithms.
	The algorithm produces a free running 0.5 Hz analog trigger signal that switches between 45% and 55% of span.
	Trigger signal controls input to DHA block.
	DHA block controls simulated trip output.
Operability Timer Test	
	MCRT interface enables test engineer to start/stop automated time test algorithms.
	TSAP provides four timers that produce two free-running square waves while the test is enabled.
	Test waveforms enable direct measurement of periods for 1-second and 5-second timers .
Failure to Complete Scan Test	
	MCRT interface provides ability to enable/disable test.
	When enabled, the test trigger signal forces the application program to stall.
	Verify that associated FL, 785 turns on.

TSAP Special Functions	
	CO,119 increments once each Equation Interpreter processing cycle. This running count provides a precise indication of processing speed during any fixed period of time.
	TSAP provides a closed PID loop that is tuned to provide a static output value.
Burst of Events Test	
	MCRT interface enables test engineer to start/stop automated Burst of Events test algorithms.
	BOE algorithm controls two digital waveforms consisting of square waves of a period of 16 seconds that are 180 degrees out of phase.
	BOE controls 1 analog input and 1 output signals each of switches between 10% and 90% of span, and the signal remains at each level for 10 seconds.
	When test is disabled, the BOE points remain static.

6.0 QA RECORDS

All data generated during performance of this test will be recorded manually to verify that the automated Operability and Prudency test algorithms will run and produce data that can be used for performance analysis. Both the test procedure with completed signoffs and the attached test data records will be regarded as permanent QA records and will be filed in accordance with QPP 17.1 “Quality Records”.

7.0 ATTACHEMENTS

Attachment 7.1 – Test Equipment Log

Attachment 7.2 – Test Summary Record

Attachment 7.1 – Test Equipment Log

Test Equipment	Instrument ID	Calibration Due Date

Test Engineer _____ **Date** _____

Attachment 7.2 – Test Summary Record

	Pass
Source Code Verification	_____
Accuracy Test Support	_____
Response Test Support	_____
Digital Response Time Algorithm Test Support	_____
Analog Response Time Algorithm Test Support	_____
Timer Test Algorithm Test Support	_____
Failure to Complete Scan Test Support	_____
Loop Counter Test Support	_____
Analog PID Loop Test Support	_____
Burst of Events Test Support	_____

_____

Test Engineer / Date