HF Controls

HF CONTROLS

HFC-6000 Control System

DMR – Control System Qualification Project

Operability Test Procedure Rev A
TP901-201-04

Effective Date: _____

Prepared By: _____

Reviewed By: _____

Approved By: _____

Revision History

Date	Revision	Author	Changes
3/3/10	A0	J Taylor	Draft
4/5/10	A	J. Taylor	Initial Release

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1.0 PURPOSE AND SCOPE

Selected components of the HFC-6000 product line will be configured as a redundant controller (Test Specimen). This controller includes a triple-redundant configuration of I/O modules. The complete Test Specimen (controllers, I/O modules, and cabinet assembly) will be subjected to a battery of tests intended to qualify it as a controller configuration to be used in safety-related applications. The following set of Operability tests are based on test requirements defined by EPRI TR-107330.

- **Accuracy Test** - This test verifies that analog I/O modules in the test specimen meet the accuracy and linearity requirements. (EPRI TR-107330 references: 4.3.2.1, 4.3.3.1, 5.3.A, 6.2.2.B.2, B.6, and B.8)

- **Response Time Test** – This test will measure the response time for discrete and analog inputs from the leading edge of the input to the leading edge of the resulting output (EPRI TR-107330 references: 4.2.1.A, 5.3.B, 6.2.2.B5).

- **Discrete Operability Tests** – Operability tests for the DI and DO channels were conducted as part of TMR testing. Because the same types of I/O modules are being used with the DMR, these tests will not be repeated.

- **Communication Operability Test** – This test will verify reliable data transfer over all serial communication links associated by the Test Specimen (EPRI TR-107330 references: 5.3.E).

- **Timer Test** – This test will verify the accuracy of the timer function accessible to the TSAP (EPRI TR-107330 references: 5.3.G, 6.2.2.B.3).

- **Failure To Complete Scan Detection** – This test will verify the capability of the system software to detect failure to complete at least one execution of the application program during each context switch interval (EPRI TR-107330 references: 4.2.3.7.A, 4.4.6.3.C, 5.3.H).

- **Failover Operability Test** – This test demonstrates operability of the failover hardware for redundant controllers (EPRI TR-107330 references: 4.3.4.7, 5.3.H).

- **Loss of Power Test** – This test will demonstrate correct response of all I/O channels to loss of source power followed by reapplication of power to the system (EPRI TR-107330 references: 5.3.J).

- **Power Interruption Test** – This test will demonstrate the capability of the power modules to sustain system operation during a temporary (transient) power interruption (EPRI TR-107330 references: 4.6.1.1.F, 5.3.K).

- **Power Quality Tolerance Test** – This test will demonstrate the capability of the Test Specimen to continue normal operation over a range of source power voltages and frequencies (EPRI TR-107330 References: 4.2.3.7.B, 4.6.1, 6.4.3, 6.4.4.F).

These tests are designed to exercise control system functions to provide a basis for evaluating its performance. The complete set of tests will be run prior to the actual qualification tests to establish a performance baseline for the system. This performance baseline will then be used as the basis for evaluating system performance during and/or following each of the qualification tests to be accomplished.

2.0 REFERENCES

2.1 INDUSTRY STANDARDS

EPRI TR-107330	Generic Requirements Specification for Qualifying a Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants (December 1996)

2.2 RELATED PLANS AND PROCEDURES

TP901-201-02	Integration Test Plan, Rev A
TP901-201-03	DMR TSAP Validation Test Plan, Rev A
VV901-300-01	Master Test Plan, Rev B
VV901-301-02	DMR Master Configuration List, Rev A
TP901-201-02	Integration Test Plan, Rev A

2.3 SUPPORT DOCUMENTATION

UG004-000-01	EWS User's Guide, Rev E
UG004-000-16	MCRT User's Guide, Rev B
UG004-000-03	HAS User's Guide, Rev E

2.4 HFC INTERNAL STANDARDS AND PROCEDURES

Implementation of HFC test programs is based on the current version of the following internal procedures:

QPP 5.1	Review and Approval of Quality Documents, Rev G
QPP 5.2	Preparation of Procedures, Rev M
QPP 11.1	Test Control, Rev H
WI-ENG-003	Configuration Management, Ref E
WI-ENG-205	Develop Software/Firmware Test Procedure, Rev B
WI-ENG-815	Red Line Procedure, Rev C

2.5 SPECIAL TERMS, ABBREVIATIONS, AND ACRONYMS

C-Link	Communication Link
BOE	Burst of Events
DPM	Dual-Ported Memory
HAS	Historical Archiving System
HPAT	HFC Plant Automated Tester
ICL	Intercommunication Link
M&TE	Measuring and Test Equipment
RH	Relative Humidity
SOE	Sequence of Events
Test Specimen	A specific combination of hardware and software components to be subjected to specified test conditions
TSAP	Test System Application Program

3.0 PREREQUISITES

The following paragraphs provide detailed instructions for setup and performance of each Operability test. Operability tests may be run individually or concurrently with other tests. To the maximum extent possible, the individual Operability tests will be automated so that a test engineer can start/stop the selected tests while a qualification test is in progress. However, certain operability tests will either disrupt operation of the Test Specimen as a whole or will require direct access to the Test Specimen hardware. Such tests will not be automated or run concurrently with other test.

3.1 EQUIPMENT REQUIRED

A detailed listing of hardware and software components of the Test Specimen are provided in RS901-200-01, Master Test Plan. Detailed requirements for component assembly and interconnection are provided by the engineering drawing package. The equipment listed below will be required during performance of this test. Test personnel shall verify that all test and measuring equipment are capable of producing the level of accuracy required by the specific test being performed and that the calibration for the M&TE to be used is current.

- PC workstation with EWS and MCRT software installed
- SOE Utility of the HPAT
- Extender card for HFC-6000 controller and I/O PCBs
- Fluke 187 Multimeter or equivalent
- Relay/timer or equivalent
- Variable ac power source capable of producing an output signal having the following range: 60 to 300 vac, 40 to 65 Hz.

- Tektronix TDS3034 Oscilloscope or equivalent (two input channels minimum)

Record all test equipment used during execution of this test in attachment 7.1, Test Equipment Log.

3.2 ENVIRONMENTAL CONDITIONS

This test will be conducted under various environmental conditions. During prequalification testing, the test will be conducted under normal operating conditions for the Test Specimen, as indicated below. During the qualification tests, required environmental conditions are stipulated within the procedures governing those tests.

Temperature	Ambient
Relative Humidity	Ambient

3.3 TEST PERSONNEL

The set of Operability tests will be conducted at the in-house test facility of HFC following completion of the TSAP Validation Test and at vendor facilities during qualification testing. All of the testing and monitoring functions will be conducted by one or more qualified HFC test engineers/technicians both at the HFC facility and at vendor facilities during qualification testing.

3.4 PRECAUTIONS

WARNING

Certain I/O circuits are energized with high voltages and may carry potentially hazardous current loads. Exercise caution whenever working around exposed terminals or circuitry.

3.5 RED-LINE POLICY

The HFC policy for entering red-line corrections into a test procedure are presented in WI-ENG-815, “Red Line” Procedure. Such entries may be used to correct errors of content and procedural sequence in test documents or in engineering drawings to prevent disruption of a test in progress.

3.6 TEST SETUP REQUIREMENTS

3.6.1 Test Specimen Setup

1. Verify that the copy of the Operability Test Procedure test in hand is a controlled copy of the latest revision according to Document Control records.

2. Verify that all integration testing has been completed successfully.

3. Verify that the TP901-201-03, DMR TSAP Validation Test, has been completed successfully.

Validation that test setup is complete: _____
Name/Date

3.6.2 SOE Point Configuration

An SOE logger will be used to monitor high speed (up to ± 1 ms resolution) logic transitions of selected DO and AO channels during operation of the Operability tests. Table 1 lists SOE point assignments for both Operability and Prudency test points. The following procedure describes the sequence of steps necessary to configure the SOE logger prior to running the Operability tests for the first time or following reassembly of the Test Specimen in a vendor's test facility.

1. Use the SOE Logger facility of the EWS to configure the SOE as follows:

   - Trigger point to activate report generation when any automated test runs
   - Pre-time cutoff of 90 seconds and post-time cutoff of 30 seconds
   - Default SOE logger directory

2. Select the Build option to verify that the SOE remote detects all of the SOE cards configured in the HPAT I/O chassis.

3. Select the Manual Start option.

4. Verify that the SOE subsystem runs an SOE scan to all configured SOE cards.

5. Select the Auto Start option to enable automatic report generation.

6. Verify that the output points listed in Table 1 are physically wired to the indicated input points of the HPAT. Each of these SOE points must be configured for isolated operation.

SOE setup is complete: _____
Name/Date

Table 1. Points Configured for SOE Logging

3.6.3 HAS Configuration

The HFC HAS software utility will be used for logging the value of analog signals as well as digital signals that do not require a time resolution of less than 1 second. Table 2 lists the combination of points selected for HAS logging. (Table 2 includes log points for both Operability and Prudency BOE tests.) The HAS log points shall be configured and verified during the first execution of the Operability and Prudency tests.

1. Enter the HAS log points specified in Table 2.

2. For analog points, set the deadband parameter to 0.005 to ensure that the logged data will validate an accuracy parameter of ±0.1%.

3. Save the spreadsheet file and exit.

Table 2. Points Configured for HAS Logging

HAS setup is complete: _____
Name/Date

4.0 OPERABILITY TEST PROCEDURE

Each of the Operability tests provides a separate evaluation for a specific aspect of the Test Specimen performance and operation. No fixed sequence of execution is assumed or implied by the order of specific tests in this document.

4.1 ACCURACY TESTS

The TSAP contains a stair-step analog algorithm (Figure 1) to support automated testing of analog I/O channels. This wave form drives one AO point of the DMR, and the resulting analog output signal is fed back into an AI point of the DMR. All AO channels are rated for 4- to 20 mA, but the AI channels are rated for 0- to 5-v. Hardware on the

terminal cards inside the test cabinet provides the necessary signal conversion. The test

Figure 1. Algorithm for 4- to 20 mA Analog Channel Accuracy Test

This procedure includes both manual and automated test sequences. The complete accuracy test will be conducted during both pre-test and post-test phases. Only the automated test sequences will be executed during the qualification tests. Table 2 lists all I/O channels configured to support automated accuracy testing and indicates which signal images will be logged. Repetition of a manual accuracy test prior to the start of a qualification test will not be necessary unless one of the AI or AO modules must be replaced.

4.1.1 Manual Analog Accuracy Test

The waveform shown in Figure 1 is generated by an algorithm running in the TSAP. The resulting image controls the signal level of an AO channel, and that signal is connected back to an AI channel. As a minimum, manual execution of this test will be conducted during the prequalification and post qualification phases. The purpose of the initial execution of the test is twofold:

- This data will serve to eliminate any inaccuracy introduced by the configuration of the test circuitry.
- The initial test will establish the baseline characteristics for comparison with system performance throughout the qualification tests.

1. Disconnect the I/O signal lines from the terminal for 4,AI,5. _____

2. Connect a multimeter to read the input signal being supplied to 4,AI,5. _____

3. Open the Equation Editor program and display the block edit window for 4,BL,56, the ANO block controlling 4,AO,1. Put the block in Manual mode to permit direct manual control of block value. _____

4. Set the block value to 10%. Record the block count value and the magnitude of the resulting analog signal level in attachment 7.2.1. If this signal exhibits any deviation, record a minimum of three values. _____

5. Repeat step ***4*** for 30%, 50%, 70%, and 90%/. If the output signal exhibits any deviation, record a minimum of three values. _____

6. Reconnect the signal lines for 4,AI,5. _____

7. Display the block edit window for 4,BL,51, the AIC block associated with 4,AI,5. Set 4,BL,56 to 10% and record the value of 4,BL,51 in attachment 7.2.1. _____

8. Record the AI count value and the value of 4,BL,51 in attachment 7.2.1. _____

9. Repeat steps ***7*** and ***8*** for ANO values of 30%, 50%, 70%, and 90%. _____

10. Put 4,BL,56 into Auto mode. _____

11. Use the MCRT to start the automated accuracy test. _____

12. Verify that the AIC block exhibits the step wave pattern. _____

13. Record the best AI value for each step level in attachment 7.2.1. Take a minimum of three readings for each step level to establish repeatability. _____

14. Use the MCRT to stop the automated accuracy test. _____

4.1.2 Automated Analog Accuracy Test

The test waveform for the analog channels I/O is generated by an algorithm running in the TSAP on command from the MCRT. No special configuration is required prior to running the automated test. The automated test sequence will be executed after initial execution of the manual test sequences during prequalification testing, and then it will be repeated at specified points throughout qualification testing.

1. On the EWS workstation start the HAS.Server program. _____

2. Use the MCRT graphic to start the automated analog accuracy test. _____

3. Allow the test to run for a minimum of three complete cycles of the test waveform (5 minutes) or the duration of the qualification test being run. _____

4. Use the MCRT to STOP the automated analog accuracy test. _____

5. Record the time and date when the test was run in attachment 7.2.2. _____

4.2 RESPONSE TIME TEST

The DMR TSAP contains three algorithms to support digital response testing. The test algorithms can be started and stopped from the MCRT workstation, and test points are configured in the SOE logger to support automatic recording of test data.

4.2.1 Digital Response Time Measurement

The algorithm for measuring digital response time consists of two parts: a round-robin discrete input/output/input/output program pattern composed of four DI channels and four DO channels and a digital trigger signal. (See Figure 2.) The first DI channel controls the first DO channel, and that signal is physically connected to the next DI channel in sequence. The last DO signal is then fed back to the first DI channel, and a NAND gate in the link from the first DI to the first DO permits the test engineer to start or stop the test from the MCRT workstation. In addition, the TSAP also includes a free-running square wave generator that produces a trigger pulse (DO,13 in Figure 2) that controls the input to DI,22, and DI,22 controls a simulated trip memory. This arrangement provides a mechanism for measuring both the stability of the processing cycles and the response time of the digital processing logic. The resulting response time measurement will include the time required for the following processing steps:

- Input filtering and signal conditioning
- Input processing by the I/O card processor
- Transfer over the internal system ICL to the controller
- Transfer over the internal system ICL to the DO card
- Output processing of the DO processor

The average processing cycle time for the cascaded DI/DO pattern is 1/8 of the total period of the free-running square wave produced by the TSAP algorithm (SOE log point 4,DO,8). The digital logic response time is measured directly by the transition of DO,13 to the response of DO,9 in Figure 2 (SOE log points 4,DO,13 and 4,DO,9). The following parameters will be used to calculate the digital response time for the DMR:

- The amount of time that 4,DO,8 is TRUE.
- The amount of time that 4,DO,8 is FALSE.
- The amount of time from the FALSE-to-TRUE transition of the trigger pulse 4,DO,13 (leading edge) to the FALSE-to-TRUE transition of the trip output 4,DO,9.
- The amount of time from the TRUE-to-FALSE transition of the trigger pulse 4,DO,13 (trailing edge) to the TRUE-to-FALSE transition of the trip output 4,DO,9.

Because the trigger pulse is not synchronized with the operation of the Test Specimen remotes, a range of response times will be observed. This range corresponds to the

difference between best case and worst case synchronization of processing cycles. The test algorithm will be logged by the SOE for a minimum of 1 minute, and the resulting data will provide the basis for calculating averaged values for the above intervals.

Figure 2. TSAP Algorithm for Digital Response Test

4.2.2 Analog Response Time Measurement

The TSAP provides a test algorithm (Figure 3) composed of two blocks and a simulated trip memory to support system response time measurements for analog components. One block receives an input from an AI channel, and the output of that block provides the input to a DHA (digital high alarm) block. The trigger pulse for the analog response time test is controlled by a free-running square wave that switches between TRUE and FALSE with a period of 16 seconds (8 seconds TRUE, 2 seconds FALSE). This algorithm drives 4,DO,20, and the resulting signal is routed to an external signal converter, which produces one analog output and one digital output. The analog output switches between 0 and 5 v and controls the input to 4,AI,6; the digital output controls an SOE input signal. The remainder of the algorithm controls the response to the AI signal and produces two outputs, 4,AO,2, and 4,DO,10, both of which control inputs to the SOE subsystem.

While the analog response time test is running, the SOE logger will record transitions corresponding to 4,AI,6, 4,AO,2, and 4,DO,10. However, because the signal conversion circuit introduces time delays that cannot be logged, these time delays will be measured during the initial execution of the test to determine the response characteristics of the DMR. During subsequent test runs, only the SOE values will be recorded and retained.

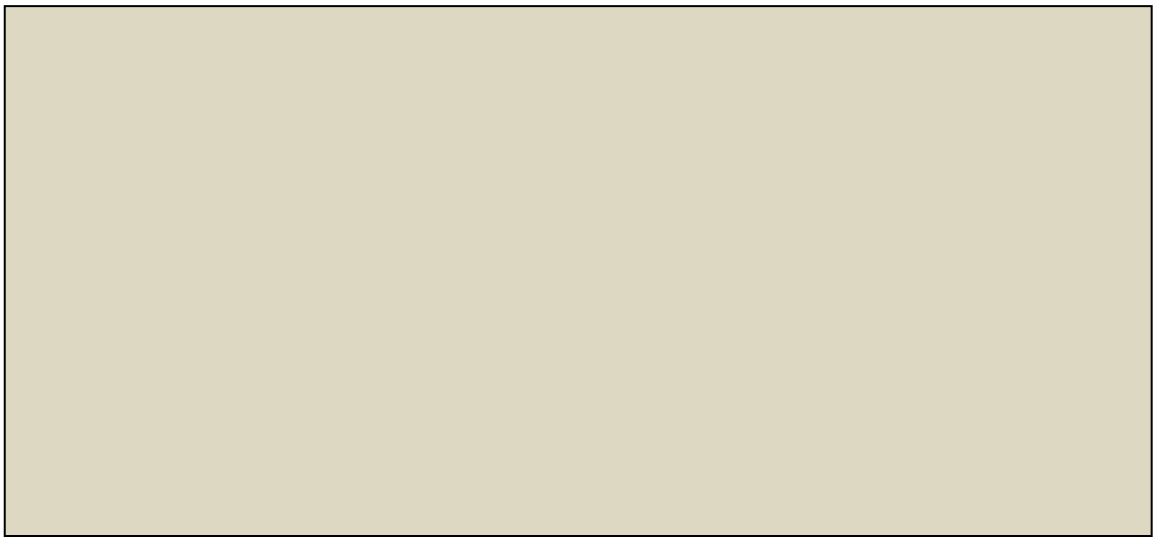

Figure 3. TSAP Algorithm for Analog Response Testing

4.2.3 Manual Test Sequence

This manual execution may be accomplished concurrently with the automated test described in subsection 4.2.4.

1. Identify the response time circuit board connected to the DMR. _____
2. Connect channel 1 of the oscilloscope between R2 (switched +5 vdc) and the negative lead of C2 (signal ground) of the signal conditioning PCB. _____
3. Connect channel 2 of the between the positive and negative terminals for AI,6. _____
4. Use the MCRT to start the Analog Response Time test algorithm. _____
5. Position traces 1 and 2 to display the relation between the switched 5-v trigger signal and the signal at the input of 4,AI,6. _____
6. Measure the transition delay from the point where the trigger signal switches from 0 to 5 v to the point where the signal reaches 2.5v at the input of the AI channel. Record this delay in attachment 7.3. Take a minimum of three measurements of this parameter for both leading and trailing edges of the trigger signal. _____
7. Connect channel 2 of the oscilloscope to HPAT terminal points for 2,DI,427 (SOEE log point for 4,AI,6). _____

8. Measure the delay between the switch point of the 5-v trigger signal and the transition of the input to the SOE channel. Record a minimum of three measurements for both leading and trailing edges in attachment 7.3.2. (The difference between this value and the value measured in step ***5*** represents the transfer delay of the signal conditioning circuit.) _____

9. Use the MCRT to stop the Analog Response Time test. _____

4.2.4 Automated Response Time Test Sequence

The automated response time test will be conducted during the prequalification phase of testing after completion of the manual tests, and it will be repeated at specified points during the qualification tests. While the test is running, logic transitions will be recorded automatically by the SOE logger.

1. On the MCRT start the Response Time tests. (Analog and digital response time tests may be run together or individually.) _____

2. While both response time test algorithms are running, All SOE log points associated with this test show activity. (See Table 1.) _____

3. Allow the test to run for a minimum of 5 minutes. _____

4. On the MCRT stop the response time test. _____

5. Verify that the SOE logger generates a report file automatically. _____

6. Verify that the SOE report file contains data for the test just run, and then record the name of the SOE report file in attachment 7.3.2. _____

4.3 COMMUNICATION TEST

The DMR includes two serial communication links. A redundant Intercommunication Link (ICL) exists from the controller to each of its configured I/O modules. Similarly, a redundant C-Link enables communication between the DMR and external equipment. An HFC-SCG06 gateway remote provides both physical and electrical isolation between the safety C-Link and the common system data highway. Because the communication links and the message structures are not readily accessible during system operation, this test will use link error counters to provide the basis for evaluating the quality of communication on these links. The test will be conducted during the pre-qualification phase of testing and then repeated at specified points during the qualification tests. The overall test method will consist of recording the value of the error counters at the start and end of a test period and interpreting the total accumulated error count as the measure of communication quality. This test typically will run concurrently with other Operability and Prudency tests.

1. Ensure that the HAS.Server program is running to enable logging of the data for communication operability tests (4,CO,10 and 4,CO,11 status). _____

2. Open the Memory Editor program. Select Rem 4, PNC00, Memory Access, and address 053A:6888. This selects the memory location for the ICL diagnostic structure starting with the slot address 00. Table 3 defines the detailed contents of this structure. _____

Table 3. ICL Diagnostic Structures

3. Use the MCRT to start one or more test algorithms to provide a level of background operation. _____

4. Read the ICL diagnostic area using the default starting address to obtain diagnostic data for the first eight configured I/O cards. Print a screen capture and attach it to attachment 7.4. _____

5. Scroll down once to obtain diagnostic data for the second eight I/O cards. Print this screen capture and attach it to attachment 7.4. _____

6. Allow the test to run for a minimum of 5 minutes or the duration of the qualification test being run. _____

7. Repeat steps ***3*** and ***4*** to obtain diagnostic data at the end of the test interval. Attach the screen captures to attachment 7.4. _____

8. Record the time at the start and end of the test period in attachment 7.4. _____

4.4 TIMER TEST

The timer test will be based on logic completely contained within the TSAP of the DMR. This logic consists of four pulse timers configured to control two separate free-running square waveforms. The output from one set of timers will be "ON" for 1 second and "OFF" for 1 second; the waveform from the second set will be "ON" for 5 seconds and "OFF" for 1 second. The two waveforms will drive two DO channels that are routed to

separate SOE input channels (Table 1) to permit automatic recording of the signal transitions.

1. Use the MCRT to start the timer test function. Additional tests may run concurrently. _____
2. Allow the test to run for a minimum of 1 minute or the duration of the qualification test being run. _____
3. Use the MCRT to stop the timer test function. _____
4. Generate the SOE report file for the data points being logged. _____
5. Open the SOE report file and verify that the expected data is present. Record the name of the SOE report file in attachment 7.5. _____

4.5 FAILURE TO COMPLETE SCAN

The Failure to Complete Scan test introduces an infinite loop in the TSAP to force failure of the primary controller. Failure of the primary will force failover to the secondary and trigger an alarm. Following failover, logic in the TSAP will prevent the remaining controller from including the infinite loop in the TSAP code. This test will be executed during prequalification testing, at the end of the high temperature phase of the environmental test, and after the SSE seismic test.

Execution of this test will force the primary controller into an offline state. Do not run the test at a time when it will compromise the results of other tests being run concurrently.

1. As a minimum, ensure that the automated accuracy, timer, and BOE tests are running in the background. _____
2. Activate Failure to Complete Scan for Rem 4. _____
3. Verify that Rem 4 primary fails after a brief delay and fails over to the secondary. The failed controller will remain disabled until it can be reset. _____
4. Verify that all automated functions activated in step ***1*** continue operating normally under control of the former secondary controller. _____
5. Use the MCRT to stop all automated tests, including failure to complete scan. _____
6. Verify that the SOE logger generates the report file automatically. _____
7. Verify that the report file contains the expected data. _____

8. Record the date and time that the test was run and the name of the SOE report file in attachment 7.6. _____

9. If the controller is accessible, actuate the reset switch for the failed controller. Verify that the controller resumes normal operation as secondary after completing its initialization sequence. _____

10. If the controller is not accessible, use the loss of power test to force a power cycle to reset the remote. _____

4.6 FAILOVER TEST

The DMR includes redundant controllers and redundant power supplies. The redundant controllers share a Dual-Ported Memory (DPM) assembly that provides the mechanism for transferring system status from the primary to the secondary controller. The power supplies normally are both powered on and provide operating power to separate power traces on the back plane. Diode auctioneering on each card in the chassis provide the mechanism for maintaining isolation between the power supplies. For this reason, only the controllers will be subjected to failover testing.

1. Enable automatic accuracy, response time, and timer tests to provide a minimum set of dynamic operations. _____

2. Set the simulated PID Loop 1 and Loop 2 to mid range. Set static points 4,AO,5 and 4,AO,6 to mid range. _____

3. Record the starting time for this test in attachment 7.7 in order to facilitate recover data for the following points from the HAS:

   - 4,CO,50 – equation loop counter value
   - 4,AO,3 – PID loop 1 value
   - 4,AO,4 – PID loop 2 value
   - 4,AO,5 – static AO value 1
   - 4,AO,6 – static AO value 2
   - 4,AO,7 – analog BOE signal

   _____

4. Slot 2 of rack 7 contains the DPM card. The P2 connector enables access to the following signals used for failover control:

   - P13-A39 SANE_A/
   - P13-C39 SANE_B/
   - P13-B39 PRI_A/
   - P13-B40 PRI_B/

   _____

5. Mount the HFC-DPM06 PCB on an extender card to enable access to enable access to I/O signals at the backplane connector. _____

6. Identify the controller that is operating as primary (A or B). _____

7. Connect the probe for channel 1 of the oscilloscope to the SANE signal for that controller; connect the probe for channel 2 to the PRI signal for the secondary. _____

8. Set the power/reset switch (SW1) on the primary controller toward the card to remove power from that card. _____

9. When the switch cycles power off, the card immediately disables its SANE status, and this transition will force transfer of PRI status to the secondary. Use the oscilloscope to record the delay between the low-to-high transition of the SANE/ signal (channel 1) and the high-to-low transition of the PRI/ signal (channel 2). Take and record a minimum of three measurements for this parameter in attachment 7.8. _____

10. Return the HFC-DPM06 PCB to the chassis and then restore power to the controller. _____

11. Monitor the affect of failover on analog control loops as follows:

    a. Mount the HFC-AO16FD PCB in slot 6 of rack 6 on an extender card.

    b. Connect the probe for channel 1 of the oscilloscope to P2-A3 and P2-C3 (signal lines for 4,AO,2).

    c. Use the MCRT to start the analog response time test.

    d. While the AO channel is transitioning from low to high or from high to low, press the red pushbutton switch on the front edge of the DPM card to initiate failover.

    e. Use the oscilloscope to capture the response characteristics of the AO signal.

    f. Use the measure function of the MCRT to calculate the duration of any disruption observed. Record this value in attachment 7.7.

    g. Take a minimum of three measurements of the transition delay, if any.

    h. Return the HFC-AO8FD PCB to the rack. _____

12. Monitor the affect of failover on digital control function as follows: _____

    a. Connect channel 1 of the oscilloscope to HPAT terminals for 2,DI,416 (logging 4,DO,8).

    b. Enable digital response time test for DMR.

    c. Press the red pushbutton switch on the front edge of the DPM card to initiate failover.

    d. Use the oscilloscope to capture the complete period of 4,DO,8 while failover is in progress. Measure and record this period in attachment 7.7.

    e. Measure the period of the square wave signal during normal operation, and record that value in attachment 7.7.

    f. Take a minimum of three measurements for both normal operation and operation during failover.

13. Record the name of the SOE report file created and the time when the test was completed in attachement 7.7. _____

4.7 POWER SUPPLY TESTS

A series of three tests will be conducted to establish operability characteristics of the power supplies being used with the test specimen. A single set of power supplies is being used by the TMR, DMR and SLC, and the detailed procedure for executing these tests is contained in TP901-202-04. Pretest setup for the DMR consists of starting the automated accuracy and response time tests to provide a level of background activity.

5.0 ACCEPTANCE CRITERIA

Acceptable results for the operability tests are defined by EPRI TR-107330, which has been used for guidance in developing the qualification test program. The following list presents the design standards for each parameter as published in the HFC specifications for the HFC-6000 product line as well as deviation limits for performance during the qualification tests. A preliminary set of results obtained during the prequalification phase of testing will establish baseline performance characteristics for the DMR Test Specimen, and these results will be used to update the acceptance criteria. Subsequent performance of the operability tests during the qualification tests will disclose any deterioration from the baseline performance caused by the stress conditions being imposed.

Accuracy Tests Acceptance Criteria

0- to 5-v AI Channels

HFC Design Specification	15 bit AI image Accuracy within ±0.1% of span over the entire range
During qualification test	Accuracy within ±0.35% of span over the entire range

4- to 20-mA AO Channels

HFC Design Specification	12 bit AO image Accuracy within ±0.1% of span over the entire range
During qualification test	Accuracy within ±0.35% of span over the entire range

Response Time

Digital Circuit	Average response time shall be 100 ms or better from activation of the trip condition to output of the trip DO signal
Analog Circuit	Average response time shall be 300 ms or better from activation of the trip condition to output of the trip DO signal
During Qualification Test	The maximum response time shall not increase by more than 10% from measured baseline value.

Communication Operability

C-Link	Overall system operation continues in the presence of noise interference.
ICL	I/O scanning continues in the presence of noise interference.

Timer Test	Timer accuracy shall vary by no more than ±1% when averaged over 10 cycles.
Fail To Complete Scan	Remote under test triggers reset within 1 sec after activation of fault. Normal operation resumes automatically following reset of controller.

Failover Operability	Transfer to secondary processor shall trigger an alarm. Analog control circuits shall not exhibit more than a 0.5% transient shift in the final output signal. In digital control circuits, the secondary processor shall not sense an invalid change in DI signals or produce an invalid transition in DO signals that persists for more than 5 ms. The period from failure of the primary to the start of dynamic control by the secondary shall be measured during prequalification testing and used as the performance baseline for subsequent qualification testing.
Power Supply Tests	Refer to TP901-202-04.

6.0 QA RECORDS

All data generated by execution of the tests covered by this procedure will become QA records. Test data generated during manual execution of the Operability tests will be recorded on the appended Test Data Record sheets. Results for the automated portions of the Operability tests will be recorded in a set of SOE and HAS report files. These files shall be transferred to CDs to provide a permanent, unchangeable record of test results for subsequent analysis. Both the manually generated test data records and the CDs produced during the qualification phase of testing will be filed in accordance with the Project Quality Plan.

7.0 ATTACHEMENTS

Test Data Record forms are attached to this document. These forms shall be filled out by the test engineer while the tests are being executed.

Attachment 7.1 Test Equipment Log

Test Equipment	Instrument ID	Cal Due Date

Test Engineer _____ Date _____

Attachment 1.2 Analog Channel Accuracy Test Records

7.2.1 HFC-AO8FD to HFC-AI16RD Manual Test Record

ANO Block in Manual Mode

1,AO,1 Under Manual Control			1,AI,5	
Set Value	**Count Value**	**Measured AO Signal (v)**	**AI Image (Count Value)**	**AIC Block Value (%)**
10%				
30%				
50%				
70%				
90%				

ANO Block in Auto Mode with Accuracy Test Running

1,AO,1	1,AI,5	
Algorithm Value	**AI Image (Count Value)**	**AIC Block Value (%)**
10%		
30%		
50%		
70%		
90%		

Test Engineer _____ Date _____

7.2.2 HFC-AO8FD to HFC-AI16RD Automated Test Record

All data for the automated AO-AI accuracy test is logged by the HAS. Record time (hour/minute) and date for each execution of the automated accuracy test.

Start Time	Stop time

Attachment 7.3 Response Time Test

0% to 50% AI transfer delay: _____ _____ _____

100% to 49% AI transfer delay: _____ _____ _____

Digital trigger signal to 4,AI,6 SOE input

Leading edge transfer delay: _____ _____ _____

Trailing edge transfer delay: _____ _____ _____

SOE Report File Name(s):

Test Engineer _____ Date _____

Attachment 7.4 Communication Test

(Append Memory Editor screen captures)

	C-Link	ICL
Time at Start of Test		
Time at end of Test		
Duration		
Append Screen Captures		

Attachment 7.5 Timer Test

Record SOE Report file name(s) for automated test execution.

Attachment 7.6 Failure to Complete Scan Test

Date and time of test execution: _____

Record SOE Report file name(s) for test execution.

Test Engineer _____ Date _____

Attachment 7.7 Failover Test

Date and Time of Test Execution: Start _____Finish _____

Failover transfer delay from trailing edge of SANE_A/ to leading edge of PRI_B/

_____ _____ _____

Transition delay in analog processing for 4,AO,2 during failover

_____ _____ _____

Transition period of 4,DO,8

Normal _____ _____ _____

During FO _____ _____ _____

Record SOE Report file name(s) for test execution.

Attachment 7.8 Power Supply Operability Tests

Refer to the test data record for TP901-202-04

Test Engineer _____ Date _____