HF CONTROLS

HFC-6000 Control System

ERD921 – TUV DMR SIL3 Safety System Qualification Project

Integration (Set-up and Check-out) Procedure

TP901-201-02 Rev B

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Revision History

Date	Revision	Author	Changes
3/25/10	A	I. Chow	Initial Release
5/7/10	B	I. Chow	Revised document according input from CR2009-0081

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1.0 PURPOSE AND SCOPE

The purpose of this procedure is to verify that the project specified hardware, wiring and communication cabling has been installed and that communication has been established over each communication link, prior to TSAP validation Test. Included in the scope of this procedure are the following activities:

- Verify that all project specified equipment / hardware has been received, functionally tested and set-up per project documents
- Verify correct software is installed in Test Specimen, HPAT and OIS/EWS
- Perform Continuity Test for all interconnection wiring
- Verify that C-Link communication has been established
- Verify that all HFC-6000 PCB's I/Os are functional and communicating with SBC06 controller

This test procedure constitutes part of the prequalification testing for the HFC-6000 control system. These tests are intended to demonstrate the DMR test specimen has been fully assembled and completely operational prior to the start of baseline performance testing.

2.0 REFERENCES

2.1 INDUSTRY STANDARDS

EPRI TR-107330	Generic Requirements Specification for Qualifying a Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants, 1996 (Ref. Para. 5.2.c)

2.2 RELATED PLANS AND PROCEDURES

VV901-300-01	ERD111/ERD921 Master Test Plan, Rev. B
TP901-200-00	Pre-Qualification Test Plan, Rev. A
VV901-301-02	ERD921 DMR Master Configuration List, Rev. A

2.3 SUPPORT DOCUMENTATION

500408-01	ERD111/ERD921 Power Distribution System Cabinet, Rev. B
500409-01	Loop Layout for ERD111/ERD921, Rev. B
700912-03	TSAP System Assembly, Rev. G
705004-04	TUV DMR Field Terminal Card Layouts, Rev. A
705008-04	TUV DMR I/O Card Layouts, Rev. A

2.4 HFC INTERNAL STANDARDS AND PROCEDURES

QPP 11.1	Test Control
WI-ENG-003	Configuration Management
WI-ENG-815	Red-Line Procedure

2.5 SPECIAL TERMS, ABBREVIATIONS, AND ACRONYMS

AI	Analog Input
AO	Analog Output
BOM	Bill of Material
DI	Digital Input
DO	Digital Output
EWS	Engineering Work Station
MCL	Master Configuration Listing
OIS	Operator Interface System
PCB	Printed Circuit Board
Test Specimen	A specific combination of hardware and software components to be subjected to specified test conditions
TSAP	Test Specimen Application Program

3.0 PREREQUISTES

3.1 GENERAL

The following paragraphs provide detailed instructions for setup and performance of the Integration (Setup and Checkout) Test. The Integration (Setup and Checkout) Test shall not commence until the equipment / hardware has been retrieved from inventory, PCBs installed functionally tested and installed, interconnection wiring, power distribution, communication cabling and HPAT wiring have been installed per the project documentation.

3.2 TEST EQUIPMENT REQUIRED

The following equipment will be required during performance of the Integration (Setup and Checkout) Procedure. Test personnel shall verify and document (see attachment 7.1) that test and measuring equipment are capable of producing the level of accuracy required by the specific test being performed and that the calibration for the MT&E to be used is current.

- NIST certified Fluke 187 Multimeter or equivalent
- Calibrated variable power supply at least 0 to 5 v dc

3.3 ENVIRONMENTAL CONDITIONS

The test will be conducted in a mild environment. The normal operating environment for the Test Specimen shall be as follows:

Temperature	50° to 104° F
Relative Humidity	7% to 90%

See section 4.1.1.

3.4 TEST PERSONNEL

Qualified HFC test engineers will be responsible for performing all phases of the Integration (Setup and Check-out) procedure.

The Integration (Setup and Check-out) procedure will be performed at the HFC facility.

3.5 RED-LINE POLICY

Red-line comments are used to correct errors of content and procedural sequence in test documents or in engineering drawings to prevent disruption of a test in progress. The procedure for performing red-line shall be done in accordance with WI-ENG-815, "Red Line Procedure".

4.0 TEST PROCEDURES

The Integration (Set-up and Checkout) procedure provides a separate evaluation for a specific aspect of the Test Sample performance and operation. Except as noted, in a particular test procedure, the testing shall adhere to the fixed sequence of execution as indicated below.

4.1 EQUIPMENT / HARDWARE SETUP

4.1.1 Equipment / Hardware Setup Prerequisites

1. Test engineers shall verify if the conditions are within the limits as specified in section 3.3 of this document.

2. Verify that the following documents in hand are a controlled copy of the latest revision according to Document Control:
    - BOM 700912-03
    - Drawing 500409-01, "Loop Layout for ERD111/TUV"
    - Drawing 700912-03, "ERD111/ERD921 TSAP Assembly"

3. Verify the Commercial Grade testing for the following items have been performed and documented:
    - KEPCO Power Supplies and rack
    - HFC-6000 PCBs

4. Verify all I/O Cable Assemblies with the following drawings:

    TSAP DMR Drawings (705004-04; 705008-4)
    HPAT Drawings (700908-01)

5. Verify all Test Specimen PCBs and power supplies have started the burn-in test. (The burn-in period is a minimum of 352 hours. Not until the burn-in period is completed shall operability and prudency tests be performed on the test specimen.)

Equipment / Hardware Setup perquisites are complete: _____

Test Engineer/Date

4.1.2 Equipment / Hardware Test Procedure

BOM and Drawing 700912-03 Rev _____ BOM Rev _____ **Initial**

1. Verify each piece of hardware is located and communication cables installed _____
2. Visually check all hardware for damage _____
3. Highlight each piece of hardware and cabling that has been checked (with yellow highlighter) _____
4. Upon completion, initial and date the drawing _____

Drawing 500409-01 Rev _____

1. Verify each Test Specimen's PCB dip switch settings have been set per project documents _____
2. Verify each Test Specimen PCB and bezel have been installed in the correct rack and slot _____
3. Highlight each Test Specimen PCB that has been checked (with yellow highlighter) _____
4. Upon completion, initial and date the drawing _____

Drawing 705004-04 Rev _____; 705008-04 Rev _____

1. Verify the connections of these drawings are connected correctly with the terminal blocks and cards. _____
2. Upon completion, initial and date the drawing _____

4.2 CONTINUITY TEST

4.2.1 Continuity Test Prerequisites

1. Verify that the following drawings in hand are controlled copies of the latest revision according to Document Control:
    - Drawing and BOM 700912-03, "TSAP System Assembly"
    - Drawing 500408-01, "ERD111/ERD921 Power Distribution"
2. Verify that the Multimeter has not exceeded its calibration date
3. Verify Equipment / Hardware Set-up is complete and validation is signed

Continuity Test prerequisites are complete: _____

Test Engineer/Date

4.2.2 Continuity Test Procedure

Drawing 500408-01 Rev _____ **Initial**

1. Perform Continuity check for all circuits depicted _____
2. Highlight each checked circuit (with yellow highlighter) _____
3. Upon completion of all circuits, initial and date the drawing _____

Drawing and BOM 700912-03 Rev _____ BOM Rev _____

1. Confirm that BOM Mark Numbers: 5, 16, 19, 21, 23 and 33 communication cables are installed _____
2. Highlight each checked cable and BOM Mark No. (with yellow highlighter) _____
3. Upon completion of all circuits, initial and date the drawing _____

4.3 C-LINK COMMUNICATION

4.3.1 C-Link Communication Tests Prerequisites

Prerequisites for Communication Test between the Test Specimen, HPAT and other peripherals are as follows:

1. Verify that Equipment Setup met acceptance criteria listed in section 5.0 and validation is signed
2. Verify that Continuity Test A met acceptance criteria listed in section 5.0 and validation signed
3. Verify that EWS Installation Pack software is installed
4. Verify Application Software and System Software have been installed
5. Verify that System Status Graphics are installed

C-Link Communications Test prerequisites are complete: _____

Test Engineer/Date

4.3.2 C-Link Test Procedure

C-Link Functional Test validates the data broadcasted using EWS/OIS.

HFC-SCG06 and OIS/EWS

	Initial
1. Connect a CAT5 cable to the A1 connector of the primary HFC-SCG06.	_____
2. Verify EWS Memory Editor can read memory from HFC-SCG06, rem 8	_____
3. Put the Memory Editor in repeat mode for 60 seconds	_____
4. Verify there are no communication errors	_____
5. Disconnect cable at A1.	_____
6. Connect a CAT5 cable to A0 connector for the primary HFC-SCG06.	_____
7. Verify EWS Memory Editor can read memory from HFC-SCG06, rem8	_____
8. Put the Memory Editor in repeat mode for 60 seconds	_____
9. Verify there are no communication errors	_____
10. Connect CAT5 cable to A1.	_____
11. Failover the SCG06 to have the secondary controller take over.	_____
12. Repeat steps 1 - 10	_____

Verify C-Link between SCG06 and OIS/EWS: _____
Test Engineer/Date

HFC-SCG06 and Test Specimen

	Initial
1. Verify the LAN cables are connected correctly to HFC-SCG06.	_____
2. Verify the DDB data being broadcasted from the Test Specimen.	_____
3. On MCRT index screen, verify there are no C-Link errors on the remotes.	_____

Verify C-Link between SCG06 and Test Specimen: _____
Test Engineer/Date

4.4 I/O FUNCTIONAL TEST

4.4.1 I/O Functional Test Prerequisites

Prerequisites for I/O Functional Test are as follows:

	Initial
1. Verify that Equipment Setup meets acceptance criteria and validation signed	_____
2. Verify that Continuity Test meets acceptance criteria and validation signed	_____
3. Verify that C-Link Communication Test meets acceptance criteria and validation signed	_____
4. Verify that the Multimeter has not exceeded its calibration date.	_____
5. Verify the variable power supply has not exceeded its calibration date.	_____
6. Verify that all of the following project required PCBs have been tested and configured per the applicable test procedure:	

Device	Calibration Required	Calibration Verified (Initials)
HFC-AI16RD (Analog Input - 0-5 vdc)	Y	_____
HFC-AO8FD (Analog Output - 4-20 mA dc)	N	

I/O Functional Test prerequisites are complete: _____

Test Engineer/Date

4.4.2 I/O Functional Test Procedure

1. The I/O Functional Test will consist of functionally testing all digital and analog I/Os individually which are used in the system.
2. The I/O Functional Test also serves as the I/O and Controller Communication Test because it verifies communication between the individual I/Os and the controller

Digital Inputs (HFC-DI16I) **Initial**

1. Simulate a contact closure by placing jumper across used DI channels. _____
2. Verify that applicable system status graphic dynamic DI symbol lights up _____
3. Verify the respective DI I/O channel's LED on the PCB lights up _____
4. Highlight I/O Module symbol and associated digital inputs on the applicable loop schematics, 705008-04 _____
5. Upon completion, initial and date the drawing. _____

Write down the information of the I/O cards verified through the procedure above.

Card Type	Location (Remote #, Slot #)

Test Engineer: _____ **Date:** _____

Digital Outputs (HFC-DO16C) **Initial**

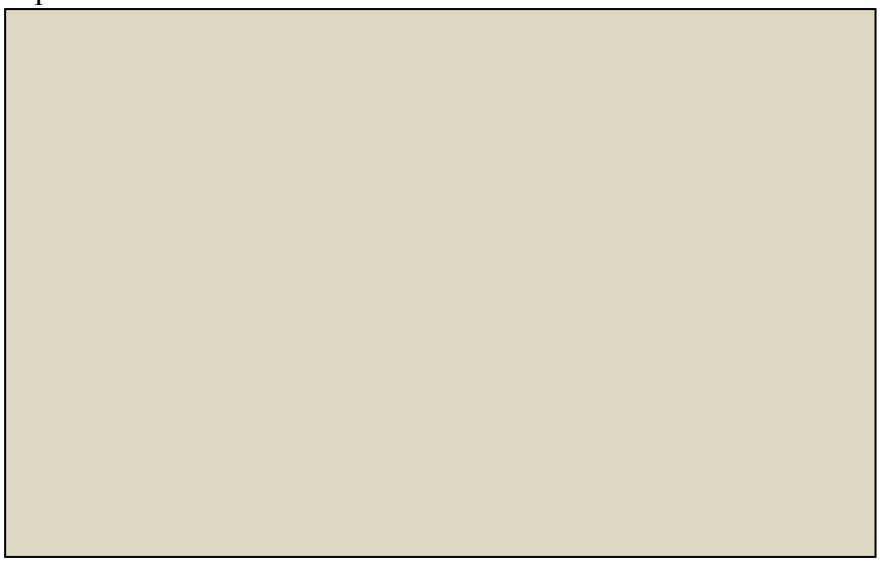
1. Display Equation Editor for remote 4. _____
2. Use the equation listed below. Compile and download. _____
3. Verify that applicable system status graphic dynamic DO symbol lights up _____
4. Verify the respective DO channel's LED on the PCB lights up _____
5. Highlight I/O Module symbol and associated DOs on schematic 705008-04. _____
6. Restore Equations. Upon completion, initial and date the drawing. _____

Write down the information of the I/O cards verified through the procedure above.

Card Type	Location (Remote #, Slot #)

Test Engineer: _____ **Date:** _____

Equation:



Analog Inputs – 0-5 vdc (HFC-AI16RD) **Initial**

1. Use loop schematic, 705008-04 the wire configuration is being utilized. _____
2. Supply 1,0, 2.5 and 5 vdc input signals to each used AI channel. _____
3. Use memory editor to verify the AI signal display tracks the 1.0, 2.5, 5 v dc generated signals. Readings will be depicted in raw counts: 6521 - 6585, 16352 – 16416, and 32735 – 32767, respectively. _____
4. Highlight I/O Module symbol and associated AIs on schematic 705008-04 _____
5. Upon completion, initial the date the drawing. _____

Write down the information of the I/O cards verified through the procedure above.

Card Type	Location (Remote #, Slot #)

Test Engineer: _____ Date: _____

Analog Outputs - 4-20 mA dc (HFC-AO8FD) **Initial**

1. Display CQ4 Editor. _____
2. Utilizing a Calibrator, connect probes to each used individual AO's channel. _____
3. Change control SP for applicable analog output. _____
4. Utilizing CQ4 Editor analog output screen, select 0, 50 and 100% values. _____
5. For each output value, verify the System Status Graphic dynamic analog output value tracks the 0, 50 and 100% values. Readings will be depicted in raw counts, 819, 2457 and 4095 respectively. _____
6. Verify the Calibrator tracks the three point generated signals. Calibrator readings should be 4, 12, and 20 mA dc (+/- 0.1% - approx +/-, 0.02 mA) respectively _____
7. Highlight I/O Module symbol and associated analog inputs on the applicable loop schematics, 705008-04 _____
8. Upon completion, initial and date the drawing. _____

Write down the information of the I/O cards verified through the procedure above.

Card Type	Location (Remote #, Slot #)

Test Engineer: _____ **Date:** _____

5.0 ACCEPTANCE CRITERA

5.1 EQUIPMENT / HARDWARE ACCEPTANCE CRITERIA

1. BOM and Drawing 700912-03
   - All hardware components and communication cables depicted on BOM and drawing 700912-03 have been highlighted and signed.
2. Drawing 500409-01
   - All Test Specimen's PCBs depicted on drawing 500409-01 have been highlighted and signed.
3. Drawings 705008-04, 705004-04
   - All connections shown on these drawings have been validated.

5.2 CONTINUITY TEST ACCEPTANCE CRITERIA

1. Drawing 500408-01
   - All circuits depicted on drawings 500408-01 have been highlighted and signed.
2. Drawing and BOM 700912-03
   - BOM Mark Numbers: 5, 16, 19, 21, 23 and 33 have been highlighted and signed.

5.3 C-LINK TEST ACCEPTANCE CRITERIA

1. HFC-SCG06 and OIS/EWS
   - Verify the EWS Memory Editor can read memory from HFC-SCG06
2. Test Specimen and OIS/EWS
   - Verify EWS are receiving DDB status from Test Specimen

5.4 I/O FUNCTIONAL TEST ACCEPTANCE CRITERIA

1. Digital Inputs, DI16I
   - All DI channels on the loop schematics have been highlighted and signed
2. Digital Outputs, DO16C
   - All DO channels on the loop schematics have been highlighted and signed
3. Analog Input, 0-5 vdc AI16RD
   - All AI (0-5 vdc) channels on the loop schematics have been highlighted and signed
4. Analog Outputs, AO8FD
   - All AO (0-20 mAdc) channels on the loop schematics have been highlighted and signed

5. Redundant Communication Gateway (HFC-SCG06)
    - C-Link communications acceptance criteria are met.

6.0 QA RECORDS

Both the test procedure with completed signoffs and the attachment 7.1 shall be reserved in accordance with QPP 17.1 “Quality Records”.

7.0 ATTACHMENTS

Attachment 7.1 – Test Equipment Log

Attachment 7.1 – Test Equipment Log

Test Data Record

Test Plan: TP901-200-00, "Pre-Qualification Test Plan", Rev. A

Test Equipment Log

Test Equipment	Instrument ID	Calibration Due Date
Multimeter		
HP 0-20 vdc Power Supply		
EWS/OIS		

Test Engineer, Date