HF Controls

HFC-6000 Qualifying System
ERD921
Environmental Stress Detail Test Report

TR901-201-03 Rev. A

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[XXXXXXXXXXXXX]

Revision History

Date	Revision	Author	Changes
6/11/15	A	Y. Lu	Initial release for detail environmental retest results at Environmental Testing Laboratory for ERD921 Test Specimen.

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1.0 Introduction

1.1 *Purpose*

An environment stress test was performed for the ERD921 test specimen for Doosan HF Controls (HFC) HFC-6000 platform. This report contains an analysis of the Operability tests (TP901-201-04,TP901-202-04,TP901-203-04) and Prudency tests (TP901-201-05, TP901-202-05, TP901-203-05) that were executed at various times during the environmental stress retest. The primary purpose for these tests was to provide objective evidence that the ERD921 test system continued to operate within specified limits before, during, and after being subjected to environmental stress conditions.

2.0 References and Acronyms

2.1 *Industry References*

EPRI TR 107330	Generic Requirements Specification for Qualifying a Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants, 1996

2.2 *HFC References*

50040801	ERD111/ERD921 Power Distribution System Cabinet, Rev. D
50040901	Loop Layout Table of PCB Assemblies ERD111/TÜV, Rev. B
QPP 17.1	Quality Process Procedures – Quality Record
TP901-201-04	DMR Operability Test Procedure, Rev E
TP901-202-04	TMR Operability Test Procedure, Rev D
TP901-203-04	SLC Operability Test Procedure, Rev C
TP901-201-05	ERD921 DMR Prudency Test Procedure, Rev B
TP901-202-05	ERD921 TMR Prudency Test Procedure, Rev C
TP901-203-05	SLC Prudency Test Procedure, Rev B
TP901-200-02	EPRI TR 107330 Environmental Stress Test Procedure, Rev. D
VV901-301-02	TUV DMR Master Configuration List, Rev C
VV901-302-02	TUV TMR Master Configuration List, Rev C
VV901-303-02	HFC-SBC04A System Master Configuration List, Rev C
VV901-300-01	ERD111/ERD921 Qualification Master Test Plan, Rev B

2.3 *Acronyms*

EPRI	Electrical Power Research Institute
ERD921	Engineering R&D Project 921
HFC	Doosan HF Controls/HF Controls
HPAT	HFC Plant Automated Tester
HAS	Historical Archiving System
I/O	Input/Output
NRC	Nuclear Regulatory Commission
PLC	Programmable Logic Controller
RTD	Resistive Temperature Detector
SER	Safety Evaluation Report
SLC	Single Loop Controller

3.0 Testing Information

3.1 *Venues*

The environmental stress tests were conducted at the Environmental Testing Laboratory, an ISO/IEC 17025 certified laboratory. The laboratory is located at 11034 Indian Trail, Dallas, Texas 75229-3513.

The testing period was from July 1st, 2010 until July 17th, 2010.

3.2 *Test Specimen Equipment List*

The HFC-6000 modules installed in the ERD921 test specimen are listed in the following table.

Table 1 – ERD921 Test Specimen HFC-6000 Modules

Quantity	Modular Type	Description
2	**PS, Jasper 24V**	**600W 24V Power Supply**
1	Rack, Jasper PS	8-slot Jasper PS Rack, 19"
1	HFC-HUB06-16-01	16 Port 10/100 Hub
1	HFC-HUB06-16-02	16 Port 10/100 Hub
1	HFC-HUB06-16-EXT	Hub Extender
1	**HFC-BPC01-19**	**Controller Chassis backplane**
1	HFC-BPC03-08	3 Loop, 8 inch backplane
5	**HFC-SBC06**	**Main Controller**
4	**HFC-DPM06**	**Dual-Ported Memory**
2	HFC-SCG06	Communication Gateway
1	HFC-DPM06BP	Backplane Connected DPM06
12	**HFC-DI16I**	**Digital Input Card with SOE**
8	HFC-DO16C	Solid State Output Card
6	HFC-AI16RD	Analog Input Card (0 – 5 vdc) (DSP)
6	HFC-AO8FD	Analog Output Card (4 – 20 mA) (DSP)
3	HFC-AI8LD	Thermocouple Input Card
3	HFC-AI8MD	RTD Input Card, 100 ohm (DSP)
2	HFC-FOT06	Fiber-Optic Transmitter
4	**HFC-ILR06**	**I/O Link Repeater/Terminator**
1	**HFC-BPE01-19**	**Expander Chassis backplane**
1	HFC-SBC04A	Single Loop Controller
1	HFC-AC36FD	Analog I/O Module

Figure 1 shows the layout of the modules inside the qualification cabinet. Only racks and locations marked with "TMR/DMR/SLC" apply to the HFC-6000 ERD921 listed equipment.

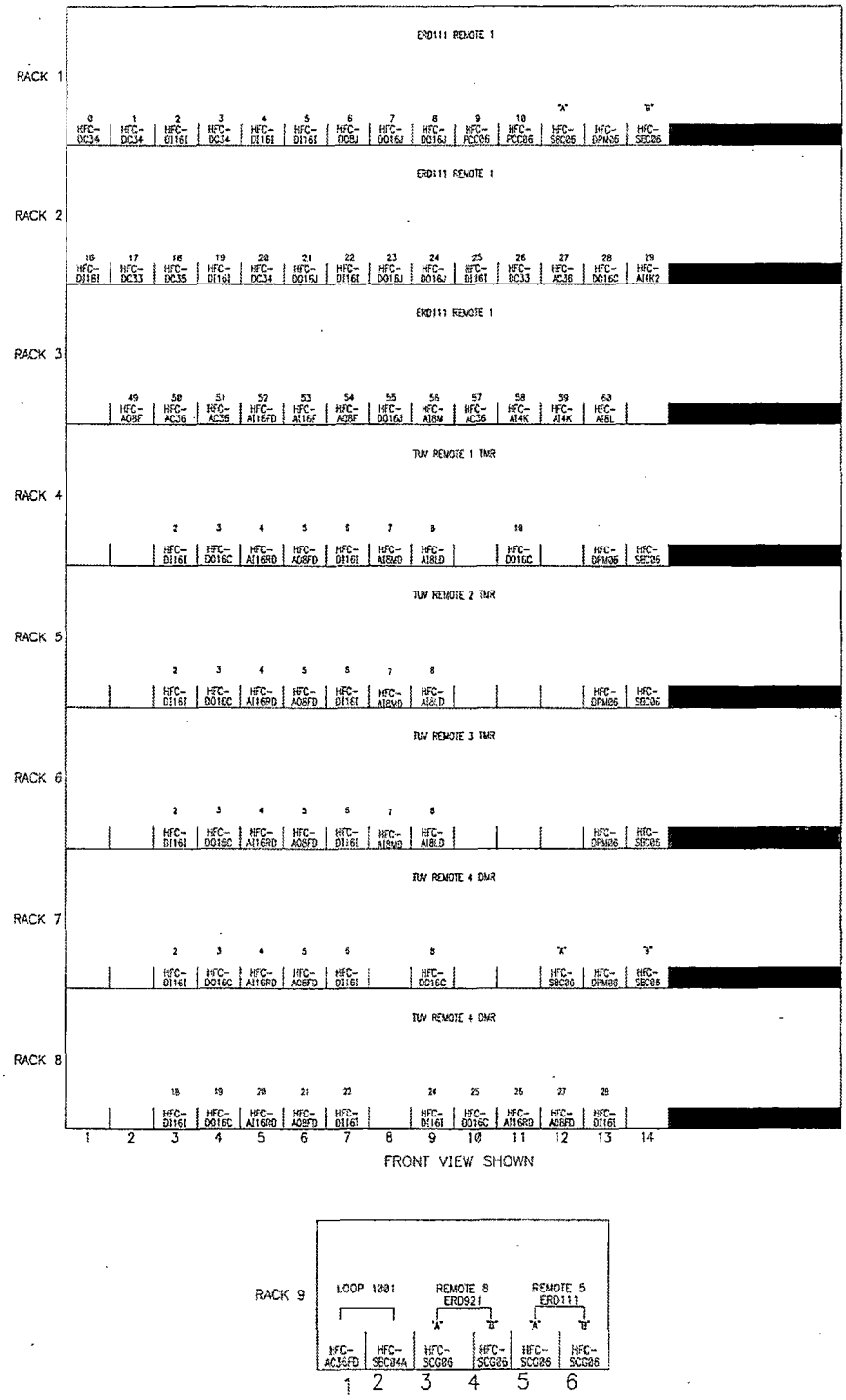


Figure 1 – Equipment Layout in the Cabinet

3.3 *Environmental Stress Validation Tests*

As specified in EPRI TR 107330-1996, operability checks or validation tests are required to ensure that the platform performs properly in various environment stress conditions as shown in Figure 2.

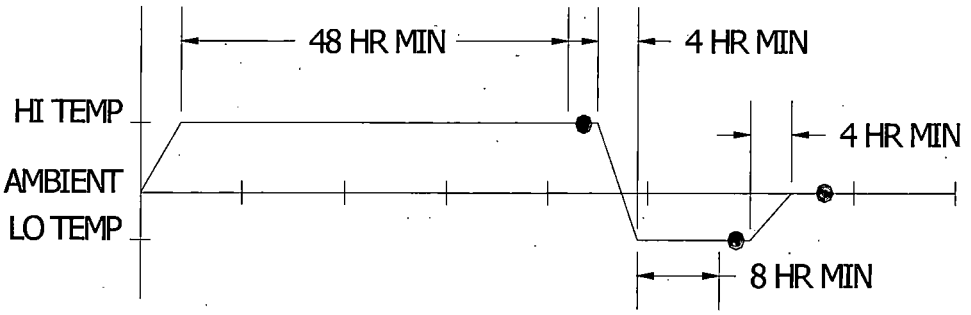


Figure 2 – Environmental Stress Test Profile

Note: The black dots on the graph designate the operability check points required by the standard.

High humidity ~90% during high temperature and low humidity ~5% during low temperature were maintained. In the rest of this report, the humidity conditions are implied by the temperature and will not be mentioned again.

These validation tests are grouped into operability and prudency tests in accordance with EPRI TR 107330. Refer to the standard for the details of these test descriptions.

3.3.1 Operability Tests

The following tests are required for the operability checks in accordance with EPRI TR 107330 as noted in Figure 2:

A. Accuracy
B. Response Time
C. Discrete Input and Output Operability
D. Communication Operability
E. Timer
F. Failure to complete scan detection
G. Failover Operability
H. Loss of Power
I. Power Interruption
J. Power Quality (Only performed after the end of high temperature testing period)

The required coprocessor operability tests were excluded because there is no coprocessor usage in HFC-6000 platform.

3.3.2 Prudency Tests

In addition to the operability tests, prudency tests are required only after the high temperature stress period in accordance with EPRI TR 107330-1996. The required burst of event tests (BOE) were divided into digital BOE and analog BOE tests. The digital BOE tests are also used for validating the discrete input/output operability of the test specimen. Detail test results and analyses are provided in the following section.

4.0 Test Results

During the environment stress retest, the time of exposure of the ERD921 test specimen to the high temperature/high humidity (HT/HH) was longer than 48 hours. The first set of operability tests not related to power supplies were performed after the initial exposure of 48 hours. In order not to disrupt the operations, operability tests related to power supplies and power quality were performed at the end of HT/HH exposure before ramping down to low temperature/low humidity. A set of prudency tests were also performed during the first operability checkpoint at the end of the initial 48 hours exposure of HT/HH. No anomalies for the ERD921 test specimen were found at any operability checkpoints. The stress profiles applied during the environmental tests are shown in the following figures.

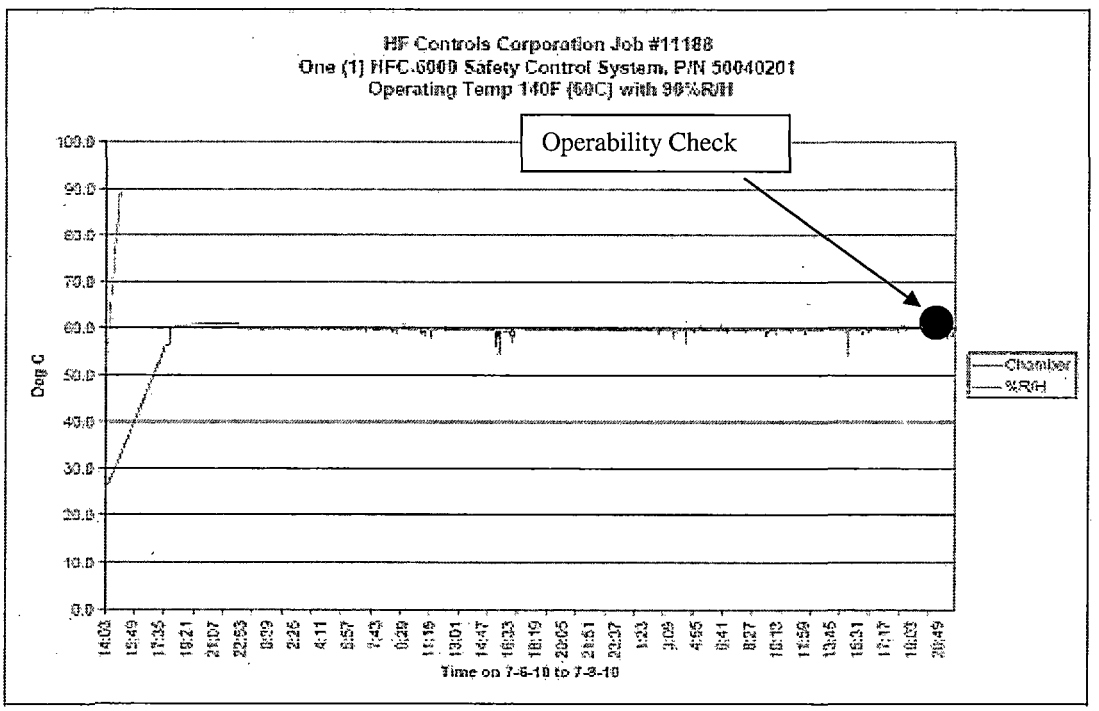


Figure 3 – Profile of High Temperature Stress I during Operation

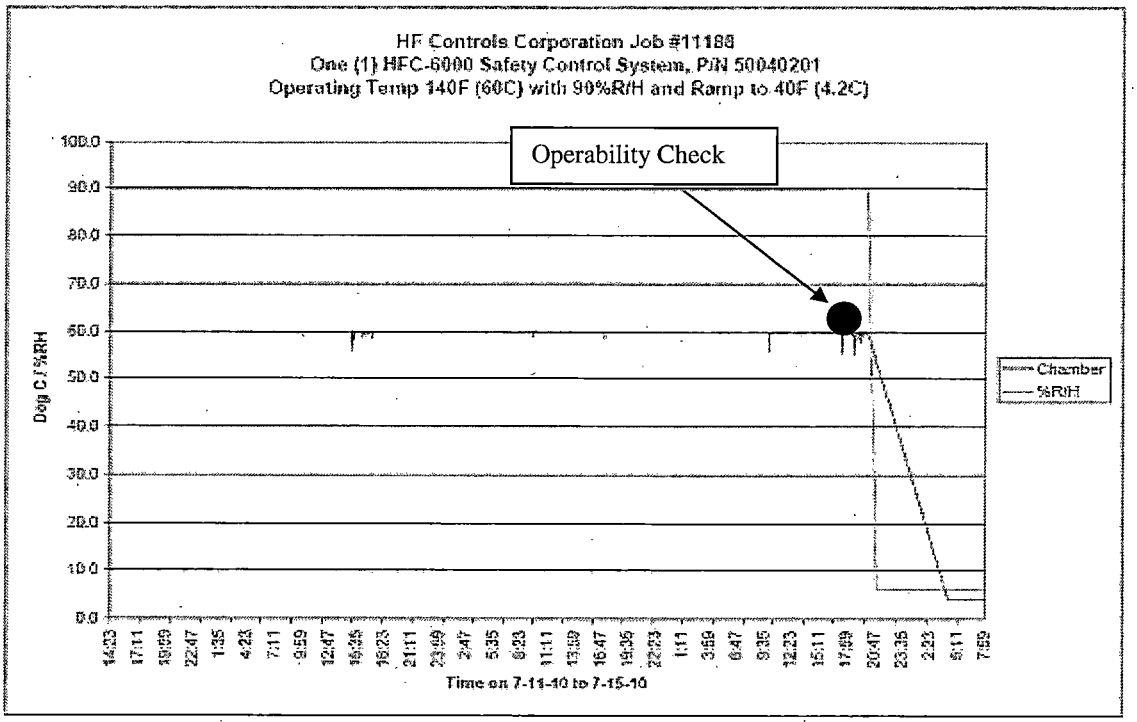


Figure 4 – Profile of High Temperature Stress II during Operation

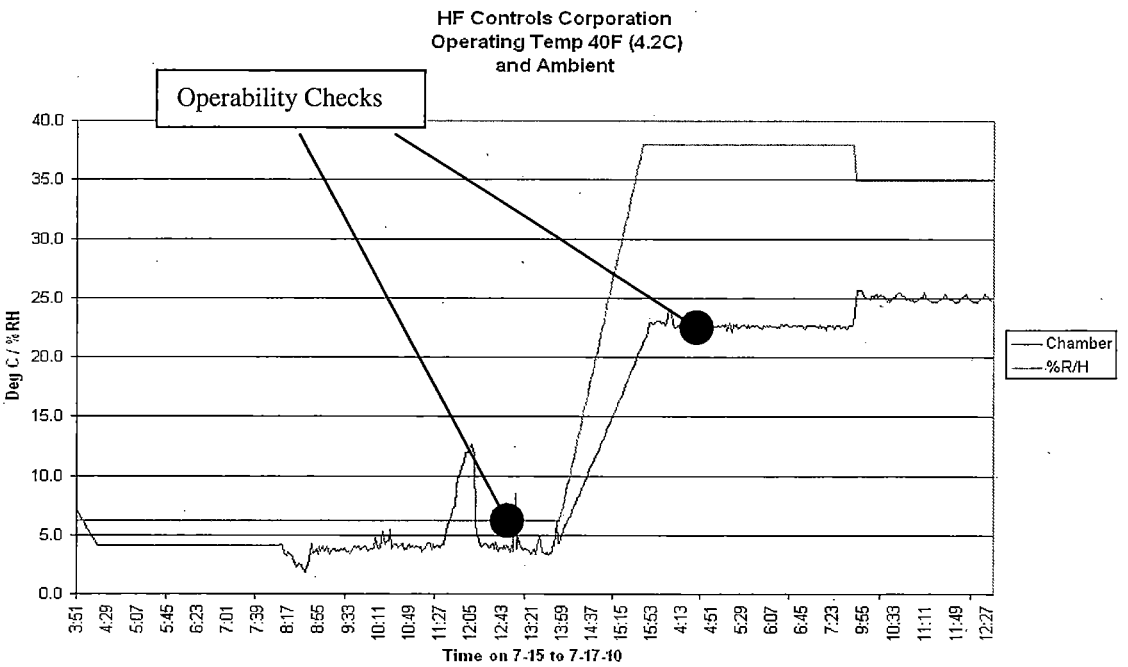


Figure 5 – Profile of Low Temperature Stress during Operation

Note: After arriving to the Environmental Testing Laboratory (ETL), before starting the environmental stress tests, a pretest consisting of operability and prudency tests was performed. The purpose of the pretest was to validate the ERD921 test specimen was properly setup after it was disassembled at the HFC facility and shipped to the ETL. The pretest data were analyzed and were found satisfactory as compared to the baseline data collected at the HFC facility. Since the focus of this report is the performance data during the environmental stress periods, the pretest data and results are not presented.

As shown in the figures above, the complete ERD921 test specimen was subjected to an environmental stress profile more than the required stress profile shown in Figure 2. The period of stressing in the high elevated temperature of 60°C/140°F or higher was 218 hours instead of 48 hours. The period of stressing in low temperature of 4.4°C/40°F or lower was 10 hours instead of 8 hours. In addition, there were stress cycles before and after the high temperature and low temperature stresses. These additional stress cycles were performed for qualifying to a different standard.

The required operability and prudency tests at the end of high temperature stress in operation were performed after 48 hours of 60°C/140°F environmental stress on July 8. The extended high temperature stress period of 218 hours was related to a device which was not part of ERD921 test specimen. The low temperature stress exposure was conducted after 4 hours ramp down time after the 218 hours of the elevated high temperature. Operability tests were performed after an 8-hour of 4.4°C/40°F environment stress. After two stress cycles of 54°C and 4.4 °C, another operability check was performed at ambient temperature. The following sections provide the detail information of the test results performed during these periods.

4.1 *Operability Tests*

4.1.1 Accuracy

At least one channel of each analog device included in the ERD921 Test System was included in the analog accuracy tests. The specific channels and I/O cards covered are listed in Table 1.

Table 2 – ERD921 Analog I/O Channels Covered by Accuracy Testing

Equipment Type	Channel Tested	Test Type
TMR Accuracy Tests		
[redacted]		Manual and automated tests
		Manual and automated tests
		Manual and automated tests
		Manual and automated tests
DMR Accuracy Tests		
[redacted]		Manual and automated tests
		Manual and automated tests

SLC Accuracy Tests	
[redacted]	Manual and automated tests

All of the manual tests were executed during the Operability pre-qualification testing conducted at the HFC test facility before the test cabinet was placed in the environmental test chamber. The purpose of the manual tests was twofold:

- Demonstrate that the ERD921 analog hardware operated within specified calibration limits prior to the start of stress testing.
- Determine the magnitude of any systemic error introduced by the test hardware being used to control and log the automated test.

The automated tests were run during the pretest at HFC, prior to the start of the environmental stress test, and at various points during the environmental stress tests. Results from the automated tests were logged by an Historical Archiving System (HAS), which was running on a PC workstation that was external to the ERD921 test system.

The test configuration consists of a five-step algorithm running in both the HPAT and in the ERD921 TSAP. See Figure 6. While the automated test was running, the HPAT generated one image of the test algorithm, and the TSAP generated a second image of that algorithm. The HPAT provides inputs to the AI channels in the ERD921 test specimen. The images of the AI channels were logged through HFC HAS server. The algorithm in the ERD921 test specimen drove AO channels to the HPAT whose values were logged through HFC HAS server.

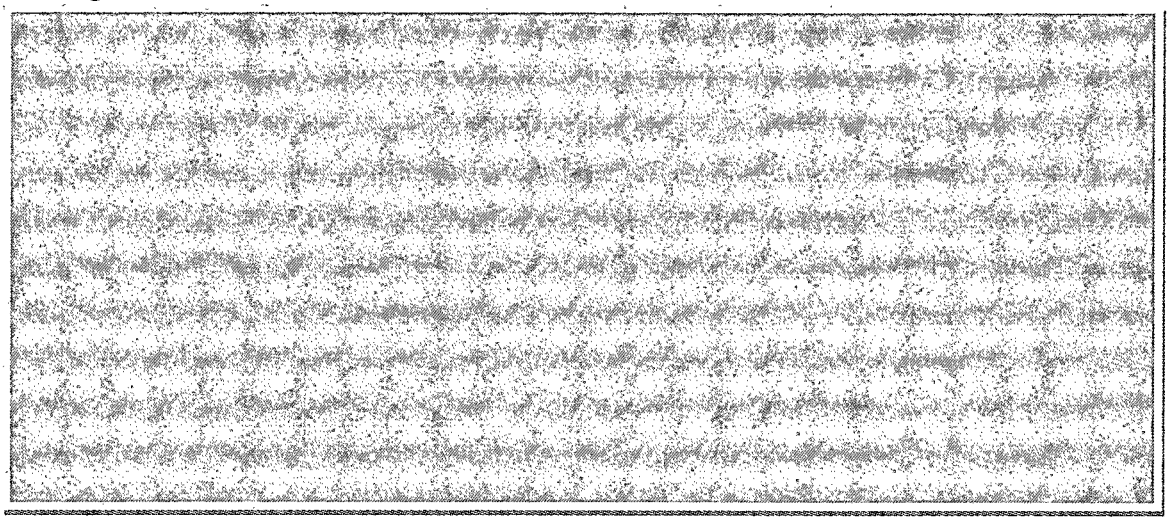


Figure 6 – Algorithm for 0 to 5V Analog Channel Accuracy Test

The automated analog accuracy I/O test was run before, during, and after environmental stress test. The following seven tables summarize the results obtained. The results shown in the table contain averaged values for each step level. Each step level of the algorithm lasted for 20 seconds, and each test run included from two to four repetitions of each level.

Acceptance criteria for these channels as specified in TP0402 in accordance with EPRI TR 107330 are as follows:

4 to 20 mA AI Channels

During qualification test — Accuracy within ±0.35% of span over the entire range

4 to 20 mA AO Channels

During qualification test — Accuracy within ±0.32% of span over the entire range

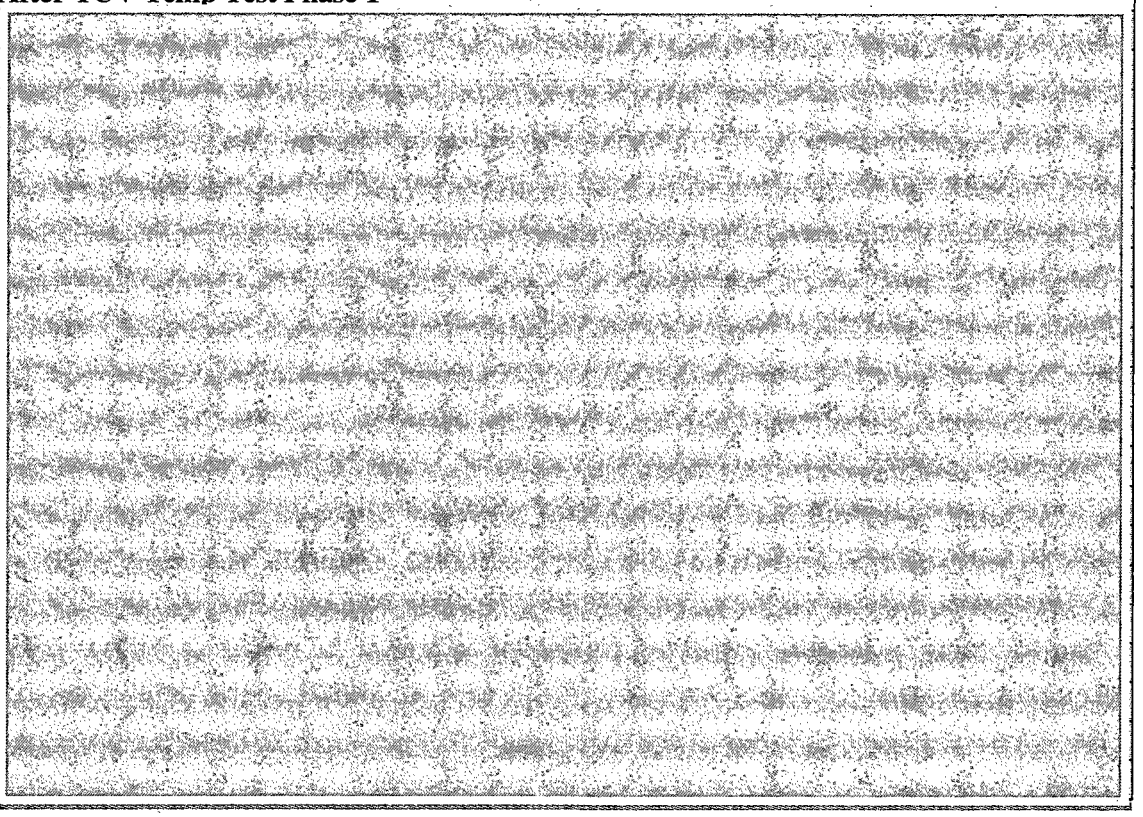
4.1.1.1 AI16RD to AO8FD Accuracy

HAS log point, 1,BL,51 provides an image of an AI channel for AI16RD, 1,AI,5. This log point was monitored throughout the operability tests performed at the end of the high temperature stress period, at the end of the low temperature stress period, and at the end of back to the ambient period.

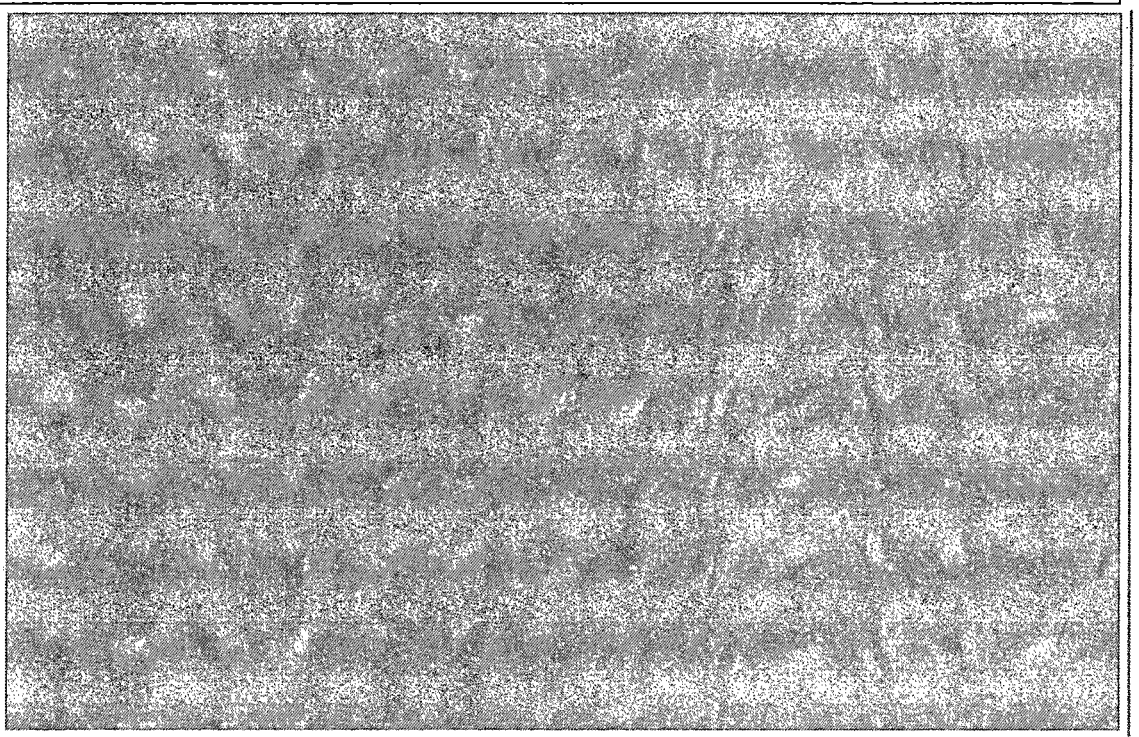
The test data were analyzed and the accuracy results are listed in *Table 3*. In each step level of all testing periods, the accuracy of the AI16RD measured was well within ±0.35% of span over the entire range. AI16RD, therefore, meets the acceptance criteria of accuracy in an environmental stress profile in accordance with EPRI TR 107330.

Table 3 – HFC-AO8FD-HFC-AI16RD Accuracy Test Results

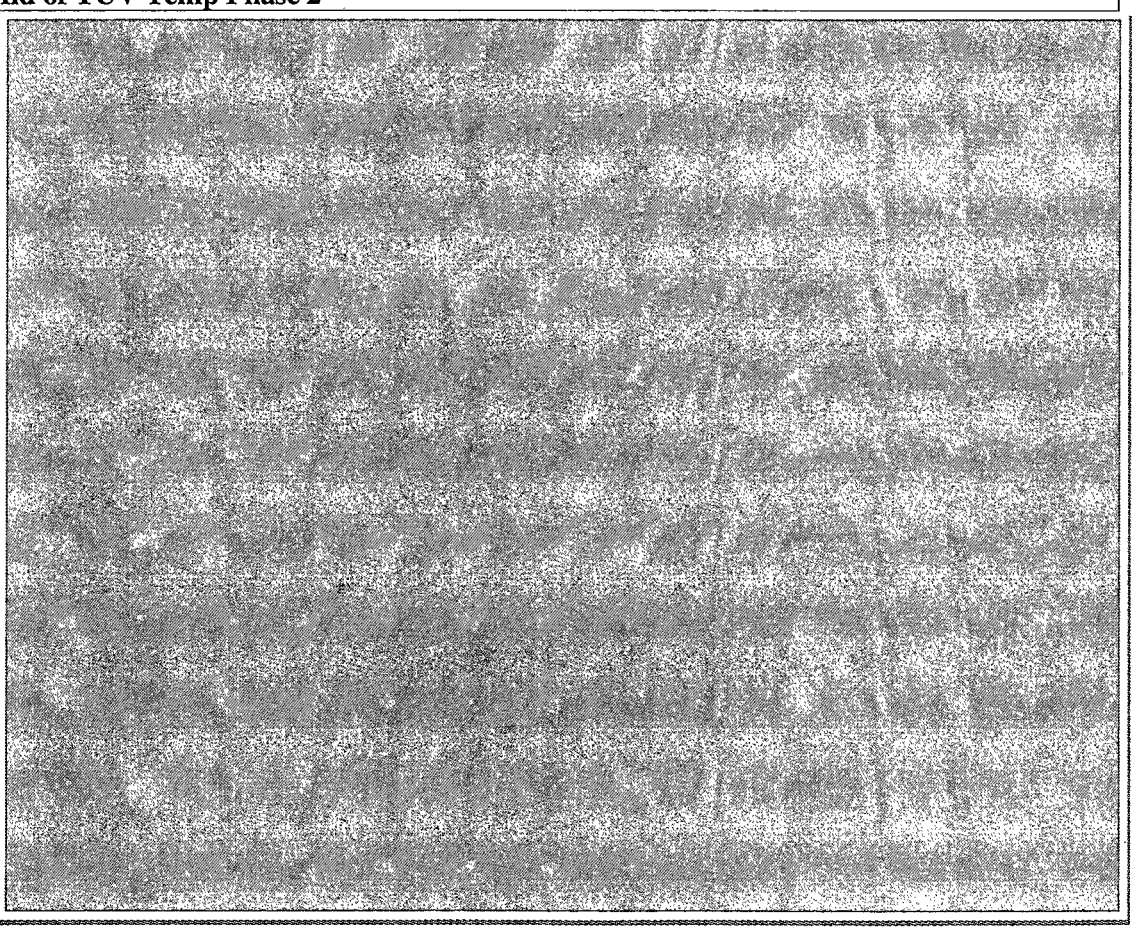
Step Level	Raw Averaged Image	% Average	% Accuracy
After TUV Temp Test Phase 1			

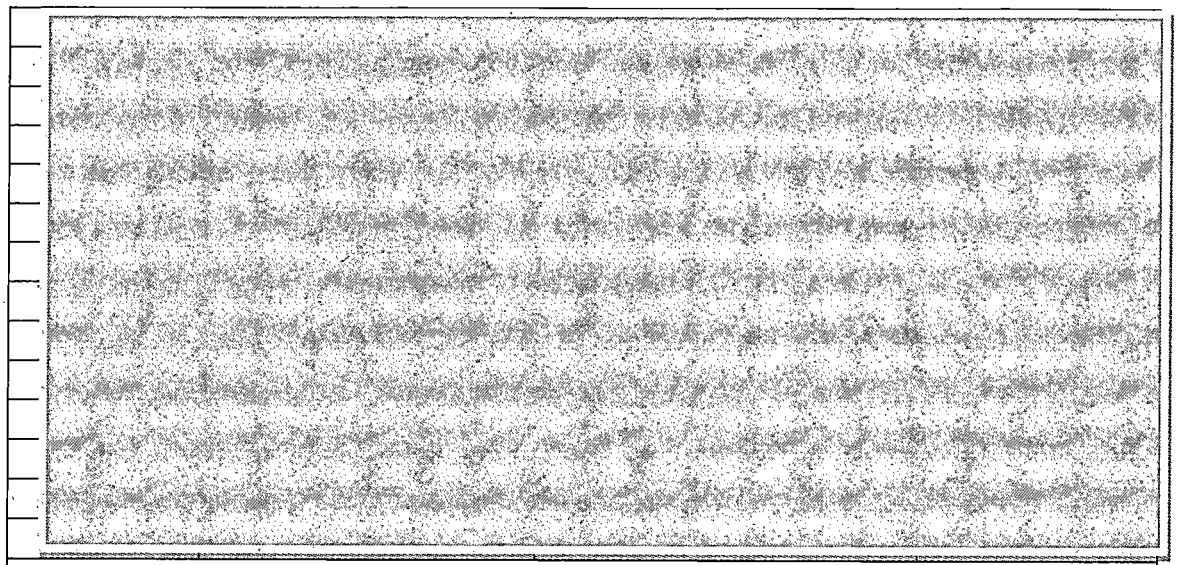


After 140°F Test

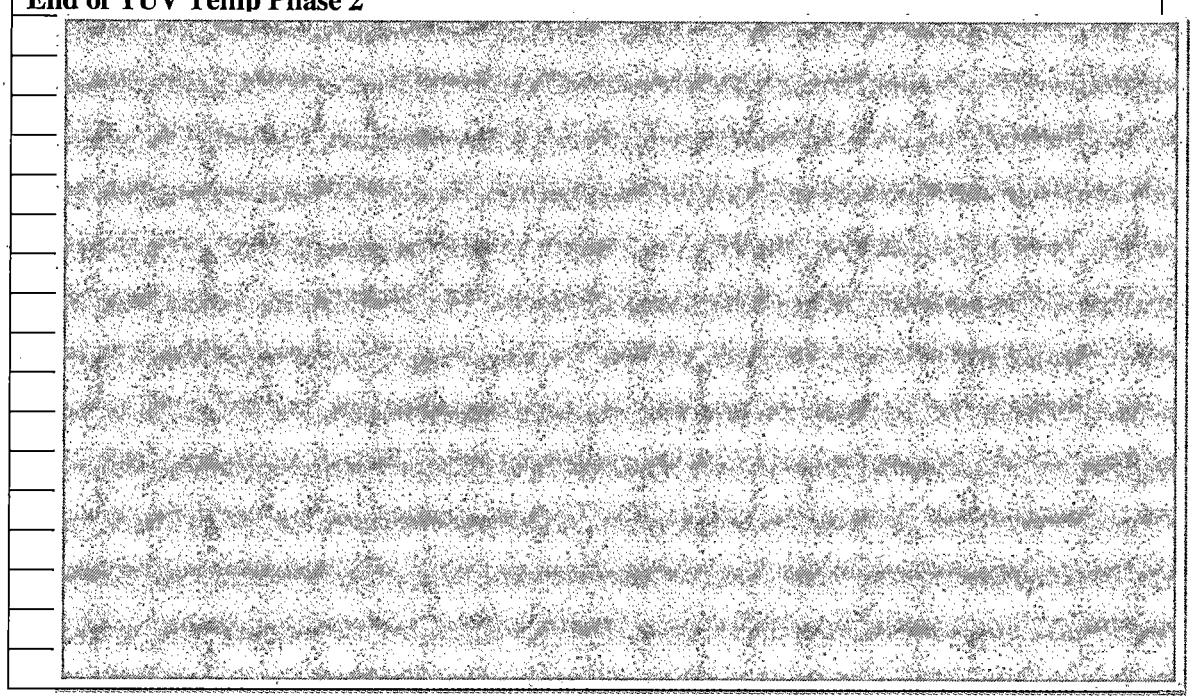


Mid of TUV Temp Phase 2





End of TUV Temp Phase 2



The following figure shows the input measurements of the AI16RD continued to exhibit linearity in each environmental stress period

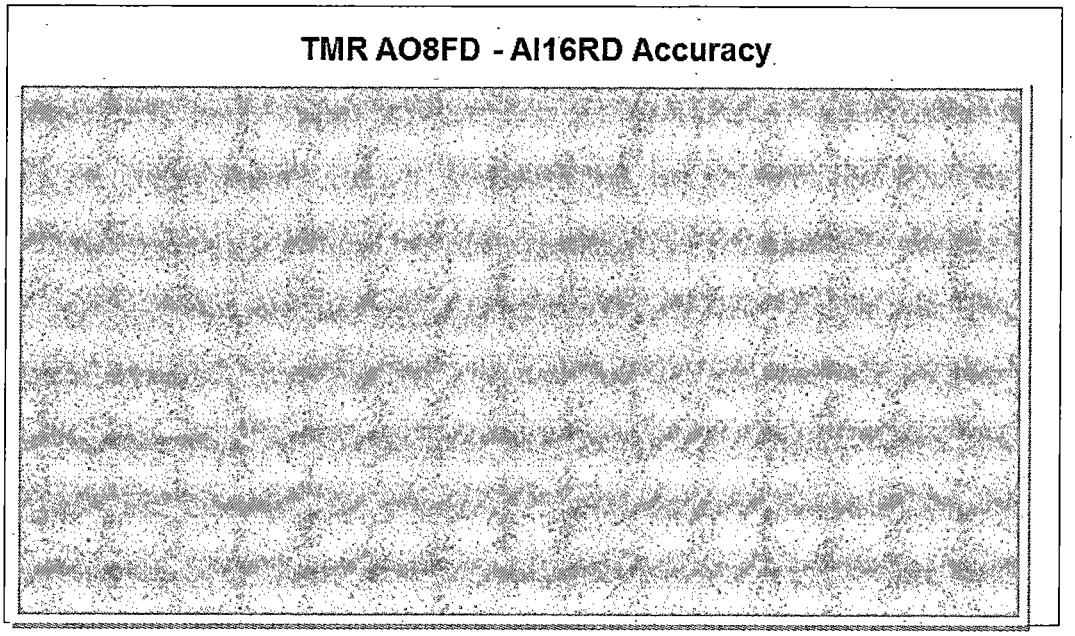


Figure 7 – AI16RD Accuracy Data during the Environmental Stress Periods

4.1.2 Response Time

The ERD921 test system was configured to run separate algorithms for digital and analog response time, which were run during each phase of the environmental test. The purpose of these tests was to provide objective evidence for the processing characteristics of the controller hardware during environmental stress conditions.

4.1.2.1 Digital Response Time

The automated digital response time test used two different algorithms. See *Figure 8*. The first algorithm consists of seven consecutive DI points driving seven consecutive DO points within the TSAP, and hard-wire connections routed the DO signals to the input points for those DI channels. When the test was enabled, these points produced a free-running algorithm that required 14 transfer passes to produce a single cycle. Consequently, dividing the average period by 14 produced one measure for the input-to-output response time.

The second algorithm consists of a single input from the HPAT that set/reset an MS point within the TSAP. The image of this MS point then controlled a trip output, so the delay between the transition of the input from the HPAT to the response of the trip output constitutes a direct measure of the input-to-output response time of the ERD921 controller.

- The measured response time shall not vary by more than ±10% from the measured baseline value.

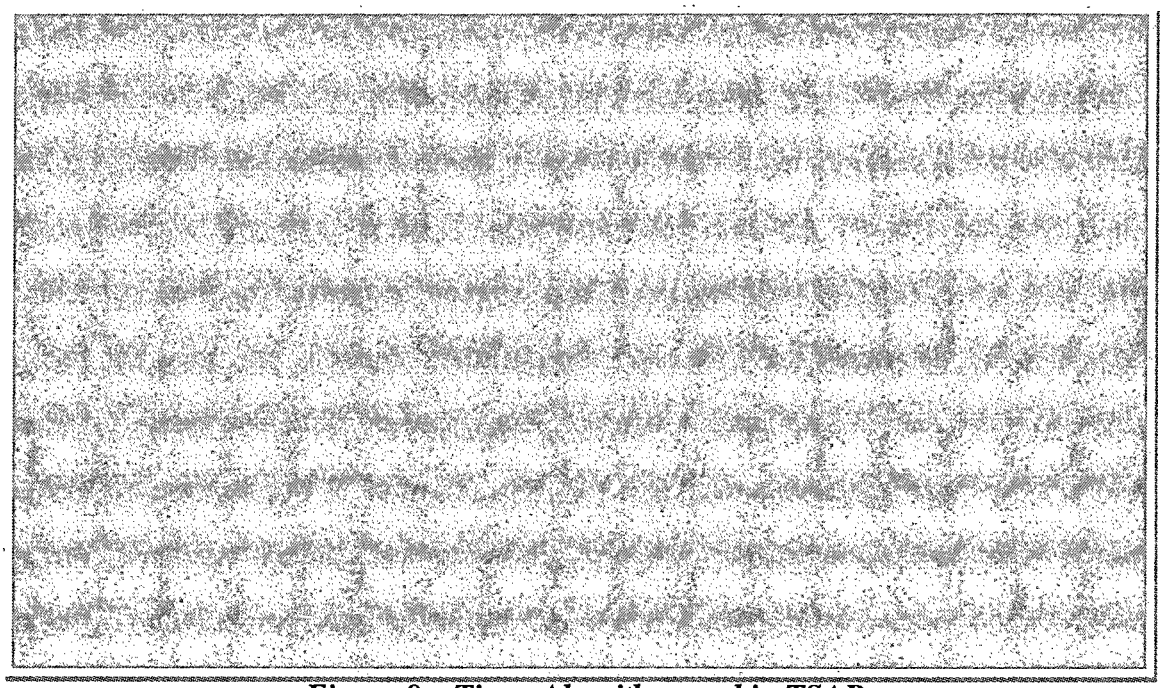


Figure 8 – Timer Algorithm used in TSAP

Table 4 lists a summary of the digital response time data logged during the environmental stress test.

Table 4 – Summary of Digital Response Time Test Results

SOE File	**TUV S1871153 – After TUV Temp Test Phase 1**	
Trip Response	**Leading Edge**	**Trailing Edge**
SOE File	**TUV Response Time 1 Analysis– After 140°F Test**	
Trip Response	**Leading Edge**	**Trailing Edge**
SOE File	**TUV S1971532 – Mid of TUV Temp Phase 2**	
Trip Response	**Leading Edge**	**Trailing Edge**
SOE File	**TUV S1980850 – End of TUV Temp Phase 2**	
Trip Response	**Leading Edge**	**Trailing Edge**

4.1.2.2 Analog Response Time

The algorithm used to test analog response time consists of a simulated analog trip signal from the HPAT and a DHA block configured to trip when its input reaches 50%. See Figure 9.

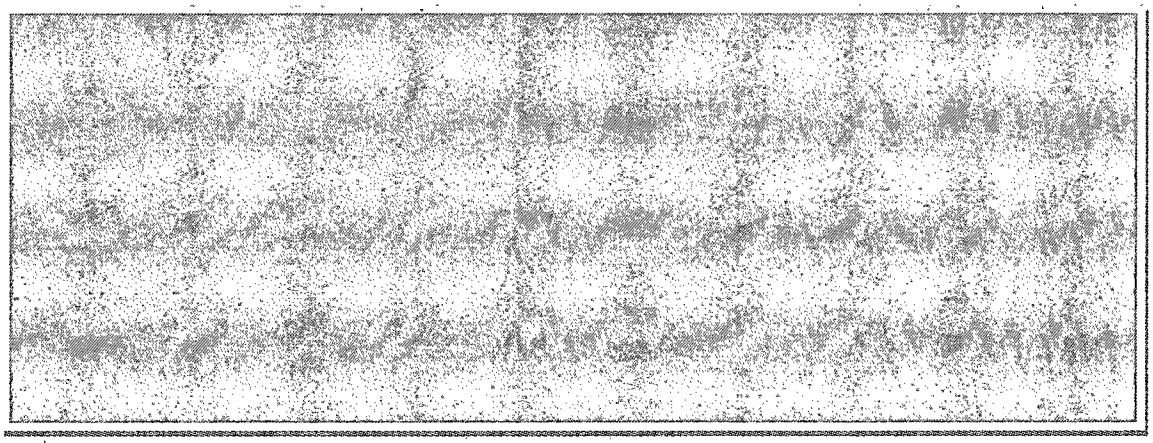


Figure 9 – Analog Response Time Test Algorithm.

Since the HAS logger is limited to a one-second update rate, the SOE logger was used to record the data for this test. In order to produce signals that could be detected by the SOE input card, an external module triggered a relay at the leading and trailing edge of the analog trip signal. Three signals were monitored for the test:

- The analog trip signal (1,AO,2) was generated by the HPAT and controlled the input to the ERD921 test specimen.
- The digital trip output (1,DO,10)

Table 5 – Analog Response Time Test

SOE File	**TUV S1871153 – After TUV Temp Test Phase 1**	
Trip Response	**Leading Edge**	**Trailing Edge**
		
SOE File	**TUV Response Time 1 Analysis– After 140°F Test**	
Trip Response	**Leading Edge**	**Trailing Edge**
		

Average	246 ms	321 ms
SOE File	**TUV S1971532 – Mid of TUV Temp Phase 2**	
Trip Response	**Leading Edge**	**Trailing Edge**
SOE File	**TUV S1980850 – End of TUV Temp Phase 2**	
Trip Response	**Leading Edge**	**Trailing Edge**

4.1.3 Discrete Input/Output Operability Tests

The discrete input operability test demonstrates the capability of each type of discrete input channel to detect a transition in the signal being monitored. The purpose of discrete output operability test was to demonstrate the capability of each type of discrete output channel to operate within its specified range of loading conditions.

During the environmental stress tests, due to the accessibility of the heat chamber, the manual testing of each of these discrete input or output channel were not feasible. Therefore, the prudency BOE test data were used for validating that these channels functioned normally during these stress conditions. See section 4.2 "Prudency Test Results" for detail analyses for the digital signals related to discreet input/output channel operability.

4.1.4 Communication Test

This test monitored the operation of the ICL and C-Link error counters during each phase of the environmental stress test.

Acceptance criteria for this test are that the system and both of its communication links continue operating without disruption before, during, and after application of the stress conditions. Nominal performance of the background tests indicate that the ERD921 test system continued operating reliably, and error logs indicate that no C-Link and no ICL errors were logged during the test.

Data collected from the prudency BOE tests during all environmental stress testing periods also verified that the communication links did not have errors. See section 4.2 "Prudency Test Results" for more information.

4.1.5 Timer Test

The ERD921 TSAP included two algorithms for testing the timer function consisting of four timers:

- One algorithm produced an output waveform that was set for one second on and one second off. This algorithm controlled SOE input point 2,DI,403(Log 1,DO,11).

- The other algorithm produced an output waveform that was set for five seconds on and one second off. This algorithm controlled SOE input point 2,DI,404(Log 1,DO,12).

The accumulated results are listed in Table 6.

Table 6 – Timer Test Results

S1892029	Averaged Period	Ave Value	Accuracy	Avg Value	Accuracy
After 140°F	On				
	Off				
	Total				

The specified acceptance criterion for the timer function is that timer accuracy shall vary by no more than ±1% of the preset value or by more than ±3 scan cycles.

Table 6 shows that the averaged timer period meets the ±1% acceptance criterion in every case. The presence of environmental stress had no impact on the performance of the timer function.

4.1.6 Failure to Complete Scan Detection

The purpose of this test is to demonstrate that the ERD921 system will initiate failover if the controller fails to complete at least one execution of the application program within a context switch period. When the test is initiated, the algorithm forces the application program to enter an infinite loop. When the primary detects failure to complete scan status, it activates an alarm flag and forces failover to the secondary. When failover occurs, the test algorithm is automatically disabled to prevent failure of the secondary controller as well. Two HPAT points, 2,DI,406 and 2,DI,407, were used for measuring the time it took for the failover to occur after an initiation of an incomplete scan event. The test was executed during the high temperature phase. During each test execution, the interval between test activation and generation of the alarm indication was measured And they were all in line with the baseline data collected during the pre-qualification test, which was about ~280ms. Thermal stress had no impact on the ability of the system to detect and respond to this condition.

4.1.7 Failover Test

The purpose of the failover operability test was to demonstrate that the ERD921 test system could transfer control from primary to secondary without disrupting the process under control. The complete test had several phases including a few manual steps for using oscilloscope connecting to specific hardware. Due to the accessibility of the heat chamber, however, only those tests that could be done outside the heat chamber were executed. This

set of tests was performed at the end of high temperature stress, the end of low temperature stress.

There was no impact on stable analog values or analog values in transition during faillover at any environmental stress conditions.

For digital loops, timer function loops were used for validating the impact of failover. There was no impact for the digital loop during failover at any environmental stress conditions. Control transfer to the secondary processor during the failover event was also logged in the alarm file.

By examining the test results, it is concluded that the environment stress conditions, either high temperature stress or low temperature stress, do not have any impact on the failover function of the ERD921 test specimen.

4.1.8 Loss of Power Test

This test was run at the end of the high temperature and low temperature phases of the environmental stress test. The purpose of the test was to demonstrate that output channels went to their inactive levels when power was lost and that they remained in those states until the controller completed its internal initialization.

4.1.8.1 At the End of High Temperature Stress

During the high temperature stress phase, the Loss of Power test was conducted on 7/14/2010 around 7:12pm to 7:22pm. The SOE log files TUV [redacted] and TUV [redacted] shows the system resumed operation without intervention after the power was restored.

4.1.8.2 At the End of Low Temperature Stress

During the low temperature stress phase, the loss of power test was conducted on 7/15/2010 around 1:40pm to 1:45pm. Similar to the high temperature case, the SOE Log files [redacted] shows the system resumed operation without intervention after the power was restored.

The test results show that after the loss of power:

1. All AO channels were open
2. All power output channels were open
3. All solid state relay DO channels were open
4. All mechanical relay DO channels were deenergized

After the power was restored, all operations returned to normal without intervention. These test results show that the environmental stress conditions, high temperature or low temperature, do not have any negative impact to the ERD921 specimen recovering from loss of power.

4.1.9 Power Interruption

The power interruption test subjects the system to a 40 ms interruption in source AC power to demonstrate the capability of the system to continue functional operation during switchover to a backup power source. The test was conducted during the high temperature and low temperature phases of the environmental test with the following background conditions configured:

- Static points were configured to known states
- Automatic accuracy test, response time test, and timer test were running

The following acceptance criteria are specified for this test:

- No controller resets
- No static DO channel changes state
- No static AO point changes its value by more than 5%
- Logged parameters for all of the automated tests remain within tolerance

4.1.9.1 At the end of High Temperature

TUV [redacted] show the data collected during the high temperature execution.

4.1.9.2 At the end of Low Temperature

TUV [redacted] and TUV [redacted] show the data collected during the low temperature execution.

All logs of digital data recorded during these tests indicate normal operation without any disruption.

- There was no indication of any disruption during either the high temperature or the low temperature execution of this test
- Values for both the averaged timer period and accuracy are comparable to those measured without the power interruption
- Values for the automated digital and analog response time are comparable to those measured without the power interruption
- RTD input values for 1,AI,961 and 1,AI,962 (fixed resistor loads) are comparable to those measured without the power interruption. RTD input values for 1,AI,968 (real RTD element) also showed no signs of disruptions
- Changes in values of static points did not occur.

4.1.10 Power Quality

The power quality tolerance test was executed once at the end of the high temperature period of the test. During this test the voltage and frequency of the primary source power were varied over the limits of the ERD921 test system power supplies, and system performance was monitored. The test was conducted on 7/8/2011 from 9:00 AM to 9:18 AM and included three phases:

- **Pretest**, Source power was set to the normal level of 120 vac at 60 Hz (9:00 to 9:03 AM). Automated accuracy, timer, and response time test were run, and selected static point values were monitored.

- **Low voltage limit**. Source power was set to 90 vac at 57 Hz and then to 90 vac and 63 Hz. Then the source voltage was reduced until the power supplies shut down. (9:08 to 9:11:19 AM) System shutdown occurred at 9:11:19 AM. Automated accuracy and BOE tests were run and selected static points were monitored.

- **High voltage**. Source power was set to 150 vac at 57 Hz, to 150 vac and 63 Hz, and then back to 120 vac at 60 Hz. (9:15 to 9:18 AM) Automated accuracy and BOE tests were run and selected static points were monitored.

The automated accuracy tests of the analog cards were running during each phase of this test to demonstrate system stability under varying states of supply power quality. Results for each phase of the test are summarized in the following tables.

Table 7 – HFC-AI16RD

Step Level	Raw Averaged Image	Corrected Average Value	Accuracy
Pretest			
10%			
30%			
50%			
70%			
90%			
Low Voltage Power			
10%			
30%			
50%			
70%			
90%			
High Voltage Power			
10%			
30%			
50%			
70%			
90%			

Table 8 – HFC-AO8FD

Average Source Value (1,BL,506)	Averaged Image Value (2,BL,215)	Accuracy
Low Voltage Power		
High Voltage Power		

All of the results listed in the table above are within specified tolerance for the parameter being measured. When the low power trip occurred, all channels being logged by the HAS registered a value of 0. The ERD921 test system resumed operation approximately 4 minutes later.

4.1.10.1 Miscellaneous Points

Various static points were monitored to detect spurious transitions. The following results were obtained during the pretest with power set to normal levels:

- There was no record for any static digital point logged during the test, indicating that no spurious DI or DO transition occurred.
- 1,CO,50 was the equation cycle counter. It logged between 30 and 32 (30.81 average) cycles every second.

Indications during the low and high voltage phases are as follows:

- There was no record for any static digital point logged during the test, indicating that no spurious DI or DO transition occurred.
- 1,CO,50 logged between 30 and 32 cycles per second until the low power shutdown. Immediately after operation resumed, it logged one record of 94 counts over a two-second interval and then resumed logging between 30 and 32 counts per second.
- 1,BL,510 and 1,BL,201 exhibited normal image for dynamic operation of the analog BOE. Both images indicated a 0 value at low power shutdown and then resumed normal operation when power was restored.

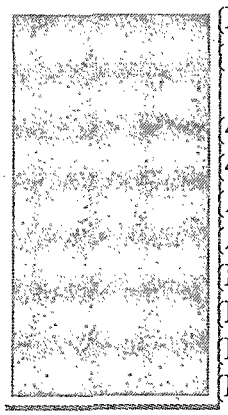
- 1,CO,10 and 1,CO,11 are the C-Link error counters. A record of 0 counts was logged at low power shutdown and again when power was restored.

4.2 *Prudency Tests*

4.2.1 Digital Burst of Event Tests

The digital BOE test was executed before, during and after the environmental test conducted on the ERD921 test specimen. Two of the source signals were logged directly – 2,DO,408 and 2,DO,409. These two signals are 180 degrees out of phase, and they are slightly asymmetric due to the characteristics of the timer function in the HPAT. This asymmetry produced a small part of the reported deviation; the remainder was produced by the processing of the ERD921 Test Specimen and the TSAP logic. In each case, the signal source was connected to a DI channel of the ERD921 test specimen, and the resulting image drove a DO channel, which controlled the input to the SOE logger. Different paths through the TSAP produced different total transfer delays from input to output, but the delay from transition to transition was expected to be consistent with that of the signal source. As indicated in the SOE logs, the averaged HI/LO interval was within tolerance for every test run.

SOE Logs:



(End Phase 1)
140°F)
(140°F)
40°F)
40°F)
Ambient)
Ambient)
Mid Phase 2)
Mid Phase 2)
End Phase 2)
End Phase 2)

Every transition was present within the stipulated tolerance of ±0.15 second. Even though there was a slightly longer delay over the tolerance limit, all transitions were recorded. These results also validated the discrete operability input/output functionality of the test specimen.

4.2.2 Analog BOE data

The analog BOE test TSAP arrangements for AI16RD and AO8FD channels are as follows:

- The HAS logged the following points to record data for this test channel: AI source (1,BL,52), Inverted AI Source (1,BL,53), AO Source (1,BL,83), Inverted AO Source (1,BL,88).

Acceptance criteria for the analog BOE test are as follows:

AI Image	Each transition is present in the logged image data. The averaged image at each level remains within ±0.35% of the source signal based on a full span of 100%.
AO Image	Each transition is present in the logged image data. The averaged image at each level remains within ±0.32% of the source signal based on a full span of 100%.

TMR BOE HAS data collected during BOE were within acceptance range. All results obtained were within the limits specified for acceptability and consistent with the results obtained during the baseline test.

5.0 Conclusions

The retest of ERD921 test specimen in accordance with EPRI TR 107330-1996 environmental envelope demonstrated that the HFC-6000 platform remained fully operational at different environmental stress conditions: high temperature 60°C/140°F for at least 48 hours, low temperature 4°C/40°F for at least 8 hours, and back to ambient after the cycle of the stressed conditions.

6.0 QA Records

The test results recorded in the test documents during the tests (see section 2.2) shall be preserved in accordance with QPP 17.1 "Quality Records" as nuclear records.

7.0 Attachments

None.