HF Controls

HF CONTROLS CORPORATION

HFC-6000 Control System

ERD921 - Qualification Test

Summary Report for Burn-in Tests, Setup and Checkout Test, TSAP Validation Test

TR901-201-01 Rev. A

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Revision History

Date	Revision	Author	Changes
9/6/11	A0	Y. Lu	Initial Release
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1.0 PURPOSE AND SCOPE

This report documents the results from the burn-in, setup and checkout tests performed on the test specimen for project ERD921. These prequalification tests serve to validate that the test specimen meets the hardware and system application acceptance criteria before the first execution of the Operability and Prudency tests which then provide a system performance baseline for subsequent qualification tests.

This report describes the types of tests performed, provides a summary of the test results, and evaluates those results based on the acceptance criteria.

2.0 REFERENCES

2.1 INDUSTRY STANDARDS

EPRI TR-107330	Generic Requirements Specification for Qualifying a Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants, 1996

2.2 RELATED PLANS AND PROCEDURES

500408-01	ERD111/ERD921 Power Distribution System Cabinet, Rev. D
500409-01	Loop Layout for ERD111/ERD921 TUV, Rev. B
700901-09	ERD111 TSAP Requirements Specification, Rev. C
700901-10	HPAT Requirements Specification, Rev. A
700907-01	ERD921 TSAP Loop Layout, Rev G
700908-01	Schematic Wiring Diagram HPAT, Rev. G
700912-03	TSAP System Assembly, Rev. B
ASC0401	TSAP Program Listing, Rev B
TP0408	ERD111 TSAP Validation Test Procedure, Rev D1
TP901-200-01	EPRI TR 107330 Burn-in Test Procedure, Rev. B
TP901-201-02	TUV DMR Integration Test Plan, Rev B
TP901-202-02	TUV TMR Integration Test Plan, Rev B
TP901-203-02	TUV SLC Integration Test Plan, Rev B
TP901-201-03	DMR TSAP Validation Test Plan, Rev B
TP901-202-03	TMR TSAP Validation Test Plan, Rev B
TP901-203-03	HFC-SBC04A SLC TSAP Validation Test Plan, Rev B
TP901-201-04	DMR Operability Test Procedure, Rev E
TP901-202-04	TMR Operability Test Procedure, Rev D
TP901-203-04	SLC Operability Test Procedure, Rev C
TP901-201-05	ERD921 DMR Prudency Test Procedure, Rev B
TP901-202-05	ERD921 TMR Prudency Test Procedure, Rev C
TP901-203-05	SLC Prudency Test Procedure, Rev B
VV0414	ERD111 Master Configuration List, Rev E
VV901-300-01	ERD111-ERD921 Qualification Master Test Plan, Rev B
VV901-301-02	TUV DMR Master Configuration List, Rev C
VV901-302-02	TUV TMR Master Configuration List, Rev C

VV901-303-02	HFC-SBC04A System Master Configuration List, Rev C
VV901-301-01	TUV DMR Test Specification Design Description, Rev A
VV901-302-01	TUV TMR Test Specification Design Description, Rev B
VV901-303-01	HFC-SBC04A SLC Test Specification Design Description, Rev A

2.3 HFC INTERNAL STANDARDS AND PROCEDURES

QPP 5.1	Review and Approval of Quality Documents
QPP 11.1	Test Control
WI-ENG-003	Configuration Management
WI-ENG-205	Develop Software/Firmware Test Procedure

2.4 SPECIAL TERMS, ABBREVIATIONS, AND ACRONYMS

EWS	Engineer Workstation
HPAT	HFC Plant Automatic Tester
FOT	Fiber-Optics Transmitter
MCRT	Microsoft (Windows) CRT
LED	Light Emitting Diode
OIS	Operator Interface System
PCB	Printed Circuit Board
TSAP	Test Application which is a synthetic application program to be used for qualification testing

3.0 BURN-IN TEST

The burn-in test requires a minimum period of 352 cumulative hours of operation. The purpose of this test is to detect any early-life failures of components and circuit cards. During the test period, all cards under test must remain in a normal operating state. Only those cards that pass the burn-in test will be placed into inventory for subsequent use as part of the HFC-6000 Test Specimen.

3.1 PCB CARDS TESTED

The following circuit card assemblies, which were in the HFC-6000 SER, were included in the burn-in test.

Table 1 – HFC-6000 Safety Platform Equipment List

Module Type	Description
HFC-BPC01-19	14 slots Controller Rack with mother board
HFC-BPE01-19	14 slots I/O Expansion Rack with mother board
HFC-SBC06	Controller Board (CPU)
HFC-SCG06	Communication Gateway Board
HFC-DPM06	Dual Port Memory
HFC-DO16C	16 channel Digital Output Board
HFC-DI16I	16 channel Digital Input Board
HFC-AO8FD	8 channel Analog Output Board
HFC-AI8MD	8 channel RTD Board
HFC-AI8LD	8 channel Thermocouple Board
HFC-HUB06-16	Communication Link HUB Board
HFC-FOT-06	Fiber Optic Transceiver Board
HFC-ILR06	Fiber Optic ICL Interface Board
RPS-25-SYSTEM-M1181	Jasper Power Supply Rack
HML601-5-1182	Jasper 24VDC Power Supply

3.2 ACCEPTANCE CRITERIA

The card edge LEDs for each card under test indicates normal operation of the card during the test interval and is an indication of the successful operation of the card during the burn-in test.

3.3 TEST RESULTS

The assemblies under burn-in test were verified periodically every day and the status was logged into an electronic database. If and when a card fails the burn-in test, it was repaired, and the test will be restarted for the repaired card to ensure that all cards reach a minimum of 352 cumulative hours of operation without failure.

3.4 CONCLUSION

Cards that passed the 352 cumulative hours of operation were retained for subsequent use as part of HFC-6000 Test Specimen.

4.0 SET-UP AND CHECK-OUT TEST

The purpose of this procedure is to verify that the project specified hardware, wiring, and communication cabling has been installed correctly and that communication has been established over each communication link prior to performing TSAP Validation Test.

4.1 TEST SEQUENCES

Included in the scope of these tests are the following activities:

- Verify that all project specified equipment / hardware has been received, functionally tested, and set-up per project documents.
- Verify correct software is installed in Test Specimen, HPAT, and OIS/EWS.
- Perform a continuity test for circuits depicted on Drawings 500408-01.
- Verify that C-Link communication has been established.
- Verify that all HFC-6000 I/O modules are functional and communicating properly with HFC-SBC06 controllers.

4.2 ACCEPTANCE CRITERIA

The overall method used for verifying correct hardware component installation and functional operation consisted of highlighting the relevant engineering drawing(s) as each item was verified to be operating correctly.

4.2.1 Equipment / Hardware

1. All hardware components and communication cables depicted on the BOM and drawing 700912-03 have been highlighted.
2. All Test Specimens' PCBs depicted on drawing 500409-01 have been highlighted.
3. All connection shown on Drawing 700907-01 and 700908-01 have been validated and highlighted.

4.2.2 Continuity Test

1. All circuits depicted on drawing 500408-01 have been highlighted.
2. Drawing and BOM 700912-03: BOM Mark Numbers: 5, 16, 19, 21, 23 and 33 have been highlighted.

4.2.3 C-Link Test

1. Verified that the EWS Memory Editor can read memory from SBC06, and verified that EWS are receiving DDB from Test Specimen.
2. Verified that the Remote Status screen values of Test Specimen and HPAT both remain at 04 or 05.

4.2.4 I/O Functional Test

1. Digital Inputs: All digital inputs channels on the Loop Schematics have been highlighted.
2. Digital Outputs: All digital outputs channels on the Loop Schematics have been highlighted.
3. Analog Input (0-20 mAdc): All analog inputs (0-20 mAdc) channels on the Loop Schematics have been highlighted.
4. Analog Outputs: All analog outputs (0-20 mAdc) channels on the Loop Schematics have been highlighted.
5. RTD Input (100 Ohm Platinum): All RTD inputs channels on the Loop Schematics have been highlighted.
6. Pulse Input: All pulse input channels on the Loop Schematics have been highlighted.

4.3 TEST RESULT

- Equipment / Hardware

  BOM and Drawing 700912-03 "TSAP System Assembly", and Drawing 500409-01 "Loop Layout for ERD111/TUV were verified and signed off by test engineers.

- Continuity Test

  Continuity checks were performed on Drawing and BOM 700912-03 "TSAP System Assembly" and Drawing 500408-01 "ERD111/ERD921 Power Distribution" and test logs were signed off.

- C-Link Communication Test

  Data broadcasting using EWS/OIS is validated by C-Link function and the test logs are signed off.

- I/O Functional Test

All digital and analog IO cards were tested individually for functionality. Excel file was created and individual test results were retained as Quality Documents. Test logs were signed off upon completion.

4.4 CONCLUSION

Test results have met all acceptance criteria for set-up and check-out test. These results and the analog accuracy test results from subsequent baseline testing will be used for comparison to accuracy results from future stress testing.

5.0 TSAP VALIDATION TEST

A synthetic application program, TSAP, installed in the test specimen includes sample control logic for power plant processes as well as logic to support automated qualification testing.

5.1 TEST SEQUENCE

The overall validation test is accomplished in two stages: source code verification, and system functional test. During source code verification, the content of the source code text files are validated against the logic diagrams from which they were created. During the functional test, the application code is installed in the controller, and functional operation of the Operability tests, Prudency Burst of Events test, and simulated control loops are verified to be correct. The test sequence includes the following activities:

- **Source Code Verification** – The source code file generated by the HFC One-Step utility program is examined line by line and compared with the graphic representation of logic diagrams 700907-01, and 700908-01.

- **Loop Logic Test** – This test verifies functional operation of the logic for each sample control loop based on the algorithm in the TSAP logic diagrams.

- **Operability Test Support** - This test verifies functional operation of the TSAP code designed to support Operability testing and verifies that the test design produces the expected data. The automated Operability tests are controlled by application code installed in the HPAT. Execution of this test does not include automated logging of test results; it is to be accomplished during the first execution of the subsequent Operability tests.

- **Prudency Test Support** - This test verifies functional operation of the TSAP code designed to support the automated Prudency tests. The automated Prudency tests are controlled by application code installed in the HPAT. Execution of this test does not include automated logging of test results; it is to be accomplished during the first execution of the subsequent Prudency tests.

5.2 ACCEPTANCE CRITERIA

Acceptable results for the TSAP are based on the verification of the specific conditions listed in Table 5.1.

***Table 2* – Acceptance Criteria**

Source Code Verification	
	All point types and point designations match those in the logic diagrams.
	All logic connections traced from point to point match the connections shown in the logic diagrams.
	All timer preset values match those shown in the logic diagrams.
	All internal block structures contain the values shown in the logic diagrams.
Accuracy Tests	
	MCRT interface enables test engineer to start/stop the automated accuracy test.
	All AI and AO channels listed for the automated accuracy test exhibit the test waveform while the test is enabled.
	Response time of the system to each step is sufficient to permit accurate recording of the AI and AO channel performance.
	RTD AI channel configured and reads cabinet ambient temperature.
	The two AI4Ks are configured with one channel pair in Rate mode and the other channel pair in Accumulate mode.
	The two AI4Ks pulse cards respond to simulated input signal correctly.
Digital Response Time Algorithm	
	MCRT interface enables test engineer to start/stop automated response time test algorithms.
	While digital response time test is running, the TSAP algorithm produces a free running square wave composed of 7 DI channels and 7 DO channels.
	HPAT algorithm produces a free-running 0.5 Hz square wave.
	The HPAT algorithm drives a simulated trip memory in the TSAP, which controls a DO channel in the Test Specimen.
Analog Response Time Algorithm	
	MCRT interface enables test engineer to start/stop automated response time test algorithms.
	The HPAT algorithm produces a DO signal that controls an analog square wave that switches between 0 and 5 v.
	The TSAP algorithm provides an alarm block to trigger a simulated trip memory.
	The AI signal triggers a simulated trip output when it reaches 50% of span; it also controls an AO channel that toggles a hardware relay to permit SOE logging.
Operability Timer Test	
	MCRT interface enables test engineer to start/stop automated time test algorithms.
	TSAP provides four timers that produce two free-running square waves while the test is enabled.

	Test waveforms enable direct measurement of periods for 1-second and 5-second timers (plus jitter).
Failure to Complete Scan Test	
	When an input triggers a logic which runs longer than 100ms, the primary controller fails, and the secondary controller takes over operation as primary.
	Manual reset of the failed controller restores normal operation.
TSAP Special Functions	
	1,CO,50 increments once each Equation Interpreter processing cycle. This running count provides a precise indication of processing speed during any fixed period of time.
	The TSAP monitors status of each power supply. Failure of any power supply triggers a common power monitor alarm.
	The analog accuracy test waveform drives the two CSM panel meters.
Burst of Events Test	
	MCRT interface enables test engineer to start/stop automated burst of events test algorithms.
	HPAT controls two digital bursts of events 0.5 Hz square waves that are 180 degrees out of phase.
	HPAT controls an analog burst of event 0.5 Hz square wave that switches between 10% and 90% of span.
	While the test is running, all points listed in Table 5 exhibit activity. When the test is disabled, all of these points remain static.
Simulated Digital Control Loops	
	MCRT provides display interface for controlling inputs to the control loop and for monitoring overall loop status, including alarm conditions.
	CSM for this loop enables user to clear alarm status and enter stop/start command inputs.
	TSAP functional response to each DI channel connected to the internal logic verified for both TRUE and FALSE logic states.
	TSAP control of each DO channel connected to internal logic verified based on logic input states.
	TSAP control of alarm status verified based on simulated alarm conditions.
Simulated Analog Control Loops	
	MCRT provides display interface for controlling digital inputs associated with the analog control loops
	M/A station enables user to switch between Auto and Manual mode.
	In Manual mode, M/A station permits manual control of the loop output variable.
	HPAT algorithm provides closed-loop simulation of an external process.
	After tuning is complete, the closed loop simulation enables the loop to reach a balanced state while operating in Auto mode without oscillation.

5.3 TEST RESULT

- **Source Code Verification**

  The TSAP source code was verified to assure the functional requirements were correctly implemented. All deviations were documented and corrected. The corrections were verified. The source code verification was signed off properly by the V&V team.

- **Accuracy Tests**

  The main purpose of these tests was to validate the MCRT trigger and TSAP functionality. The accuracy algorithms were validated and were signed off properly by the V&V team.

- **Digital Response Time Algorithm**

  The cascaded algorithm within the TSAP program was validated. The algorithm can be trigged from the MCRT. Simulated trip output generated by TSAP in response to transitions of trigger signal was also validated. This test was performed by and signed off by the V&V team.

- **Analog Response Time Algorithm**

  The HPAT algorithm was verified during the test, it is triggered to start or stop by the MCRT. This test was performed by and signed off by the V&V team.

- **Operability Timer Test**

  This algorithm was validated during the test; it is started or stopped by the MCRT. This test was performed by and signed off by the V&V team.

- **TSAP Special Functions**

  BOE timer preset values of 1 second, 1.5 seconds, and 10 seconds were used to produce the response curve for the TSAP. The counter 1,CO,50 maintained a running count of processor cycles. The TSAP generated a power fault alarm on failure of any power module. The analog accuracy test controls displayed two AO channels reserved for driving CSM meters. All TASP special functions were tested and signed off properly by the test engineer against the acceptance criteria.

- **Burst of Events Test**

  The test algorithm was started and stopped by MCRT. Digital algorithm consists of a 0.5 Hz square wave. Analog algorithm consists of an analog square wave (10 seconds high, 10 seconds low) that switches between 10% and 90% of span. Each point listed for the Burst of Events test exhibits activity while test is running. All

BOE related functionalities were tested and signed off properly by the test engineer against the acceptance criteria.

- **Simulated Digital Control Loops**

  This test verifies many functionalities of the simulated digital control loop. Each digital control loop communicates with its CSM. MCRT interface enables manual control of defined DI signals for the control loops and displays simulated alarm status conditions. Manual inputs from CSM switches supply operator control inputs to the control logic. Each combination of logic states was exercised individually to verify overall control functions. Each connected DI signal for each digital control is read and processed in accordance with the functions depicted on its loop logic diagram. The logic of each simulated control loop produces the expected combination of status outputs for the specific combination of input conditions. Each simulated digital control loop was tested and signed off properly by the test engineer against the acceptance criteria.

- **Simulated Analog Control Loops**

  This test verifies many functionalities of the simulated analog control loop. Each analog control loop communicates with its M/A station. Switches on the M/A station enable selection of Manual or Auto mode. Logic in the HPAT provides a simulation of an external process, permitting closed loop operation of the PID loop. After the feedback loop is tuned, the TSAP logic controls its output without oscillation. Each level alarm was verified individually, and each output controlled an alarm indication on the MCRT display. Each simulated analog control loop was tested and signed off properly by the test engineer against the acceptance criteria.

- **Failure to Complete Scan Test**

  Test was performed by and signed off by the V&V team.

5.4 CONCLUSION

The TSAP validation results demonstrated that the TSAP source code generated from the One-step program development tool reflects the logics depicted in the control schematics. Algorithms in TSAP were validated for supporting the required operability and prudency testing. TSAP special functions, simulated digital and analog control loops were validated that the functions in TSAP correctly execute the controls described in schematics.